10 GHz Ultra-High Speed GaAs Decision Circuit Design

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Abstract

Giga-bit level IC design has already been progressed by GaAs MESFET technology. This work is to present a 10Gbps ultra-high speed design with sensitive decision circuit using 0.5 μm gate MESFET technology. The decision circuit is basically consisted of Master-Slave type D-FF, source-coupled FET differential amplifier named Source-Coupled FET Logic(SCFL) circuit. This GaAs digital SCFL circuit includes two FETs(E-mode MESFET and D-mode MESFET) and also includes some of resistors and diodes between input signals and ground. Source-follower generally minimizes the load of the SCFL and is included in the output node to improve the performance. Based on the fabricated 0.5 μm devices, process parameters are successfully extracted and optimized to check for 10 GHz operation from the D-FF SCFL decision circuit using circuit simulator before real GaAs IC process fabrication. The GaAs SCFL circuit was operated at 10 Gbps ultra-high speed level, which is designed for future high speed optical receivers.

I. Introduction

GaAs IC and system technology has been paid much attention to the field of ultra-high speed IC design since the beginning of 1980[1]-[3]. GaAs, one of the most promising next semiconductor materials, also has demonstrated many advantages over silicon material such as 5-8 times faster speed, high resistance against reactor[4]. GaAs manifests light-emitting characteristic and thereby its researches are actively progressing. GaAs high speed digital circuit was introduced by HP in 1973 and 4 Gbps high speed with recess gate FET and epitaxial substrate has reported in 1977[5]. Lately GaAs ICs such as NOR/OR standard logic IC, FF, counter, frequency divider, AD converter which are being used in high speed communication systems and instrumentation system are already commercialized. Most of current high speed systems adopted ECL technique in voltage and signal level to provide compatibility for currently used ECL IC, however trend in voltage and signal level by GaAs technique has been realized[6][7]. As a result, Giga-bit level IC design is already progressed by GaAs MESFET technology. This research is to present a 10Gbps ultra-high speed design with sensitive decision circuit using 0.5μm gate MESFET technology. The decision circuit is basically consisted of D-FF from SCFL(Source coupled FET logic)[6]-[8].

II. GaAs MESFET Devices

It is important to choose an accurate DC model for all operation region. Inaccurate DC model may result in improper prediction and extreme process and temperature for a desired circuit performance and therefore circuit may not work properly. The accurate DC model parameters are implemented into circuit simulator to check for the circuit validity. Fig. 1 shows an equivalent model of the MESFET device. Intrinsic drain current $I_{DS}(V_{GS,i}, V_{DS,i})$ is an important MESFET device characteristic. The basic I_{DS}-V_{DS} model in Eq. (1) based on[8][9] shows a good agreement with fabricated measurement as shown in Fig. 2.

$$I_{DS} = [\frac{\beta(V_{GS,i}-V_T)^2}{1+b(V_{GS,i}-V_T)}](1+\lambda V_{DS,i})\times [1-(1-\alpha\frac{V_{DS,i}}{3})^3] \quad \text{for } 0 < V_{DS} < 3/\alpha \qquad (1a)$$

$$I_{DS} = [\frac{\beta(V_{GS,i}-V_T)^2}{1+b(V_{GS,i}-V_T)}](1+\lambda V_{DS,i}) \quad \text{for } V_{DS} \geq 3/\alpha \qquad (1b)$$

where $V_{GS,i} = V_{GS}-I_D R_S$ $V_{DS,i} = V_{DS}-I_D(R_S+R_D)$, **b**, α, β, λ are fitting parameters and others have

their standard meanings. The b, α, β, λ should be determined.

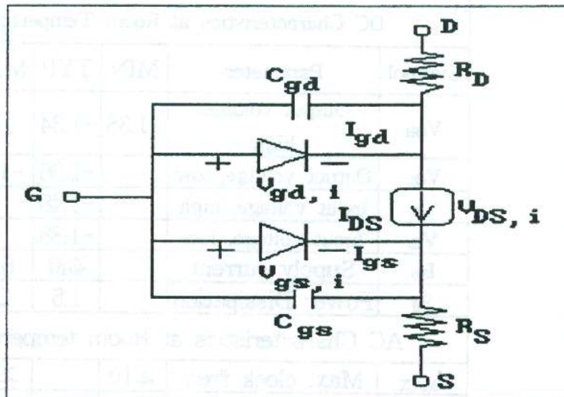


Fig. 1. An equivalent model of MESFET.

to design the Master-Slave(MS) type D-FF decision circuit accurately. The $0.5\mu m$ gate length E/D-MESFET parameters are extracted from fabricated devices as shown in Table 1. Fig. 2 shows drain-voltage characteristic for D(depletion-mode)-MESFET at the gate bias step of 0.1 v. Models in Eq. (1a) and (1b) agree well with the measurement results in Fig. 2 as aforementioned.

Table. 1. Extracted parameters for D-MESFET devices.

Parameters	E-MESFET	D-MESFET
vto	0.27	-0.3
alpha	8.8	5.48
beta	4.21e-4	5.53e-4
lambda	0.9	0.31
b	0.3	0.3
rd	927	927
rs	927	927
cgs	0.7e-15	0.7e-15
cgd	0.14e-15	0.14e-15
pb	0.65	0.65

As shown in Fig. 3, the transconductance g_m for the $0.5\mu m$ gate length E/D-MESFET with gate width of $20\mu m$ is determined by the transfer characteristic I_{DS}-V_{GS} at a drain bias V_{DS}= 1V. A g_m's as high as 379 mS/mm for D-MESFET and 279 mS/mm for E-MESFET are obtained[4].

III. Results and Discussion

Differential amplifier circuit is widely being used for circuit applications. Bipolar ECL or CML circuit is a good example. Such technology can

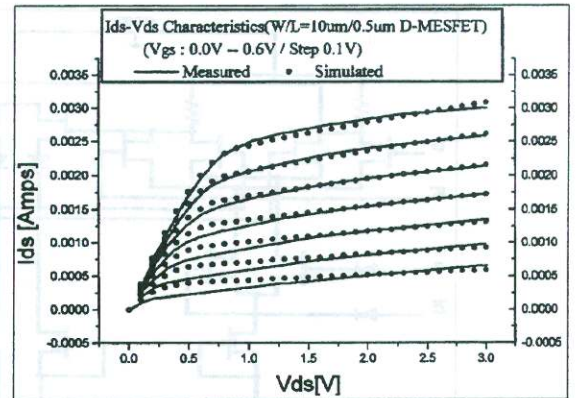
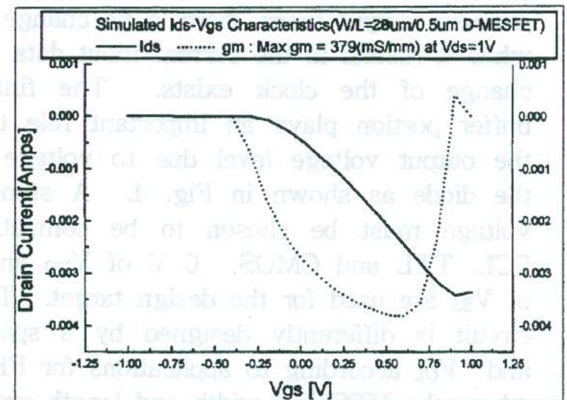


Fig. 2. I_{DS}-V_{DS} characteristic for D-MESFET

be also applied to GaAs MESFET logic circuit. Fig. 4 shows the D-FF decision circuit using Source-Coupled FET Logic(SCFL) whose circuit is composed of three blocks: clock input block, data input block, and output buffer block. This GaAs digital D-FF circuit includes two FETs(E-mode MESFET and D-mode MESFET) based on SCFL differential amplifier circuit and also includes some of resistors and diodes



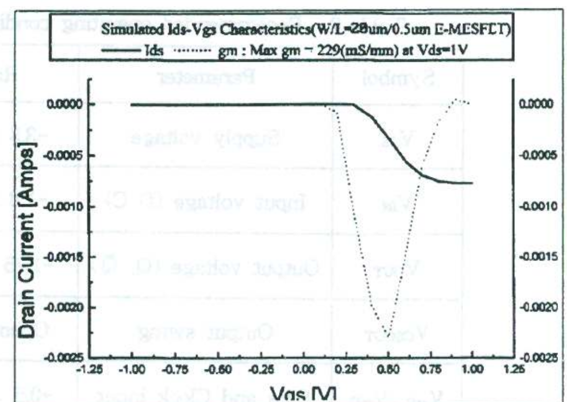


Fig. 3. Transfer characteristics for (a) D-MESFET; (b) E-MESFET.

between input signals and ground. source-follower

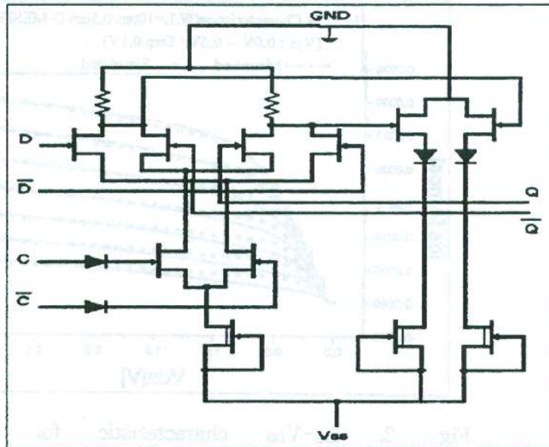


Fig. 4. D-FF decision circuit using SCFL.

generally minimizes the load of the SCFL and is included in the output node to improve the performance. However, it can be ignored when the load is small. Note that resistors at drain node rather than FET passive load are used to simplify the SCFL gate biasing. For the data input block, two input data(D, D̄) and two signals which are feedbacked from output buffers are given as inputs. The output remains as the previous output when there is no change in clock, while it results in the current input data when the change of the clock exists. The final output buffer portion plays an important role to control the output voltage level due to voltage drop by the diode as shown in Fig. 4. A standard V_{DD} voltage must be chosen to be compatible with ECL, TTL and CMOS. 0 V of V_{DD} and -3.5 V of V_{SS} are used for the design target. The SCFL circuit is differently designed by a specific V_{OH} and V_{OL} according to applications for FET's area where the MESFET width and length are 20 ㎛

Table 2. Recommended operating conditions

Symbol	Parameter	Rating
V_{SS}	Supply voltage	-3.5 ± 0.2V
V_{IN}	Input voltage (D C)	-1.8 ± 0.2V
V_{OUT}	Output voltage (Q, Q̄)	-1.75 ± 0.4V
V_{CSOUT}	Output swing	Open ~ Vss
V_{ref1}, V_{ref2}	Data and Clock input	+0.5 ± 0.25V
T_{stor}	Temperature ranges	-60℃ ~ +150℃

Table 3. DC voltage levels(Vss = -3.4V~-3.75V, GND = 0.0V, Tc = 0 ~ 85℃) and AC characteristics

Symbol	Parameter	MIN	TYP	MAX	Units
DC Characteristics at Room Temperature					
V_{OH}	Output voltage, high	-1.38	-1.34		V
V_{OL}	Output voltage, low		-1.96	-1.88	V
V_{IH}	Input voltage, high		-1.48		V
V_{IL}	Input voltage, low		-1.88		V
Iss	Supply current		440	615	mA
P_d	Power Dissipation		1.5	2.3	W
AC Characteristics at Room temperature					
f_{MAX}	Max. clock freq.	≥10		≥10	GHz
t_r	Output rise time		40	55	ps
t_f	Output fall time		30	50	ps
V_{INmin}	Minimum data input swing		30	100	mV_{p-p}

and 0.5㎛, respectively, source current, and drain resistance. Noise margin is designed to satisfy for two conditions; one is the logic swing ΔV should be less than $0.7-V_T$ where V_T is the pinchoff voltage, but FET is switched between ohmic region and cutoff region. The other is enough level-shifting between the input and the output should be controlled for source-drain voltage to avoid the ohmic region. In this report, absolute recommended operating conditions and voltage levels are listed in Table 2 and Table 3. The input signal and its reference input are provided into the SCFL circuit which is a type of D-FF that is operated by output signals.

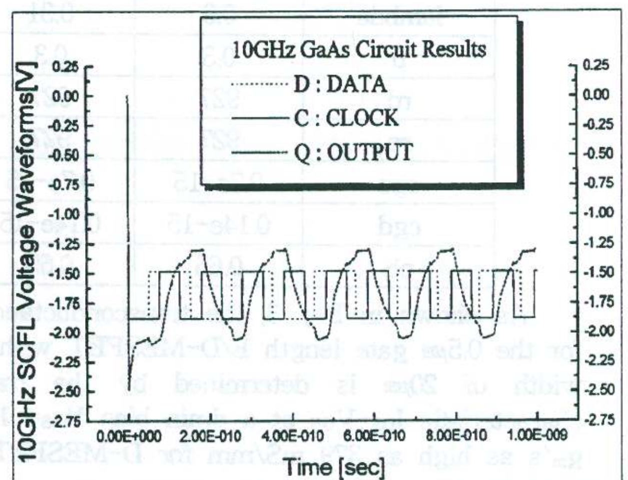


Fig. 5. Simulation result of D-FF SCFL decision circuit when gate-source capacitance and gate-drain capacitance are 1.0(fF) and 0.2(fF).

Output(dotted line: Q) shows the 10 GHz range. Voltage levels of each node based on DC

operating points are adjusted and then changed to normal input signals to simulate the decision circuit properly. Fig. 5 demonstrates the output waveforms, confirming a 10 GHz ultra-high speed operation with the range of -1.62V to -2.02V in input data, resulting in -1.26V through -2.17V of output voltage waveform. However Fig. 6 with more than 1.4(fF) and 0.28(fF) in gate-source and gate-drain capacitance shows that output waveform(Q) did not reach out the desired maximum and minimum voltage swing, which means the D-FF SCFL circuit would not operate at the 10GHz level. The reasonable values of 1(fF) and 0.2(fF) in gate-source and gate-drain capacitance demonstrates a successful 10 Gbps level operation as shown in Fig. 5. A 0.5μm MESFET device process technology to obtain low capacitances would result in desired circuit performance.

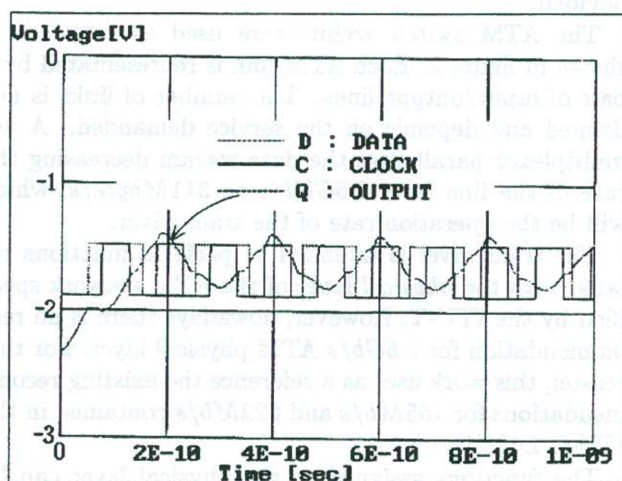


Fig. 6. Simulation result of D-FF SCFL decision circuit when gate-source capacitance and gate-drain capacitance are 1.4(fF) and 0.28(fF).

Ⅳ. Conclusions

Based on the fabricated 0.5 μm devices, process parameters are successfully extracted and optimized to check for 10 GHz operation from the D-FF SCFL decision circuit using circuit simulator before real GaAs IC process fabrication. The GaAs SCFL circuit was operated at 10 Gbps ultra-high speed level, which is designed for future high speed optical receivers.

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