Implementation of a 2.5Gb/s ATM Transceiver in GaAs Technology

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Abstract

In this paper we present a 0.6μm GaAs MESFET implementation for a 2.5Gb/s ATM transceiver. The good power-delay feature of the technology, gives a power consumption below 5W for the transceiver. Due to the lack of recommendations for 2.5Gb/s ATM physical layer, the work presented uses the existing recommendations given by the ITU-T for 155Mb/s and 622Mb/s.

Introduction

The *Broadband Integrated Services Digital Network* (B-ISDN) is becoming highly usable in communications where the requirements imposed by the applications are reaching the bandwidth limits. *Asynchronous Transfer Mode* (ATM) has been chosen to perform the targets proposed by B-ISDN. To fulfill the potentiality assigned to B-ISDN, both switching and transmission capacities today available must be widened, designing systems in the Gbit/s range. This requires to improve conventional technologies to go further. Another option is the use of new technologies combined with architectural strategies which allow improvements in the performance of the whole system.

Gallium Arsenide (GaAs) nowadays offers a maturity degree allowing VLSI levels combining both high-speed and low-power consumption. Furthermore, power consumption is not affected by clock frequency giving advantage over Silicon in those systems computationally-intense with high frequency of operation. These ATM subsystems are a challenge for conventional technologies (CMOS), and there is no other solution than massive parallelisms, even using BiCMOS.

In this article we introduce aspects of a transceiver architecture and how to overcome problems related with high frequency rates. Medium convergence functions in the physical layer of the ATM will be discussed in detail and results will be given in terms of area and power consumption. in order to fulfill the characteristics required for a 2.5Gb/s ATM transceiver.

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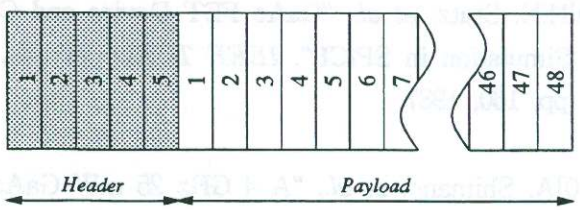

Fig. 1. *Asynchronous Transfer Mode* cell

ATM System description

The ATM transmission is based on fixed size cells. Each cell —in the ITU-T standards— is composed by a header of 5 bytes and 48 bytes of payload as it is shown in figure 1. The header carries 4 bytes with — among other information— a label identifying this cell belonging to a *virtual path* and to a *virtual channel*. The final byte of this header is the *header error control* byte (HEC). There is no error control over the 48 bytes of payload.

The ATM switch architecture used as reference is shown in figure 2. Each ATM link is represented by a pair of input/output lines. The number of links is not defined and depends on the service demanded. A demultiplexor parallelizes the data stream decreasing the rate of the line from 2.5$Gbit/s$ to 311$Mbyte/s$, which will be the operation rate of the transceiver.

The transceiver is intended to perform functions related with the *physical layer* of the ATM network specified by the ITU-T. However, nowadays there is no recommendation for 2.5Gb/s ATM physical layer. For this reason, this work uses as a reference the existing recommendations for 155Mb/s and 622Mb/s contained in the ITU-T I.432[1].

The functions assigned to the physical layer can be

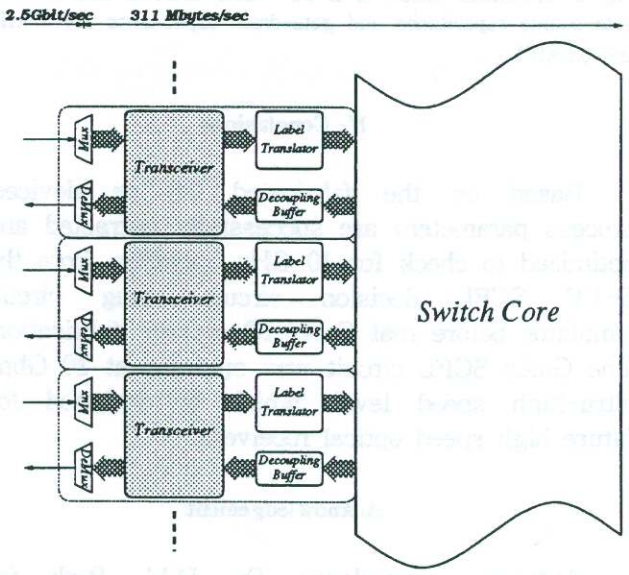

Fig. 2. ATM switch reference architecture

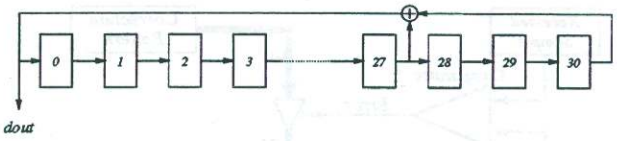

Fig. 3. Serial Scrambler

classified into two main groups: *Medium Convergence* and *Operation and Maintenance* (OAM). This work deals in detail with medium convergence functions. The main tasks assigned to the medium convergence are the scrambling, header control error, discrambling and cell delineation.

A label translator follows the transceiver mapping old cell labels to new ones and adding routing information to the cell. Then, the cells go through the switch core, after which they go to a buffer which decouples the switch rate with the line rate. Then, the transceiver inserts the header error control byte, and scrambles the data stream. Finally, a multiplexor converts from $311Mbyte/s$ to $2.5Gbit/s$.

The frequency of operation of the transceiver will be $311MHz$. This means that the internal structures of computation must be transformed to process a byte per cycle, instead of a bit per cycle. This parallelization is not trivial in most of the cases and requieres a detailed study.

Transceiver implementation

To carry out this system, a convenient architecture must be chosen. As mentioned before, in order to lower the clock frequency, a eight-bits-parallel implementation is selected so the clock frequency is reduced to $311Mhz$. This frequency is easily handled by *GaAs* MESFET Technologies, so that instead of speed, much of the effort was focussed on noise margin and power consumption optimization. Parallelization increases the complexity of the system. In order to overcome this drawback, most of the functions in the transceiver are byte-oriented (one byte per clock cycle is processed),

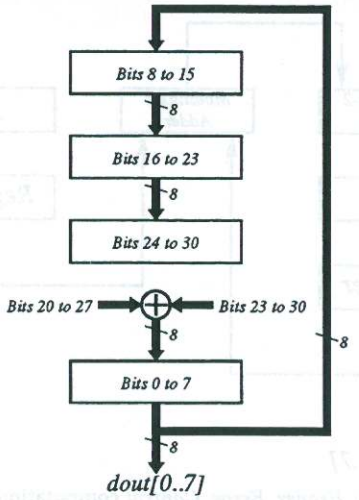

Fig. 4. Parallel Scrambler

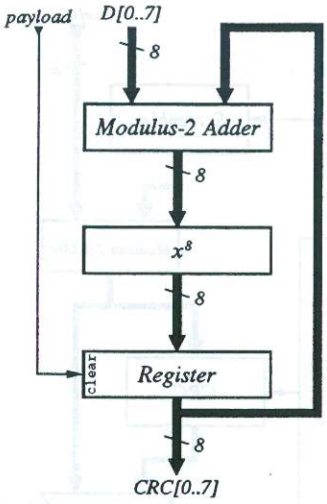

Fig. 5. Parallel *Header Error Control* computation

thus producing a smoother growth in complexity.

The process chosen for this design was **H-GaAs-III** from Vitesse Semiconductor Corp. [2]. This technology offers E/D transistors with $0.6\mu m$ minimum channel lengths. Enhancement transistors present nominal threshold voltage of 220mV while Depletion transistor is in the range of $-825mV$. Up to five metal levels are avalaible, and integration levels overpass a million devices, reaching VLSI levels of integration.

The design methodology used for implementation was *Ring Notation* [3] approach together with *Merged Logic* [4]. *Direct Coupled FET Logic*(DCFL) is preferred in most of the cases due to its simplicity and performance. Typical delays for DCFL logic gates are in the order of 50 to 100 ps with power consumptions between 200 and 300 μW. In those paths in which high load capacitance is encountered, *Source-follower Direct Coupled FET Logic* (SDCFL) is used. When high fanout must be driven *Super Buffer FET Logic* (SBFL) is preferred, taking in consideration the noise introduced by this logic family in the power lines.

A. Scrambler

The ATM cell stream is scrambled with a *distributed sample scrambler* [5], [6] which generates a pseudo-random sequence with a $2^{31}-1$ samples period. This is made by a modulus divider by $x^{30}+x^{28}+1$. In order to avoid the frequency involved in a serial scrambler ($2.5GHz$) a parallel scrambler was designed. This structure, shown in figure 4, generates eight bits per clock cycle. The full custom implementation occupies an area of $580\mu m \times 380\mu m$ with 794 devices, and a power consumption of $65mW$.

B. Header Error Control (HEC)

The fifth byte of the ATM cell —known as *Header Error Control* (HEC)— must be remainder of the modulus division of the first to fourth bytes by x^8+x^2+x+1. This HEC must be inserted by the transceiver and will be used to protect the integrity of the header of the cell

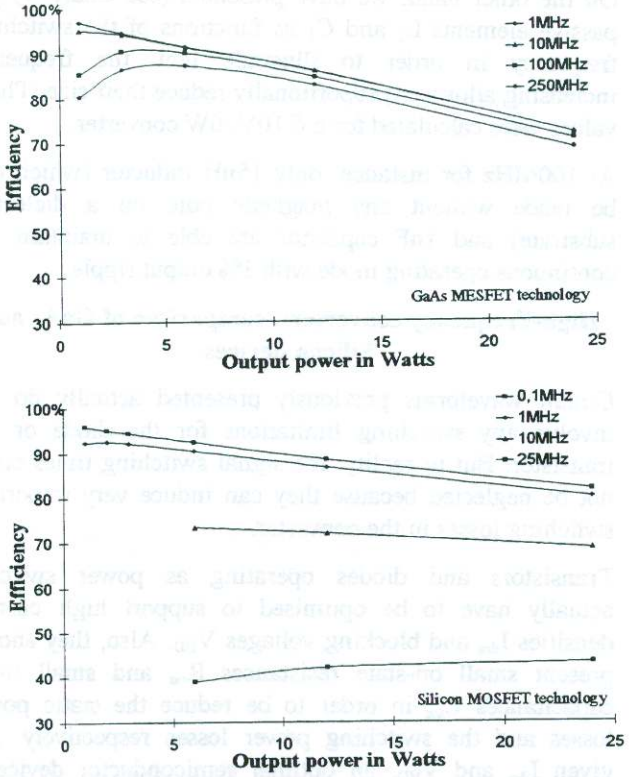

Fig. 3 : Evolutions of the power efficiency of GaAs MESFET's based (top chart) and Silicon MOSFET's based (bottom) boost configuration versus the output available power. (PSPICE simulation results).

Hybrid technology integration of a 100MHz Boost converter

We have already used this hybrid integration technique in a previous prototype using non optimised GaAs devices and operating at 100MHz with 1.4ns switching times [8]. As shown in Fig. 4 however, efficiency and output voltage evolutions versus the duty ratio suggest to use a faster gate driver in order to guarantee a higher but constant power efficiency and a wide output voltage range with respect to the duty ratio.

The prototype we propose in this paper (see Fig. 5) has been designed for a 100-MHz, 5:10V and 5W operating mode, using a MESFET based gate driver which can provide down to 500ps switching times. A GaAs Schottky barrier power rectifier, fabricated in the IEMN, has been optimised to support a 20V reverse voltage with 0.15Ω series resistance and 18pF zero-voltage capacitance. A hybrid square inductor has been designed with the two dimensional simulator (HP-MOMENTUM) and realised on a low dielectric constant substrate in order to reduce its parasitic capacitance. A commercial power MESFET (FLL120MK) which provides 5A and supports 15V has been used. We have also used progressive dc-decoupling capacitances which have been mounted close to the switching components.

A measured power efficiency of 76%, an output power level of 4W/8.8V for signal switching times of about 800ps have been obtained. Results obtained by simulation (see Fig. 6) show a good agreement with measurements and prove the validity of our device modelling.

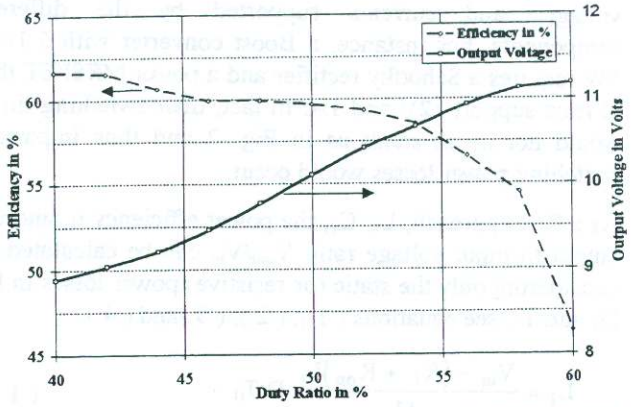

Fig. 4 : Measured Efficiency & Output Voltage for a 100MHz-6V/12V Square-Wave Boost Converter versus the Duty Ratio

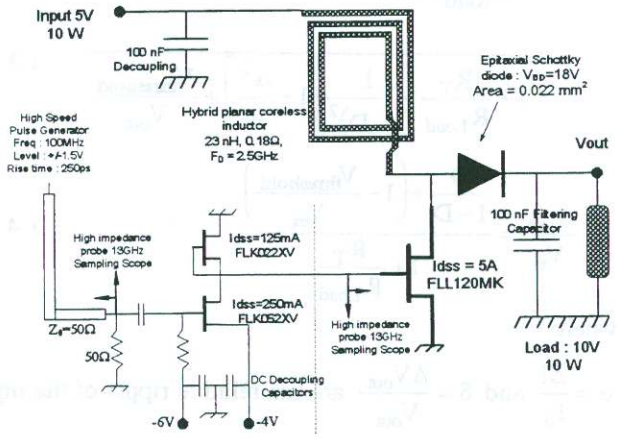

Fig. 5 : Hybrid technology prototype including a MESFET-based gate driver and using a coreless planar inductor and a Schottky barrier power rectifier.

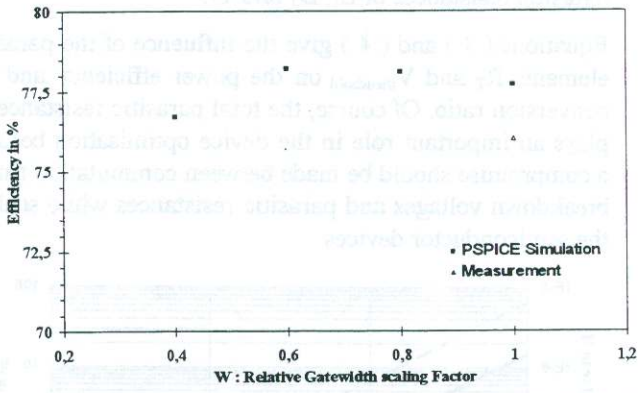

Fig. 6 : Simulated and measured power efficiency of a 5-10V 5W boost converter as a function of the gatewidth scaling factor. For I_{dss}=5A, W=1.

In contrast with the square-wave converter theory however, simulations show that decreasing the switching times (by reducing the gatewidth scaling of the power MESFET) do not considerably increase the power efficiency. In fact, transient analysis in which we consider all parasitic inductances in the hybrid technology converter, showed very important oscillations that induce additional power losses in the structure. A 13GHz sampling Scope has

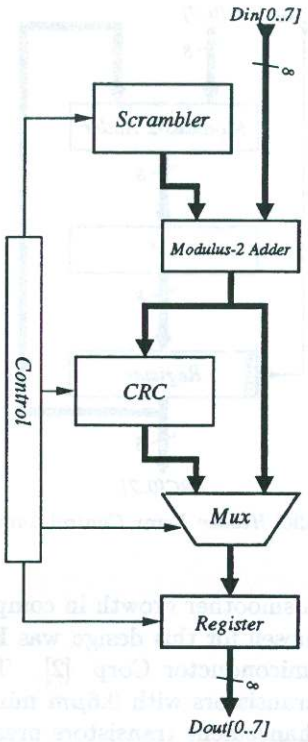

Fig. 6. *Transmission Convergence* block diagram

and for performing the cell delineation on the receiver side. Also a parallel architecture of this HEC computation must be designed allowing to compute eight bits per cycle and keeping a clock frequency of $311Mhz$. The structure of this unit is shown in Figure 5. This cell occupies an area of $600\mu m \times 200\mu m$ with 449 devices and a power consumption of $45mW$.

C. Transmission convergence

Figure 6 shows a simplified block diagram of the transmission convergence cell. The input data stream is scrambled with the scrambler through a modulus-2 adder. The HEC unit is always performing the HEC calculation. The control unit resets the HEC unit at the first byte of the cell. At the fifth cycle, this control unit inserts the output of the HEC unit into the data stream through the multiplexer.

The full layout of this control unit is shown in Figure 9. This cell occupies an area of $790\mu m \times 820\mu m$, with 1875 devices which means 2900 devices/mm^2 and a power consumption of $160mW$.

D. Discrambler

The discrambler used on this system is based on the scrambler. Its block diagram it's shown in figure 7. For a proper operation must be synchronized with the transmitter side scrambler so it has an additional logic for synchronization. The process of synchronization is based on a pair of samples of the internal state of the transmitter scrambler sent on each ATM cell. On the receiver, these samples are compared with the internal state of the discrambler. If differences were found, a correction pattern would be added to the internal state of

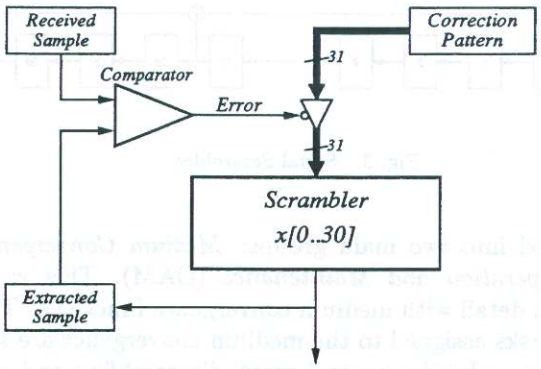

Fig. 7. Discrambler block diagram

the discrambler. If proper correction patterns are used, only 31 samples are required to synchronize the discrambler —that is to say 16 ATM cells—. The selection of the correction patterns is not a trivial matter. The I.432 recommendation gives the patterns for a serial discrambler, but this pattern should be modified for working with a parallel discrambler. This parallel implementation occupies an area of $680\mu m \times 480\mu m$.

E. Cell delineation

The process of cell delineation is driven by the HEC unit on the receiver. This unit has several differences with the HEC of the transmitter side. It has two modes of operation: *hunt* and *normal mode*.

On *normal mode*, it works just like the transmitter HEC. On *hunt mode*, this HEC unit searches a sequence of 40 bits that matches with a cell header (congruent with $x^8 + x^2 + x + 1$). This test should be done bit by bit. If this approach is implemented with a parallel structure with lower clock frequency, the complexity of

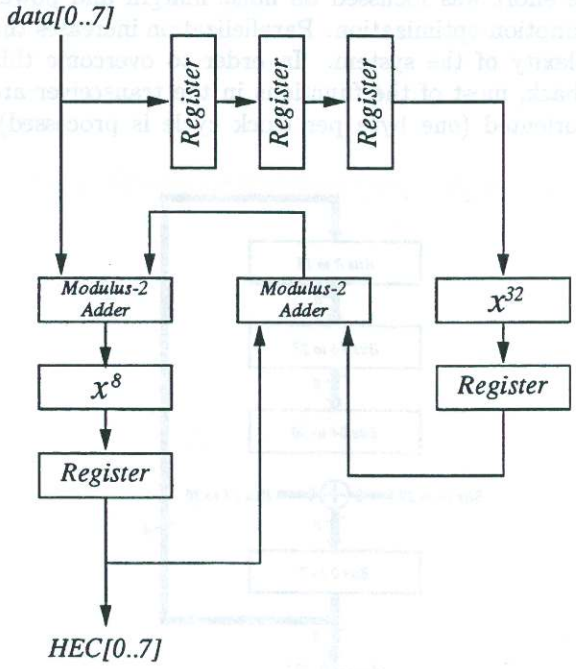

Fig. 8. Receiver *Header Error Control* computation for cell delineation

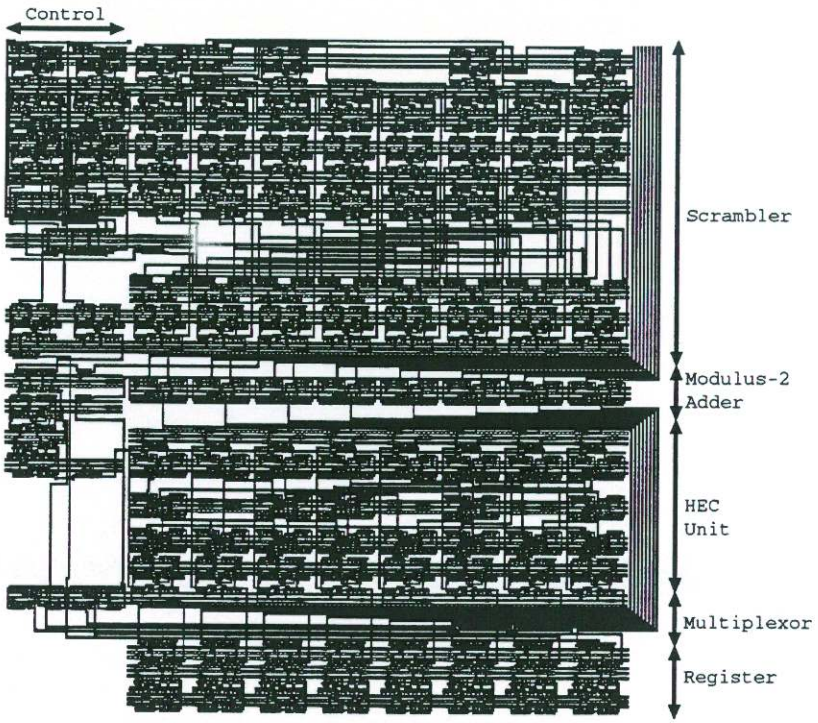

Fig. 9. *Transmission Convergence* layout

the system grows dramatically. For this reason, our implementation performs a byte by byte test, which means that the byte should be aligned. This byte alignment should be perform by a external unit which shifts one bit if a header weren't found after a number of bytes. The structure of this unit is shown of Figure 8.

Conclusions

The solutions for high speed systems not only rely on new technologies but also on the use of efficient architectures. With parallelization, lower clock frecuencies can be achieved making feasible the systems implementation. On the other hand, parallelization denotes higher complexity of the systems which means more area as well as power consumption. Gallium Arsenide technology allows design with low power consumption, we can get clock frequencies that are beyond the limit of Silicon technology.

This article has shown some aspects in the implementation of a $2.5Gb/s$ ATM transceiver. An estimation for the power consumption of this structure gives a value below 5W for an internal operating frequency of 311MHz. Transistor count is around 30.000. As long as we know, the resulting circuit achieves performances not obtained in any other CMOS related circuit. Studies for a $10Gb/s$ ATM have been started in our group not only using architectural strategies (in which with a 32 bits parallel processing a 311MHz clock frequency can be kept), but also exploring other technologies such as HEMTs.

Acknowledgments

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