High-Performance of InGaAs/GaAs Doped-Channel Heterostructure Field-Effect Transistor (HFET) Prepared by MOCVD

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Abstract

In this paper, we will investigate a metal-insulator-semiconductor (MIS) like InGaAs/GaAs doped-channel structure both in theoretical analysis and experiment. First, a charge control model is employed to simulate the basic electronic properties of the doped-channel field-effect transistor (FET). Then, a practical device is fabricated and processed. From the results, we can find that the device shows good transistor characteristics. A high breakdown voltage of 17.4 V, a maximum drain saturation current of 930 mA/mm, a maximum transconductance of 235 mS/mm, and a very broad gate voltage swing larger than 3V with the transconductance higher than 200mS/mm are obtained for a $2\times100\ \mu m^2$ gate-dimension FET. From the comparison, we find that the experiments are in good agreement with the theoretical simulations. The performances provide a promise of the proposed device to be a good candidate for practical circuit applications.

I. Introduction

Over the past years, rapid progress in epitaxial growth technologies, such as molecular beam epitaxy (MBE) and metal organic chemical-vapor deposition (MOCVD), have greatly contributed to the realization of new high-performance devices. For device has been applied in high-power, high-speed systems, there are several basic requirements such as high current capability, high breakdown voltage, good current linearity, and high cutoff frequency. To satisfy these requirement, Metal-semiconductor field-effect transistor (MESFET)[1-2] and high electron mobility transistor (HEMT)[3] have been thought to be particularly promising devices. However, there are several disadvantages in these devices[4]. Compared to conventional HEMT`s and MESFET`s, doped-channel MIS-Like FET`S (DMT`s) have been proposed and fabricated [5-6]. The main advantages of DMT`s are: (i)two operation modes, (ii)high breakdown voltages, (iii)good current linearity and short-channel effect alleviation and (iv)large forward gate voltage tolerance. In this paper, we employ an improved analytical model of heterostructure field effect transistor`s (HFET`s) [7] to describe and simulate the performances of the studied DMT device. This allows us to obtain an excellent agreement with the experimental results. The detailed properties and performances for normally on DMT are investigated. Experimental results have demonstrated that DMT`s possess unique properties and pronounced potentiality for high speed and high-frequency, high power device applications.

II. Analytical Model and Simulation

In this section, we will discuss the current-voltage (I-V) characteristics both in intrinsic and extrinsic devices with an analytical model[7].

This analytical model is based on several assumptions. First of all, we neglect the gate current. This assumption makes this model much simpler but limit its validity to voltage below the turn-on voltage for the gate current. The second assumption is the validity of the Gradual Channel Approximation (GCA) with constant gate to channel capacitance in the portion of channel where electron velocity is smaller than the electron saturation velocity V_{sat} [8]. The third assumption is that the relation between the electric field and the electron velocity is given by a modified two-piece approximation. Finally,

we assume that once the velocity saturation occurs near the drain edge of the channel, channel length modulation is responsible for further increase in the drain current. Such an approach gives a lower bound for the drain conductance in the saturation region.

For intrinsic case, the drain-to-source current can be expressed as [7,9,10]:

$$I_{DSL} \equiv \frac{1}{G_M}\frac{2V_{GT}V_{DS}-V_{DS}^2}{V_{DS}+2V_L}, \qquad (1)$$

in linear region and Eq.(2) in the saturation region. Where $G_M=1/wC_0v_s$, C_0 is the gate-to-channel capacitance, $V_{GT}= V_{GS}-V_T$ is the effective gate bias for intrinsic device, V_T is the threshold voltage, and $V_L=E_sL$, L is the effective electric gate length, $V_b=E_sb, b=\sqrt{t\cdot(d+\Delta d)}$, t is the effective thickness of the two-dimension electron gas in the saturation region, d is the GaAs layer thickness, Δd is the correction factor for gate-to-channel capacitance and I_{DSAT}, V_{DSAT} are the saturation current and voltage at saturation point in linear region.

For extrinsic device, the voltage drop across the source and drain resistances no longer are treated as a small perturbation to the external bias. In this section, the model is extended to describe the extrinsic I-V characteristics affected by parasitic source and drain resistance.

The relationship between extrinsic and intrinsic voltage can be easily obtained :

$$V_{GS} = V_{gs} - I_{DSL}R_s \qquad (3)$$

$$V_{DS} = V_{ds} - I_{DSS}(R_s + R_D), \qquad (4)$$

where V_{gs}, V_{ds} are extrinsic gate-to-source and drain-to-source voltage, R_s, R_D are source and drain resistance . Substituting Eqs. (3), (4) into Eq.(1),(2), we can obtain the drain-source current in linear and saturation regions for extrinsic case.

Figure 1 shows the simulated extrinsic ($R_S=R_D=20\Omega$) I-V characteristics. The saturation current at $V_{GS}=0$ is 48 mA. The simulated values of extrinsic transconductance g_m and output conductance g_{ds} versus drain-source voltage are illustrated by the dashed lines in Fig.2. The theoretical simulations of the relationship between the extrinsic transconductance g_m, drain saturation current I_{DSAT} and gate-source voltage V_{GS} are shown by the dashed lines in Fig.3. From the simulated results, we can find that the MIS-Like FET have good performances in large signal and high speed applications.

III. Devices Process and Experimental Results

A practical DMT device was prepared by metal organic chemical vapor deposition (MOCVD) technique on a (100)-oriented semi-insulating GaAs substrate. The structure contained a 0.5μm undoped GaAs buffer layer, a 120Å n^+-$In_{0.2}Ga_{0.8}As$ ($n^+=4\times10^{18}$ cm^{-3}) channel, a 500Å n^-GaAs ($n^-=5\times10^{16}cm^{-3}$) Schottky contact layer, and a 300Å n^+-GaAs ($n^+=3\times10^{18}cm^{-3}$) cap layer. A cross-section view of the device is depicted in Fig.4. After exitaxial growth, wet chemical etching, vacuum evaporation, and lift-off techniques were used to fabricate the device. First, the mesa areas were defined to isolate devices. Then, source and drain ohmic contacts were formed by alloying evaporated Au-Ge-Ni metals at 450 °C for 30 second. The wafer was etched in a $NH_4OH:H_2O_2:H_2O$ (3:5:100) solution to remove the n^+-GaAs cap layer within the gate region. Finally, the gate Schottky contacts were formed by lifting off evaporated. The studied gate dimension is $2\times100\mu m^2$.

The I-V characteristics of the experimental results is shown by the solid lines in Fig.1. The applied gate-to-source voltage is increased with 0.5 V/step and the maximum gate-to-source voltage can reach +2.5V. It is clear that the drain saturation current I_{dsat} increase linearly with the increasing the V_{gs}, and the maximum value of I_{dsat} reaches 98mA. This large current can enhance the device driving ability in circuit application. The observed threshold voltage is about -2.9V. Figure 3 has shown the variations

$$I_{DSS} = I_{DSAT}\left\{1+\frac{2V_b}{V_{GT}+2V_L}\ln\left[1+\frac{(V_{DS}-V_{DSAT})}{8V_b(V_{GT}+V_L)}\cdot\frac{(V_{GT}+2V_L)^2}{V_L}\right]\right\} \qquad (2)$$

of drain-source saturation current I_{dsat}, and transconductance g_m with the applied gate voltage V_{gs}. The I_{dsat} is varied approximately linearly with V_{gs}. The maximum transconductance g_m is 235 mS/mm. A large V_{gs} swing (>3V) with g_m higher than 180 mS/mm is obtained. The large V_{gs} swing can increase the application potentiality for large input signal circuit. The transconductance g_m and output conductance versus applied drain-source voltage are shown by the solid lines in Fig.2. The gate-source voltage V_{gs} is kept at 0.25V, and the series source and drain resistance, Rs, R_D are 20 Ω. It shows that the transconductance g_m is increased with the drain-source voltage V_{DS} within the regime of $V_{DS} \leq 3.5V$. When $V_{DS} \geq 3.5V$, the g_m keeps at a constant value of about 230 mS/mm. On the other hand ,the output conductance g_{ds} shows a decreased characteristics when the V_{ds} is increased

IV. Comparisons between Theoretical Analyses and Experimental Results

The comparisons between theoretical simulations and experimental results are shown in Fig. 1, 2, and 3. Generally, the theoretical simulations show good agreement with experimental results. For the I-V characteristics, as shown in Fig.1, the simulated values are somewhat higher than the experimental results in the linear regime. In addition, the simulated curves show the more sharp variation of I-V characteristics near the beginning point of saturation regime. The variations of transconductance and output conductance with the applied drain-source voltage are illustrated in Fig.2. It is known that a relatively large deviations between theoretical simulations and experimental results are found. The season is not clearly understood. Perhaps, this is caused by the neglect of gate current in the theoretical assumption. The influence of gate-source voltage on the device properties is revealed in Fig.3. Again, the neglect of gate leakage current causes the theoretical value of drain saturation current are slight higher than those of experimental results especially at higher V_{GS} regime. On the other hand, in the transconductance variation profile, the g_m values exhibit relatively large deviation at $|V_{GS}| > 1.5$ V. In summary, due to the good consistence between simulated and experimental values over the main operation regime, the proposed theoretical model and analyses are suited for describing the DMT's characteristics.

V. Conclusion

The continuous HFET model has been used to simulate the MIS like InGaAs/GaAs doped channel structure. From the results of simulation, we can see that the MIS-like InGaAs/GaAs doped channel structure has good electronic properties. In addition, a practical device is fabricated and processed. From the comparison, we can find that experiment results are in good agreement with the theoretical simulations.

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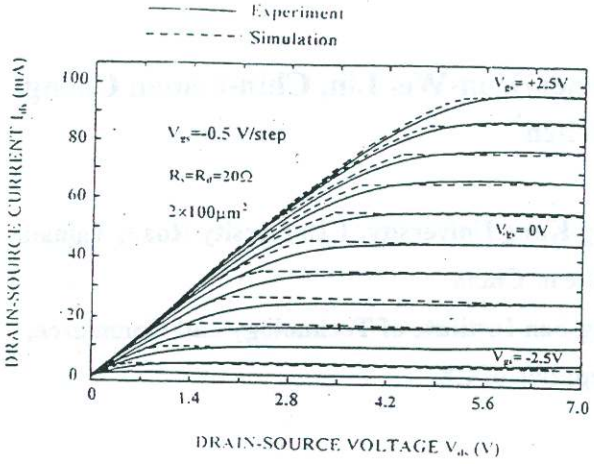

Fig.1 The simulated and experimental I-V characteristics of an extrinsic device with R_S=R_D=20Ω.

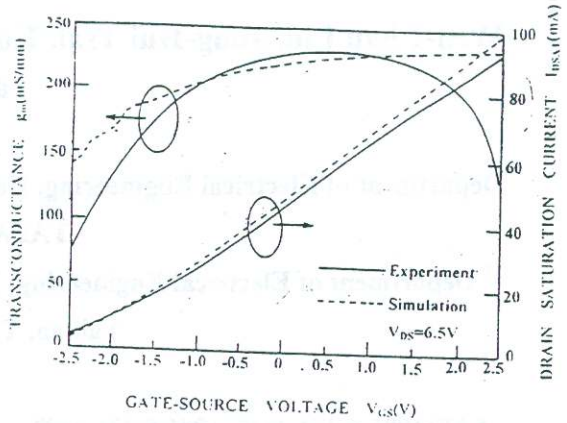

Fig.3 The relationship between the transconductance, drain saturation current and the applied gate-source voltage.

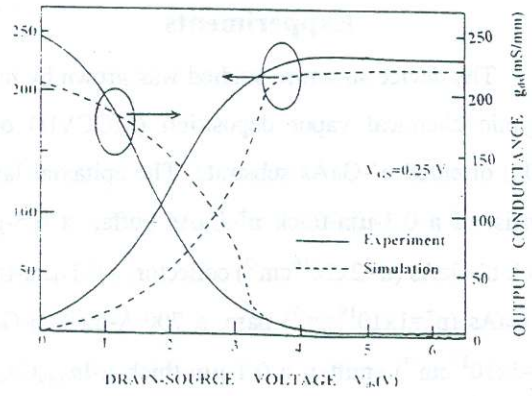

Fig.2 The relationship between the transconductance, output conductance and the applied drain-source voltage.

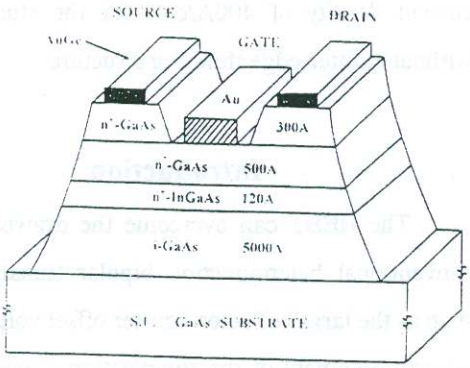

Fig.4 Schematic cross section of the studied device.