III-V complementary HIGFET technology for low power microwave and high speed/low power digital integrated circuits

Hussein FAWAZ, Jean-François THIERY, Nuyen LINH*, Francis MOLLOT, Jean-Claude PESANT, Marc FRANCOIS, Michel MULLER, Elisabeth DELOS and Georges SALMER.

Institut d'Electronique et de Microélectronique du Nord, UMR CNRS 9929, Université des Sciences et Technologies de Lille, 59652 Villeneuve d'Ascq Cedex, FRANCE.

**PICOGOGA*, 5, Rue de la Réunion, Z.A. de Courtaboeuf, 91940, Les Ulis, FRANCE.

Abstract

A self aligned complementary HIGFET technology has been developed for high speed/low power digital and microwave analog applications. The process uses 9 lithographic steps including two level of interconnect metal. Typical transconductances of 290 mS/mm and 65 mS/mm are acheived on 1μm gate length N and P-channel devices respectively. 0.5 μm gate length N-HIGFET show a Ft of 40 GHz and an intrinsic Fc of 80 GHz. These devices show promise for incorporation in complementary digital, MMIC and RF power circuits.

Introduction

Recently, low voltage operation very high speed transistors with ultra-low power dissipation are strongly required in developing advanced high performance integrated circuits for portable systems. Pseudomorphic AlGaAs/InGaAs/GaAs Heterostructure Insulator Gate Field Effect Transistors (HIGFET's) are attractive devices for application to high speed/low power IC's due to their potential advantages over Si CMOS circuits of equivalent gate dimensions [1], [2], [3], i.e. superior speed performance, lower threshold voltage sensitivity, constant speed versus temperature and process simplicity. Moreover, the HIGFET device can be looked as a serious challenger for power applications for low power wireless telecom terminals. In fact, comparing to other III-V devices, it benefits at the same time from an excellent gain linearity and a high power density both using a single positive power supply. A complementary HIGFET (C-HIGFET) process has been developped in IEMN intended for high speed/low power digital IC's and low power microwave / low cost analog device. In this paper, we present the C-HIGFET process and device results for both digital and analog applications.

Device strucutre

Two device strucutres are used:

Shown in Figure 1 is the HIGFET device structure for complementary high speed/low power digital IC's. The layers consist of MBE grown GaAs buffer 2000Å, followed by a silicon delta doping of sheet concentration $3.3.10^{11}$ cm^{-2}, an undoped GaAs spacer layer 30 Å, undoped $In_{0.2}GaAs$ channel layer of thickness 150 Å, undoped $Al_{0.75}GaAs$ 250 Å thick, capped with 100 Å of undoped GaAs layer. The use of high AlAs mole fraction in the AlGaAs layer has been optimized in order to reduce the gate leakage currents of both N and P channel HIGFET [4]. This current is essentially due to the thermionic emission of carriers from the InGaAs channel over the AlGaAs barrier. It was demonstrated [5], that the gate leakage current is reduced when the bandgap dicontinuities are increased. The conduction band offset ΔEc of AlGaAs with respect to InGaAs increases monotonically up to an AlAs mole fraction of approximately 45 %. For AlGaAs barriers with higher AlAs mole fractions, ΔEc decreases slightly due to the effect of indirect transition to the X valley [6], [7]. The valence band offset ΔEv on the other hand, increase monotonically for all AlGaAs composition. Previous works [4] have shown that a composition of 75 % of AlAs mole fraction is the most appropriate choice in order to enhance both band discontinuities for complementary structures.

For analog applications in which only N-HIGFET devices are used, the epitaxial schema shown in Figure 2 is more suitable. The main difference between the two structures is the reduction of the Al rate from 75 % to 40 % in order to minimize the gate leakage current.

The silicon delta doping was used for threshold voltage adjustment of the N and P channel devices [8].

Device fabrication

A schematic cross-section of the self-aligned ion-implanted C-HIGFET process is shown on Fig. 2. 4000 Å of WSi was first sputter deposited. Next, e-beam lithography is used to write gate structures with lengths between 0.2μm and 1μm using AZ PN 114 resist. The WSi layer is then patterned using reactive ion etching. N-channel and P-channel source and drain lithography and implants are sequentially performed. The implants are self-aligned to the refractory gates. The N-channel source and drain implant specie is Si with 60 KeV at a dose $4.10^{13}cm^{-2}$. In order to reduce the contact resistance of the source and drain ohmic contacts, a N^{++} implantation was performed after a second implant lithography. The N^{++} implantation consists of a 60 KeV Si at a dose of $10^{14}cm^{-2}$. The P-channel source and drain regions are co-implanted with 80 keV P and 15 keV Be at

a dose $10^{14}cm^{-2}$. Likewise the N-channel, P^{++} implantation was also performed. It consists of a co-implant of 100KeV P and 20KeV Be at a dose of $10^{15}cm^{-2}$. The self-aligning implant is activated using 850°C, 10 seconds, rapid thermal anneal. The resulting N^{+} and N^{++} sheet resistivities were 280Ω/sq and 145Ω/sq respectively, and P^{+} and P^{++} sheet resistivities were 700Ω/sq and 170Ω/sq respectively. AuGe/Ni/Au and Au/Mn/Ni/Au ohmic contacts are then defined for N-channel and P-channel devices respectively. The contact resistance was typically 0.07-0.1Ω.mm for both N-channel and P-channel and contacts were found stable to temperature as high as 450°C. Ti/Au is used for interconnexion and devices are finally passivated with Si_3N_4.

Device performance

Digital

For high speed / low power operation, N and P channel devices has been realized using the epitaxial structure described in the Figure 1. Typical I-V characteristics of $2x20x1\mu m^2$ N and P-channel devices are shown in Fig. 4 and 5. The device has very good pinch-off characteristics and output conductances. The threshold voltage are near 0.55V for N-HIGFET and -0.4V for P-HIGFET. The N-channel device extrinsic transconductance is 290 mS/mm and the P-channel device near 65 mS/mm. Standard deviations of the threshold voltage of the devices over 2-inch wafers was 35mV for the N-HIGFET and 26mV for the P-HIGFET. Fig. 6 and 7 show the distribution of the threshold voltage for the N-HIGFET and the P-HIGFET respectively. The small variation of threshold voltage is characteristic of HIGFET's where the threshold voltage depends only on the N-and P-Schottky barrier heights, the conduction and valence band discontinuities of the $Al_{0.75}GaAs/InGaAs$, the sheet concentration of the silicon delta doping plan and the distance between the silicon delta doping and the metal/semiconductor interface which are controlled to better than 1 % by the MBE process. The subthreshold characteristics of a N and P-channel devices are shown in Figure 8, where subthreshold slope of 80 mV/dec and off current less than 0.3 nA/μm are obtained for the N-HIGFET and subthreshold slope of 320 mV/dec and off current of 67.5 nA/μm are obtained for the P-HIGFET. The relative important value of the subthreshold leakage current of P-HIGFET's is due to the implant straggle effects, stress enhanced diffusion of the P-type dopant under the gate and the drain induced barrier lowering [9]. The gate turn-on voltage defined as the gate voltage resulting in a leakage of $1\mu A/\mu m^2$ current at Vds = 0, is 1.4 V for the N-HIGFET and -2.2 V for the P-HIGFET.

The AC performance of the N and P-channel devices was evaluated using microwave S-parameter measurments. Maximum F_t for the N-HIGFET was 24 GHz with a F_{max} of 39 GHz and those for P-HIGFET was 5GHz for both F_t and F_{max}. Figure 9 shows the F_t and F_{max} as a fuction of the gate bias for the N-HIGFET. The microwave results are comparable to HEMT's of similar gate length. Typical N and P-channel devices parameters are given in Table 1.

Analog

N-HIGFET with 1 and 0.5 μm gate length were fabricated using the epitaxial structure shown in Figure 2. DC transfert characteristics are shown for both devices in Figure 10 - 11. Device performances are also summarized in table 2. The $2*50*1\ \mu m^2$ N-HIGFET shows a maximum transconductance (gm) of 360 mS/mm, a maximum drain current (Ids) of 320 mA/mm and a turn-on voltage (Vto) of 1.62 V. Likwise, the $2*50*0.5\ \mu m^2$ N-HIGFET shows a maximum gm of 520 mS/mm, an Ids of 480 mA/mm and a Vto of 1.35 V. The 0.5 μm gate length N-HIGFET has not been fully optimized, as it shows shift of the threshold voltage and increase of the gate leakage current due to an additionnal leakage by the edge of the gate. On wafer measurements from DC to 40 GHz gave a maximum Ft of 24 GHz for the $2*50\ 1\ \mu m^2$ N-HIGFET and a maximum Ft of 40 GHz for the $2*50*0.5\ \mu m^2$ device. Further improvement in the microwave performance of the submicron devices are expected by optimizing the source and drain implant conditions and the gate resistance. Optimized devices for use as a power amplifier for a low power supply are being designed.

Conclusion

We have developed a complementary HIGFET process which is well suited for high speed/low power digital and microwave analog applications. N and P-channel devices have demonstrated excellent performances at low power supply.

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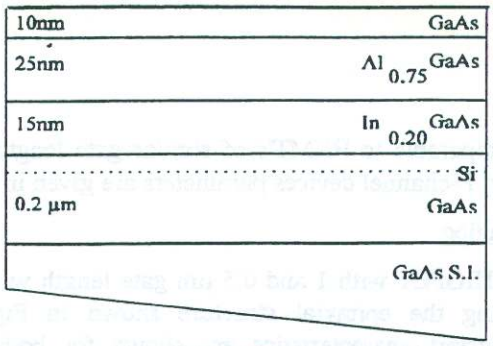

Fig. 1 : Cross-section of HIGFET epitaxy for Al rate x=0.75.

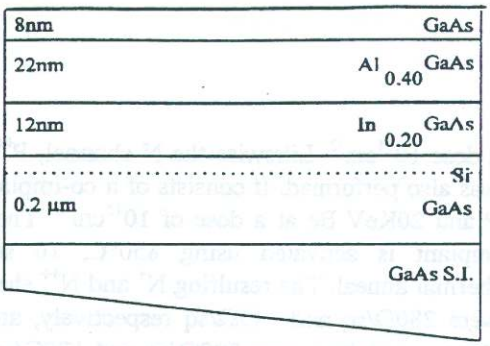

Fig. 2 : Cross-section of HIGFET epitaxy for Al rate x=0.4.

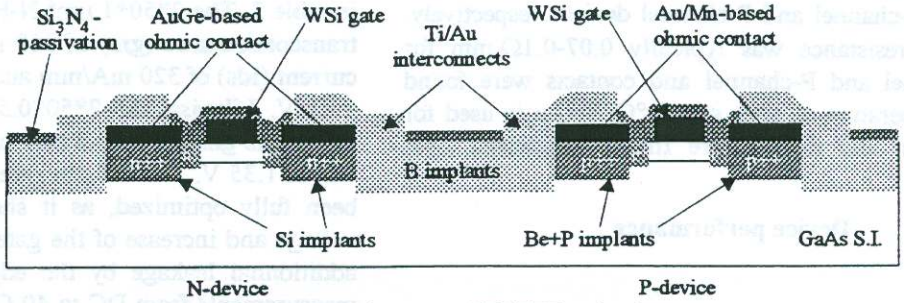

Fig. 3 : Complementary HIGFET technology

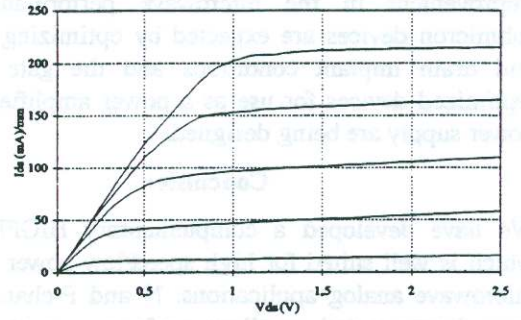

Fig. 4 : Id-Vd measurement of 1µm-N-HIGFET (x=0.75). Vgs max = 1.6 V. Step Vgs = 0.2 V.

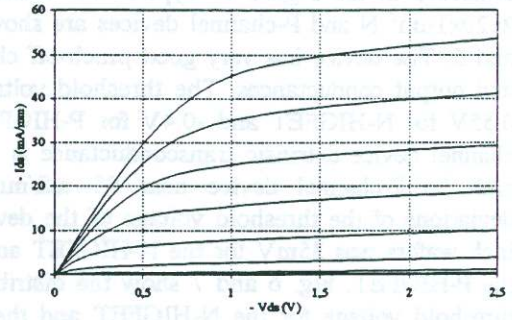

Fig. 5 : Id-Vd measurement of 1µm-P-HIGFET (x=0.75). Vgs min = -1.6 V. Step Vgs = 0.2 V.

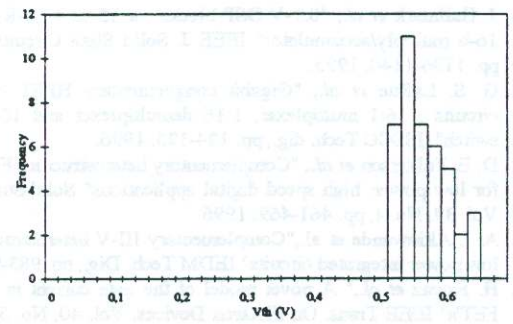

Fig. 6 : Threshold voltage distribution of 1µm-N-HIGFET. Standard deviation is 0.035 V.

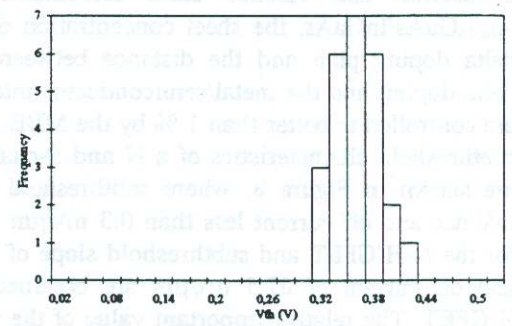

Fig. 7 : Threshold voltage distribution of 1µm-P-HIGFET. Standard deviation is 0.026 V.

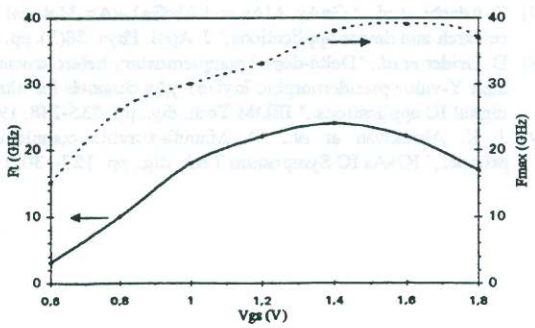

Fig. 8 : Ft (solid line) and Fmax (dashed line) of 1µm-N-HIGFET (x = 0.75) as a function of gate voltage.

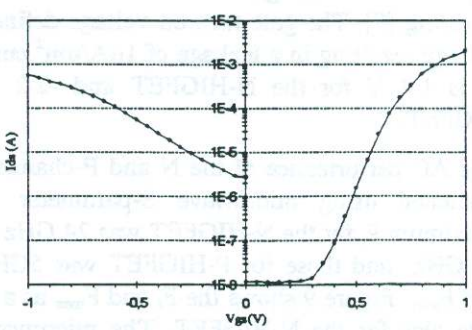

Fig. 9 : Subthreshold Ids caracteristics for 1µm N- and P- HIGFET. Drain voltage is +/- 1.5 V.

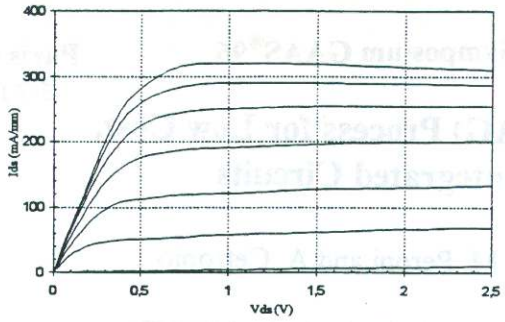

Fig. 10 : Id-Vd measurement of 1µm-N-HIGFET (x=0.4). Vgs max = 2.0 V. Step Vgs = 0.2 V.

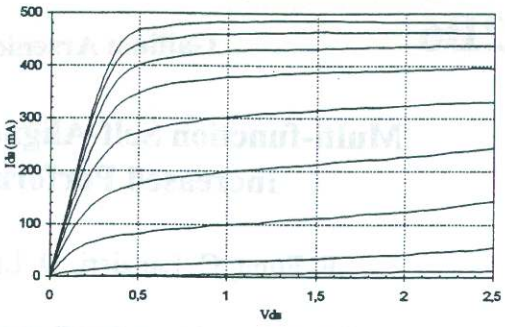

Fig. 11 : Id-Vd measurement of 0.5µm-N-HIGFET (x=0.4). Vgs max = 2.0 V. Step Vgs = 0.2 V.

	N-device	P-device
L (µm)	1	1
W (µm)	2*20	2*20
Idss (1.5V) (mA/mm)	190	50
Gm (mS/mm)	290	65
Vth (V)	0.55	-0.40
Beta (mA/mm^2)	340	48
Vto (V)	1.4	2.2
S (mV/dec)	80	320
F_T (GHz)	24	5
Fmax (GHz)	39	5

Table 1 : N- and P- device HIGFET parameters (x=0.75).

L (µm)	1	0.5
W (µm)	2*50	2*50
Idss (2.0V) (mA/mm)	320	480
Gm (mS/mm)	360	520
Vth (V)	0.70	0.50
Beta (mA/mm^2)	470	610
Vto (V)	1.62	1.35
Ns (cm^{-2})	2.6×10^{12}	2.1×10^{12}
µ (cm^2/Vs)	4800	4700
F_T (GHz)	24	40
F_C (GHz)	30	75
Rs (Ω.mm)	0.25	0.15

Table 2 : 1µm and 0.5µm N- device HIGFET parameters (x=0.4).