Multi-function Self-Aligned Gate (MSAG) Process for Low Cost, Increased Performance GaAs Integrated Circuits

F. Fumi, C. Lanzieri, D. Lupano, G. Negri, M. Peroni and A. Cetronio

Finmeccanica Centre for Microelectronics and Optoelectronics Technologies (CETME)
Via Tiburtina, 00131 Roma, ITALY

Abstract

We report on the realisation of an original SAGFET technology, presenting d.c. and r.f. measurements on discrete devices as a demonstration of the validity of said technology. Even though at an initial stage, the low-noise, control and power devices, simultaneously fabricated on the same wafer, are comparable with the more mature recessed-gate technology, yielding NF better than 2 dB and P_{out} better than 500 mW/mm at 12 GHz. As an example of the potentiality of this technology a prototype Tx/Rx chip is also presented.

Introduction

Self-alignment of the n^+ implantation in the drain and source regions using the gate as a mask gives low access resistance to the channel of the intrinsic FET, with benefits in d.c. and r.f. performance [1 , 2 , 3], without the need of critical photolithography. Moreover, the planarity of the process presents higher yields and better uniformity with respect to the more conventional recessed-gate process. These advantages make economically feasible the realisation of multi-functional MMIC's with low-level, high-power, and control devices integrated on the same chip, to produce for example a single-chip Tx/Rx circuit.

Several possible technological approaches for self-aligned gate FET's are reported in literature, most of which are more or less refined versions of two main classes of processes: "low temperature", and "high temperature" gate metallization [4]. The low temperature approach employs a dielectric "dummy gate" to mask the n^+ implantation, replaced by the gate metal only after annealing by means of a complex resist planarization and dielectric etch sequence [5]. The high temperature process employs a refractory metal or alloy to define the gate geometry before the n^+ implantation, and side-wall dielectric spacers are used to increase the distance between the n^+ region and the gate contact [6].

In the approach reported below we have accomplished a technology which eliminates the critical steps of the above mentioned processes; i.e. no "dummy gate" and no "side-wall" spacer technique. To achieve this, the realization of a

Tab. 1. Channel implantation conditions for multi-function devices. In each case the $^{12}C^+$ implantation energy is 300 keV.

	$^{28}Si^+$ IMPLANT		$^{12}C^+$ IMPLANT
	Energy (keV)	Dose (cm^{-2})	Dose (cm^{-2})
Low-Noise	120	1×10^{13}	4×10^{12}
Control	135	9×10^{12}	3×10^{12}
Power	150	8×10^{12}	2×10^{12}

WN_x/Au metallization scheme, stable up to 900°C on GaAs, has been a key technological step. In particular, in said approach, a gold cap is used for the self-aligned gate mask of the n^+ implantation, made through a layer of WN_x that acts both as the encapsulating layer for post-implant annealing and as the gate Schottky contact, and a highly selective, low damage WN_x plasma etch process for producing the necessary "T-shaped" gate structure, with controllable footprint lenght in the range 1.0 to 0.5 µm.

Experimental

The active channels of the MESFET devices were either realised by ion-implantation or by molecular beam epitaxy. In the former case selective implantation of $^{28}Si^+$ for the n-type layer and $^{12}C^+$ for the p-type buried layer was used, with profiles optimized to device performance (see Tab. 1) via appropriate computer simulations of device parameters, having as objective high g_m/C_{GS} for low-level devices and high breakdown voltages for power devices. For the MBE grown devices a similar approach was used except that in this case the electron confinement under the gate was achieved by GaAs/AlGaAs superlattice buffer layer.

The implantated layers were activated by rapid thermal annealing (RTA) in the presence of a sputter-deposited Si_3N_4, which was removed with the uppermost layer of GaAs after annealing. Said procedure is equivalent to a through-nitride implantation [6], but with better reproducibility of active device performance. Infact, we have assessed that the doping activation was not constant in the first few hundreds Ångstroms of the GaAs surface

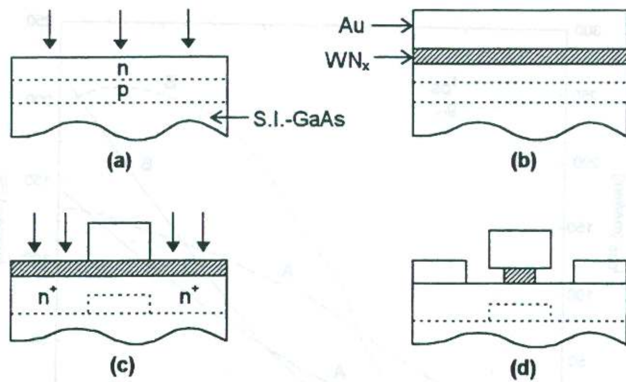

Fig. 1. SAGFET processing steps. (a): channel n and p implantations and annealing (not applied to epitaxial substrates); (b): WN_x/Au gate metallization; (c): gate definition, self-aligned n^+ implantation and annealing; (d): WN_x RIE, ohmic contacts formation, and T-gate plasma etching.

for the latter condition.

Having determined the doped channel region, the following technological steps (schematically illustrated in Fig. 1) were exactly the same both for epitaxial and implanted devices. A thin WN_x and a thick Au film were deposited on the entire wafer and the gate geometry was subsequently defined on the Au cap by ion-milling. The n^+ implantation of $^{28}Si^+$ and RTA followed, and then WN_x was removed by anisotropic reactive-ion etching (RIE) in a CF_4+O_2 gas mixture. After the formation of alloyed Au/Ge/Ni ohmic contacts, an isotropic plasma etch in a CF_4+O_2 gas mixture was made to create the T-shaped gate structure, with subsequent C_{GS} measurements and control to realise the desired footprint.

After gate and ohmic contact definition, devices and multi-function MMIC's were completed via a standard technology composed of: plasma enhanced CVD Si_3N_4 passivation; capacitors with sputtered Si_3N_4 dielectric; Ni/Cr or ion-implanted resistors; Ti/Pt/Au and electroplated gold with air-bridges for interconnections.

Results and discussion

A. Gate metallization and n^+ implantation and annealing

Annealing of the n^+ implantation requires a very stable gate metallization. Pure W has been excluded because of its high reactivity with oxygen [7], and instead a reactively sputtered WN_x alloy has been used. The sputter deposition conditions were optimized to minimize the stress of the WN_x film. Said stress was found to be compressive at 1.25×10^{10} dyn/cm^2 for the as-deposited film, and reduced to 8×10^9 dyn/cm^2 after thermal treatment at 500°C for 180 s because of crystallization [8]. Said film configuration prevents Ga and As out-diffusion during the high temperature annealing, as confirmed by X-ray photoemission spectroscopy (XPS) and secondary-ion mass

Tab. 2. Results of Van Der Pauw measurements of sheet resistance (R_{SH}) and carrier concetration (n_{SH}) on different n^+ layers, implantated through a WN_x film with energy E_{IMPL} and dose 2×10^{13} cm^{-2}, and annealed for 10 s at temperature T_{ANN}. Set A is different in having a thicker WN_x than set B.

Set	E_{IMPL} (keV)	T_{ANN} (°C)	R_{SH} (Ohm/□)	n_{SH} (cm^{-2})
A	300	800	325	5.50×10^{12}
	300	900	309	4.96×10^{12}
	250	800	561	2.90×10^{12}
	250	900	550	2.76×10^{12}
B	300	800	165	1.13×10^{13}
	300	900	154	1.06×10^{13}
	250	800	224	8.80×10^{12}
	250	900	226	8.74×10^{12}

spectroscopy (SIMS) profiles, which indicated no change in the atomic concentrations at the WN_x/GaAs interface after annealing up to 900°C. Stabilization of the WN_x film by means of an intermediate temperature cycle prior to the high temperature annealing step was necessary to increase the reliability of the Au/WN_x gate structure.

The capping and Schottky contact properties of the WN_x film were evaluated in the 800-900°C temperature range by means of C-V and I-V diode characteristics. From C-V measurements it is apparent that above 800°C there is little change in the carrier concentration profile and as such a virtually constant activation efficiency of approximately 80% is obtained. As shown in Tab. 2, what is more important in determining the overall sheet resistance of the n^+ layer are implantation energy and film thickness. In particular, for a constant annealing temperature and implantation energy, a factor of two reduction in sheet resistance is possible by optimizing the WN_x film thickness. From the diode I-V characteristics we estimated the Schottky barrier height to be approximately 0.7 eV with a corresponding ideality factor of 1.2, independent of the annealing temperature in the range 800 to 900°C.

B. Power devices

The d.c. performance of power SAGFET's is found to be comparable to those of the recessed-gate MESFET family with the same channel doping profile: i.e. saturation current $I_{DSS} \approx 280$ mA/mm $g_m \approx 80$ mS/mm (measured at $V_{GS} = 0$ and $V_{DS} = 3$ V); pinch-off voltage $V_P \approx 4.5$ V (defined at $I_{DS} = 1$ mA/mm); $C_{GS} \approx 1.5$ pF/mm. The only difference was found to be the lower g_m of the SAGFET device near pich-off, due to the lateral tails of the n^+ implantation from the drain and source regions (referred as "short-channel effect").

The corresponding r.f. performance is illustrated by the

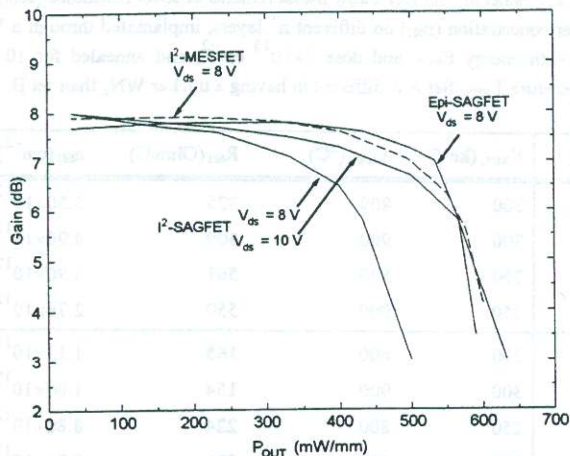

Fig. 2. Gain as a function of output power for: a) ion-implanted SAGFET (V_{DS} = 8 V and 10 V), b) epitaxial SAGFET, and c) standard ion-implanted recessed-gate MESFET.

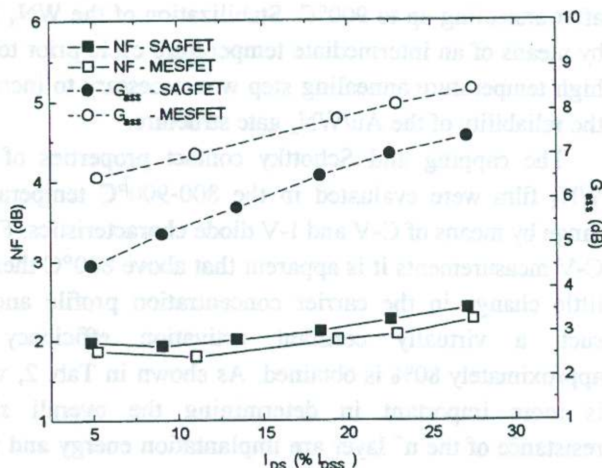

Fig. 3. Noise figure and associated gain of implanted SAGFET and implanted recessed-gate MESFET, given as a function of I_{DS} (in percent of I_{DSS}).

gain (G_{ass}) versus output power (P_{out}) characteristics at 12 GHz, presented in Fig. 2 for the two technologies. As shown, for the ion implanted devices (i.e. MESFET and SAGFET) the gain (7.5 ÷ 8.0 dB) and P_{out} at 1 dB compression ($P_{max} \approx$ 500 mW/mm) are very similar. The main difference being the lower power added efficiency (PAE) of the SAGFET device which required a higher drain bias voltage to achieve the same P_{max}.

The channel doping profile was found to be the main reason for the lower PAE of the ion-implanted SAGFET with respect to MESFET. Infact, as shown in Fig. 2, the epitaxial SAGFET device, with better control of channel doping, for the same bias conditions as the standard ion-implanted MESFET yields a $G_{ass} \approx$ 8 dB and $P_{max} \approx$ 550 mW/mm.

C. Low-level devices

The low-level SAGFET's, like their power counterpart,

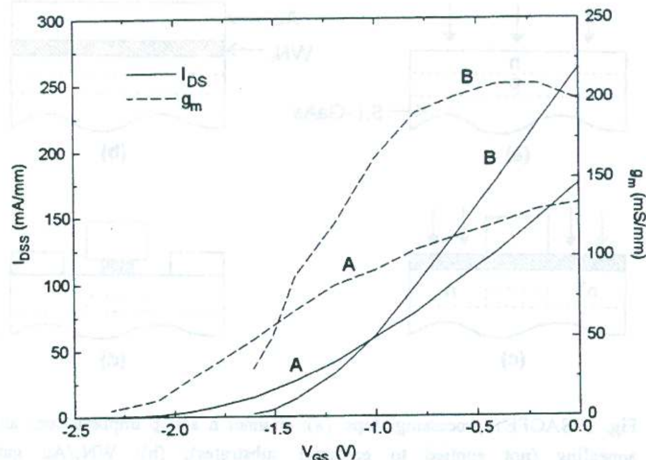

Fig. 4. I_{DS} and g_m as a function of V_{GS} for ion-implanted low-level SAGFET devices, without (A) and with buried p layer (B).

exhibit d.c. results similar to the recessed-gate MESFET's having the same implanted channel profile. Typical values obtained were $I_{DSS} \approx$ 180 mA/mm and $g_m \approx$ 140 mS/mm, $V_P \approx$ 2.0 V, $C_{GS} \approx$ 1.5 pF/mm. In Fig. 3 noise Fig. (NF) and associated gain (G_{ass}) at 12 GHz for different values of I_{DS} are shown, for both types of devices.

As shown, even though there is a good agreement in noise figure between the two technologies (i.e. $\approx$ 0.2 dB) a large discrepancy in associated gain (as much as 2 dB) is evident. Said observation can be explained assuming that similar parasitics contribute to NF in both cases and that g_m accounts for the lower gain found in the SAGFET. Just like in the power device, a short-channel effect is observed which lowers g_m near pinch-off, the current region of interest for low-noise applications.

As for the power device, a higher performance is expected with better carrier confinement, achieved with the introduction of the implanted buried p-layer. Preliminary d.c. measurements performed on low level discrete devices with the buried p are shown in Fig. 4, where results for the devices described above are also shown for comparison.

As shown, the introduction of the p layer results in a higher I_{DSS}, lower V_P, and, as a consequence, a higher g_m with respect to the corresponding devices decribed above. The same effect is observed on power devices. In particular, g_m is higher because the p layer beneath the n channel allows the use of higher n and n^+ concentrations and the reduction of gate footprint without the risk of short-channel effects.

Even though r.f. measurements are not avaliable for this article, extrapolations of the excellent d.c. characteristics indicate that these devices have higher performances than standard MESFET's. Infact, advantages will derive from the nearly doubled intrinsic cutoff frequency (g_m/C_{GS}) at I_{DS} = 10÷20% I_{DSS} for low noise

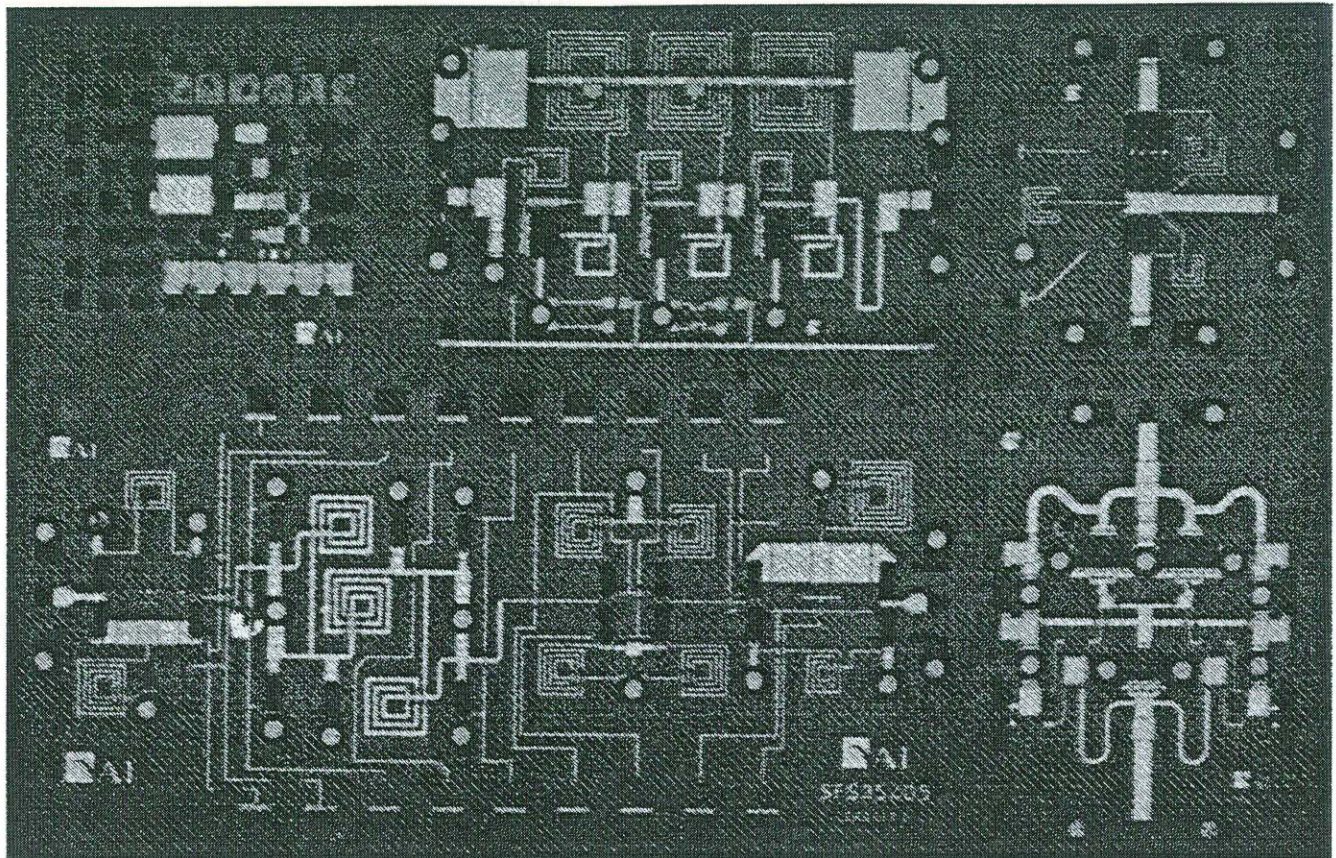

Fig. 5. Photograph of the integrated multi-function MMIC's. Clockwise from top left can be distinguished: a 3-stage low noise amplifier, a power switch, a power amplifier, and a 6-bit phase shifter.

applications, and from the increased I_{DS} linearity for power applications.

D. Multi-function circuits

To evaluate the feasibility of multi-function integration we have realized on the same wafer all the types of FET's (device models for next generation MMIC designs) and MMIC's necessary to the production of a Tx/Rx module: i.e. a three-stage low-noise amplifier, a 6-bit phase shifter, a power switch and an output power amplifier (shown by the photograph in Fig. 5).

Conclusions

In this paper we have outlined an original SAGFET technology which overcomes the major weaknesses and bottlenecks of current MESFET based processes. Said technology, based on both ion-implantation and epitaxy, even though in a preliminary phase, is already yielding performance (NF better than 2 dB and Pout ≈ 500 mW/mm at 12 GHz) and yield results comparable with the well consolidated MESFET technology. Moreover, preliminary d.c. characterization of devices with buried p-layer reveals increased g_m/C_{GS} value and I_{DS} linearity. As an example of the potentiality of SAGFET technology, a prototype integrated Tx/Rx chip for active phased array radar application has also been realised.

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