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Automatic design of GaAs MESFETs for thermal effect optimization

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Abstract

In this paper it is proposed an automatic procedure to extract optimal layout parameters in order to thermal effect minimization, for a MESFET with conventional structure, according to other design specifications. These parameters are the gate length, the gate width, the number of gates, the gate to gate spacing, the die thickness and the heat sink temperature. The procedure accounts for the dependence of the thermal conductivity of gallium arsenide on temperature and doping density.
Moreover the proposed procedure, joined with an I-V and a C-V MESFET thermal model already proposed by the authors is a part of a CAD tool for GaAs I.Cs. design for thermal effect optimization.

Introduction

The general evolution of power devices for higher frequencies operation using GaAs MESFETs and the recent interest in integrating power devices on MMICs on GaAs substrates emphasize the growing importance to thermal problems in design tasks. In fact, a problem with GaAs technology is the low thermal conductivity of gallium arsenide and this gives rise to thermal design problems which must be solved if good reliability is to be achieved.
Because of either operating temperatures different from 27 °C (external thermal effects) or the increase in temperature due to device heating because of electrical power dissipation (internal thermal effects), physical and technological parameters of devices [1-10] and, consequently, their electrical characteristics are modified.
In fact, considering a range of temperature about from -55 °C to 155 °C, internal and external thermal effects require an accurate I-V modeling, already proposed by the authors [11], an accurate C-V modeling [12] accounting for MESFET current and capacitance dependence on temperature, and the development of proper thermal design rules in order to optimize the device layout to allow a fast and well distributed heat spreading, i.e. in order to minimize the device thermal resistance.
In this paper it is proposed an automatic procedure to extract optimal layout parameters to minimize the thermal resistance of a MESFET with conventional structure.
This procedure joined with the accurate MESFET thermal model already proposed by the authors, allows to make up a CAD tool for automatic design of MESFETs based I.Cs.

A proper thermal layout design of GaAs power MESFETs involves the optimization of many geometrical and technological parameters, that is to say the device thermal resistance that depends on these parameters, which are, referring to fig. 1: the gate length L and the gate width W, the spacing between gate fingers, S, in a multigate power structure, the gate number n and the die thickness F.

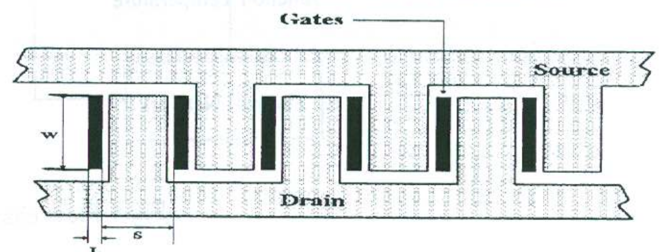

Fig.1 Layout geometry of the multigate MESFET.

In this paper the solder layer and the heat spreader are not considered but it is only taken into account the die on which the MESFET is fabricated.
The proposed procedure is based on thermal design rules described in the following section.

Thermal design rules

The thermal resistance of GaAs MESFETs increases with: the number of gates [13] (in a multifinger power structure); the die thickness; the temperature (because of the decreasing of the GaAs thermal conductivity); the unit gate width (because of the significant aid to the lateral heat dissipation due to the presence of metal layer adjacent to sources of heat flow).
On the contrary, the thermal resistance decreases by increasing: the gate spacing, the total gate width and the gate length. Anyway, this last parameter is generally imposed from other specifications as frequency performance and integration density. Therefore the gate length is not a very useful parameter for thermal design optimization because it can vary in a very small range of values.
The previuos considerations suggest that it is advisable to design a multigate structure with a great number of gates having a small width.
Via holes could be very important heat conducting paths only if there are placed as close as possible to the highest power dissipation region in the channel, that is the drain end of the gate. If the technology for the placement of via

holes allows that strategical positioning there can be reached a significant improvement in thermal resistance as well as a reduction in parasitic inductance [14], [15].
The thickness of the metallizations and the particular metal used to fabricate the gate, source and drain electrodes play a very important role for the reduction of the MESFET thermal resistance. In fact the metal layer aids the heat flow parallel to the gate width. The improvement in thermal resistance due to the presence of thick metallizations, is typically about 15% to 20%, and is likely to be increasingly significant for smaller gate widths and large spacing among gate fingers [14].
The optimal metal to fabricate ohmic contacts for drain and source electrodes is AuGe-based one in the considered range of temperature.
A saturation current reduction is caused by degradation of either electron mobility or the gate Schottky barrier due to thermal effects owing to metal semiconductor interdiffusion. In order to avoid the last degradation it is very important a suitable choise of metal used to fabricate the gate electrode. For this reason the Schottky contact for the gate junction is generally fabricated with gold based layered metalizations (as TiPtAu, TiPdAu, TiMoAu, CrPdAu) or various alloys such as TiW or WSi_X [16].
The optimal metal to fabricate the heat sink is gold, because of its high thermal conductivity, with other layered metallizations in order to avoid interdiffusion phenomena [14-17].
The thermal resistance of GaAs increases increasing the doping level; therefore in the device the thermal power dissipation takes place in the doping channel, that is a region of lower thermal conductivity than the semi-insulating bulk. For this reason the peak temperature undergoes a great decrease (whose value depends on the particular MESFET and on many other parameters as the input electrical power) if there are fabricated substrate thinnings under the active channel. Therefore, in a more refined but also more expensive technology, an important role to minimize the device thermal resistance could be played also by localized thinnings in substrate regions of high power dissipation, filled with a good conductor such as gold, named also buthtubs [15], [18], [19] and positioning via holes as close as possible to highest power dissipation regions [14]. Consequently if buthtubs are well fabricated drain away most of the heat therefore the contribution of surface metallic layers and via holes is almost negligible.
A very good combination of heat sink technology and buthtub fabrication is obtained with a Source Island Via-hole (SIV) structure [19]. An improved version of the SIV FET structure is the advanced SIV FET structure [19] that contains a selectively formed buried Plated Heat Sink (PHS technology) instead of having thick gold metal backside.
It is important to observe that either for conventional or advanced SIV MESFET structure it is advisable, for example, to reduce thermal resistance by designing a power MESFET with great number of gates of small unit gate width and with large spacing between gates. However, an increase of the gate number results in an increase of the thermal resistance; moreover an extension of the area on which device is fabricated is not convenient for the integration density. Therefore it is possible that for a particular MESFET structure a set of optimal values of these previous parameters is automatically determined making up a particular procedure to implement a total minimization of the device thermal resistance.
The initial values of the design parameters necessary to run the minimization procedure of thermal resistance are determined from the other design MESFET specifications as the maximum transistor saturation drain current, the resolution defined by the available technology in order to obtain the maximum integration density, the frequency performance and so on.
The last considerations about thermal design rules concern the microwave performance and the choise of bias point of MESFETs. First of all it is important to observe that common source configuration allows the highest amplifier gain and the best r.f. stability. Besides the microwave performance of MESFET can be related to three typical frequencies: the cut-off frequency f_c of the current gain; the cut-off frequency f_g of the maximum available gain and the maximum frequency f_o of oscillation. These frequencies are expressed as functions of the small-signal parameters. In order to maximize both f_g and f_o it is advisable to have high f_c, small output conductance g_o and a low feedback capacitance C_{gd}. For these reasons the most important design specifications for r.f. performance are f_c and C_{gd}. These requirements can be achieved by reducing the thickness of active channel and the gate length whilst increasing the doping level in order to avoid variations of pinch-off voltage. The specification about g_o is well satisfied especially avoiding thermal effects, i.e. by a well choose of bias point. Referring to fig. 2, it is convenient to choose the bias point of the device assuming a high value of I_{ds}, in order to obtain highest gain under small-signal conditions, and maintaining a value for V_{ds} near 2 or 3 V to avoid internal and sometime also external thermal problems.

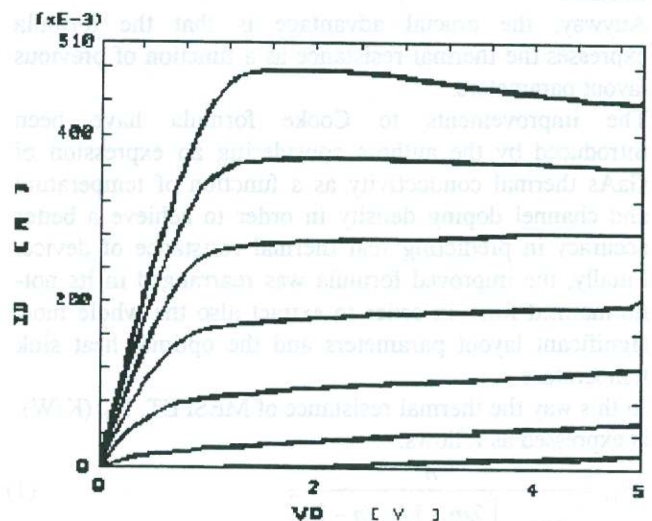

Fig. 2 I-V characteristics measured by the authors on a depletion mode power MESFET with considerable internal thermal effects. Vgs varies from 0 V to -3 V with a step of -0.5 V

Anyway, if it is more important to optimize thermal effects than to obtain the highest gain it is advisable to choose the bias point assuming a middle value for I_{ds}, i.e. choosing $V_{gs} \cong V_t/2$, where V_t is the threshold voltage of the device, and V_{ds} in the middle of the saturation region. In this way it is possible to obtain the best linearity performance, the best optimization of thermal effects and a good trade-off between minimum noise figure and the available gain. In fact, as it was outlined by the authors [21], internal thermal effects influence the saturation region of I-V characteristics more than the linear one for highest and lowest values of V_{gs}. Besides the MESFET is quite unsensible to external thermal effects in the cross point that is at (I_{ds}, V_{ds}, V_{gs}) values for which temperature does not make any influence. The cross point for a long gate MESFET is near the knee region while for short gate device is in the linear region.
A quite accurate estimation of the I-V characteristics can be calculated by means of an approximate I-V physical model as the very simple one in [21].

The proposed layout design procedure

The formula expressing the thermal resistance as a function of the previous parameters to implement in a minimization algorithm has been obtained by the authors improving the simple closed-form equation of thermal resistance developed for a conventional MESFET structure and proposed by Cooke [13].
In fact, Cooke formula does not account for the dependence of thermal conductivity of GaAs on temperature and doping level. Moreover it accounts for 3-D heat spread although the source of heat is considered approximatly equivalent to the charge on the gate electrode and would be therefore a surface thermal source. Besides the effect of heat flow off the ends of the gates has been ignored because it is important only in devices with a large L/W ratio, which is an unusual situation in modern design of broad-band amplifiers and high-speed switching circuits.
Anyway, the crucial advantage is that the formula expresses the thermal resistance as a function of previous layout parameters.
The improvements to Cooke formula have been introduced by the authors considering an expression of GaAs thermal conductivity as a function of temperature and channel doping density in order to achieve a better accuracy in predicting real thermal resistance of device. Finally, the improved formula was rearranged in its not-normalized form in order to extract also the whole most significant layout parameters and the optimal heat sink temperature.
In this way the thermal resistance of MESFET, R_{th} (K/W), is expressed as follows:

$$R_{th} = \frac{n}{WK_{th}\pi\left[\dfrac{2(n-1)}{\ln D_1} - \dfrac{(n-2)}{\ln D_2}\right]} \tag{1}$$

in which:
K_{th} is the thermal conductivity of GaAs expressed in W/(cm K) [20]:

$$K_{th} = \frac{C}{AT-B} \tag{2}$$

where T is temperature in K; the A, B, C coefficients depend on channel doping density;

$$D_1 = \left\{ \frac{2\left[\cosh(\pi \frac{S+L}{4F}) / \cosh(\pi \frac{S-L}{4F})\right]^{1/2} + 1}{\left[\cosh(\pi \frac{S+L}{4F}) / \cosh(\pi \frac{S-L}{4F})\right]^{1/2} - 1} \right\} \tag{3}$$

$$D_2 = 2\sqrt{\frac{1+\sec h\left(\frac{\pi L}{4F}\right)}{1-\sec h\left(\frac{\pi L}{4F}\right)}} \tag{4}$$

The introduction of (2) in (1), i.e. the introduction of temperature in the expression of thermal resistance to minimize the layout parameters, allows also to extract automatically the optimal heat sink temperature.
In order to achieve a reliable and very simple automatic layout design, there are very useful these quite pessimistic approximations: first of all it is used only (2) as thermal conductivity of the GaAs although the device has an active channel (doping GaAs) grown on a substrate (intrinsic GaAs); this is a pessimistic approximation because GaAs thermal conductivity decreases increasing doping level. Moreover there is not considered the influence of via holes for the heat spreading. This approximation allows a great semplification because modeling via holes makes much complex the expression (1). Nevertheless, it is a reasonable approximation and does not involve a significant loss in accuracy because via holes have an important role in order to aid heat spreading only if there are positioned near the region of maximum power dissipation and in a MESFET this region is the drain end of the gate [14] while generally via holes are positioned near the sources.
Another hypothesis, very useful in order to extract the optimal heat sink temperature, is that the bonding layer is silver loaded epoxy. In fact, in this situation the difference between the GaAs substrate temperature and the heat sink one is as small as possible compared with the temperature difference obtained with other bonding layers [15].

Conventional MESFET layout design example

As an example it was designed a depletion mode MESFET with the following specifications, according to the previous considerations: the bias point is in I_{ds} = 70 mA and V_{ds} = 3 V; the doping density in GaAs active

channel is $N=3.5*10^{17}$ cm^{-3}; for the given doping density the values of the coefficients in (2) are [20]: A = 0.0091743; B = 0.44143; C = 1; maximum drain current 100mA $\leq I_{dss} \leq$ 120mA; drain current density I_{ds}/W = 100mA/mm; threshold voltage V_t = -3.5 V; cut-off frequency of the current gain f_c = 50 GHz; unit gate width w = 100 μm.

From these specifications it is possible to calculate minimum and maximum values for the layout parameters to be automatically extracted.

To this aim simple design equations are used [21-23] that are very accurate especially for drain current density J_{ds} = 100 mA/mm and V_{ds} = 3 V.

The minimum and maximum values are necessary to run the minimization routine that is based on the random optimization algorithm.

The set of the optimal layout parameters extracted is: number of gate n = 11; gate length L = 0.4 μm; die thickness F = 51 μm; gate to gate spacing S = 27 μm; total gate width W = 0.11 cm; optimal heat sink temperature T = 309 K. The calculated thermal resistance, equal to 48.7 K/W, is the minimum possible for the previous MESFET design specifications.

Typical values of metallization thickness are assumed, that is 3.5 μm for Au-Ge based ohmic contacts of source and drain and 0.5 μm for the TiPtAu Schottky gate junction.

To fabricate the heat sink is chosen gold, because of its high thermal conductivity [16], [17].

A characterization procedure of the designed MESFET allows to extract the empirical parameters of the dc I-V and C-V thermal models already proposed by the authors. In this way it is possible to implement the model itself in a CAD tool for circuit simulation and to design any GaAs I.Cs. based on the designed MESFETs.

Conclusions

In this paper it was proposed a procedure to design automatically the GaAs MESFET layout fabricated with conventional structure.

This procedure allows to extract optimal layout parameters and heat sink temperature in order to minimize the thermal resistance.

The formula of thermal resistance as a function of layout parameters is an improved version of Cooke formula accounting for the dependence of GaAs thermal conductivity on temperature and channel doping density. Although in this paper the formula was developed for conventional MESFET structure physical considerations about heat spreading allows to make some quite pessimistic approximations that allows to adapt the formula itself also to the advanced SIV structure MESFET design [24], obtaining very satisfactory results.

A design example of conventional MESFET confirms the consistency of the proposed technique.

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