A Universal Test Set for DC and Pulsed I-V Characterization of Various Semiconductor Devices

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ABSTRACT

A universal DC and pulsed I-V test set is presented, that allows automated DC-only, pulse-only and DC + pulse measurements on 2 and 3 terminal semiconductor devices, the later ones in 3 selectable common-configurations. Tests can be done on packaged devices and on-wafer; temperature dependency studied and time-depended features like trapping effects in GaN-based HEMTs. Novel is that once the overall test setup is assembled, no external hardware changes are neccesary for a full (automated) characterization of all quadrants of the I-V plot, and that in the pulse mode the V and I sampling point already can be at 8 ns from the leading edge, allowing measurements with very limited average device temperature increase.

INTRODUCTION

The demand for a flexible DC and pulsed I-V test set to characterize our proprietary semiconductor devices like the Hot Electron Injection Laser (Hoskens et al (1)), our GaN-based HEMTs (Jacobs et al (2)), polarization switchable VCSELs (Strijbos et al (3)) and RTDs (Kwaspen et al (4,5)) led to the design and construction of the presented universal test set. It enables automated I-V testing of all kinds of 2 and 3-terminal devices in DC-only, pulse-only and DC + pulse mode for 3 common cases and floating (DC-only). Testing can be done on packaged chips; on devices mounted in fixtures or placed into cryostats or on-wafer using probe heads. Once the test set is embedded into the overall measurement setup, no hardware changes are neccessary, since all signal routing and voltage and current sensing is done internally. Pulsed I-V can already be made within 8 ns from the leading edge, limiting chip temperature rise to a minimum. The control of several functions can be done with a separate actuator, or manually by grounding the control lines or by buffered PC I/O lines. Examples of test applications are given.

TEST SET DESIGN

Operation of the universal test set is explained by means of Fig. 1 where the set is embedded in the overall measurement setup while Fig. 2 shows all common configurations and signal definitions. Available instruments connected through GPIB, or PC-based instrument boards assemble the overall setup shown. External polarity change of the DC-source voltages is optionally. The DC currents in the device under test (DUT) are read from the DC-source current monitors (high test set leakage resistances). The test set consists of a fully floating DC section and a microstrip line-based pulse section that can be used independently (DC-only, pulse-only, DC + pulse tests possible). All neccessary bias-tees, voltage and (pulse) current sensing circuitry, switching elements for routing of DC and pulse signals from sources to DUT, to voltmeters and to oscilloscope are internally. General labelling is used (Fig. 2) since the measured quantities depend on the configuration selected: index i for input side, index o for output side of a 3-terminal device. Actual labelling of measured DUT currents/voltages is done in software in relation to the configuration selected. DC-source 1, pulse source 1, Voltmeter 1 and two oscilloscope channels can be connected to the input side of a 3-terminal DUT, the other sources, voltmeter and oscilloscope channels are for the output side. DC voltages Vi and Vo measured at the DUT can also be used for remote sensing of the DC sources. The test set fully can be controlled by 7 control lines (be, cb, cb, ce, com-e, com-b, com-c; Fig. 1). Connecting line be or cb to ground connects DC-source 1 to the corresponding DUT terminals, while the second cb or the ce line does the same with DC-source 2, enabling all configurations. Zeroing one of the com control lines activates the routings for the corresponding pulse mode configuration. A 10 channel GPIB-programmable actuator performs this in the automated situation, or buffered PC I/O lines can be used. Simple switches can do the job in manual control.

A visual and audible signal warns for illegal circuit configurations during program development. A removable front panel overlay adapts function signalling for e-b-c or s-g-d devices tested. Fig. 3 shows some photographs of the completed test set (dimensions 4x14 x20 cm).

PERFORMANCE

The completed test set shows an isolation resistance of >10 GOhm between the e, b and c output lines and between these lines and ground (all possible routings tested). The series resistance of the route, DC-source input terminals to the

e, b and c center conductors of the SMA output connectors, was < 0.08 Ohm (all possible routings tested). In the pulse mode, the conversion sensitivity for main line pulse currents ie, ib, and ic is 4.75 mV/mA (50 Ohm oscilloscope input impedance; <= 1us pulse width). The pulse response of the route, pulse source input to e, b, c output connectors, was checked with a 30 ps TDR step waveform. The voltage and current waveforms vi, vo, ii and io were recorded for a number of load resistances installed at the e, b or c output, including 50 Ohm, a short and an open circuit. The results indicate that measurements at these connector reference planes reliably and accurately can be done at 8 ns from the leading current edge (see time markers in Fig. 4a). When the DUT is at a remote location in a test fixture, in a cryostat or in on-wafer tests, the connecting coaxial cables delay the pulse signals and one has to take transmission line phenomena into account to choose the correct sampling point of time for the measurement (Fig. 4b; 0.6 m of 50 Ohm coaxial cable between SMA output connector and terminating loads). The time markers in Fig. 4b show that the sampling point here must be at least 25 ns delayed from the leading edge for accurate measurement of load resistances of all values.

APPLICATIONS

Numerous examples can be given for the application of the universal test set. We choose some from our own semiconductor research program (see Introduction). Fig. 5a shows a common-source DC + pulse measurement at room temperature on an AlGaN/GaN HEMT on sapphire, showing gate lag before passivation. The gate of the device (length 2 um; width 2x 40um) is DC biased around threshold (Vgs=-8 VDC), so Id(DC) is low at a constant Vds of 10 VDC (no drain pulse applied). A positive 100 ns wide pulse with 9 ns risetime is also applied to the gate so in that time frame Vgs=0, and the device is switched on. The drain current shows a typical shape with a too low pulsed current value (25 mA) compared to Id(DC)=32 mA @ Vgs=0 VDC, indicating dispersion. Figure 5b shows the DC and pulsed Id-Vds curves of this (unpassivated) device. Surface passivation improves the device performance as Fig. 5c shows for a similar device on the same sample. The corresponding DC and pulsed Id-Vds plot is shown in Fig. 5d.

CONCLUSION

A universal DC and pulsed I-V test set is presented, that allows automated DC-only, pulse-only and DC-offset pulse measurements on 2 and 3 terminal semiconductor devices, in 3 selectable common-configurations.
Pulsed I-V can already be made within 8 ns from the leading edge, limiting chip temperature rise to a minimum. Although intended for research purposes, the universal test set is as well suited for educational class-room projects on semiconductor devices, due to its compact, simple and low-cost design.

ACKNOWLEDGEMENTS

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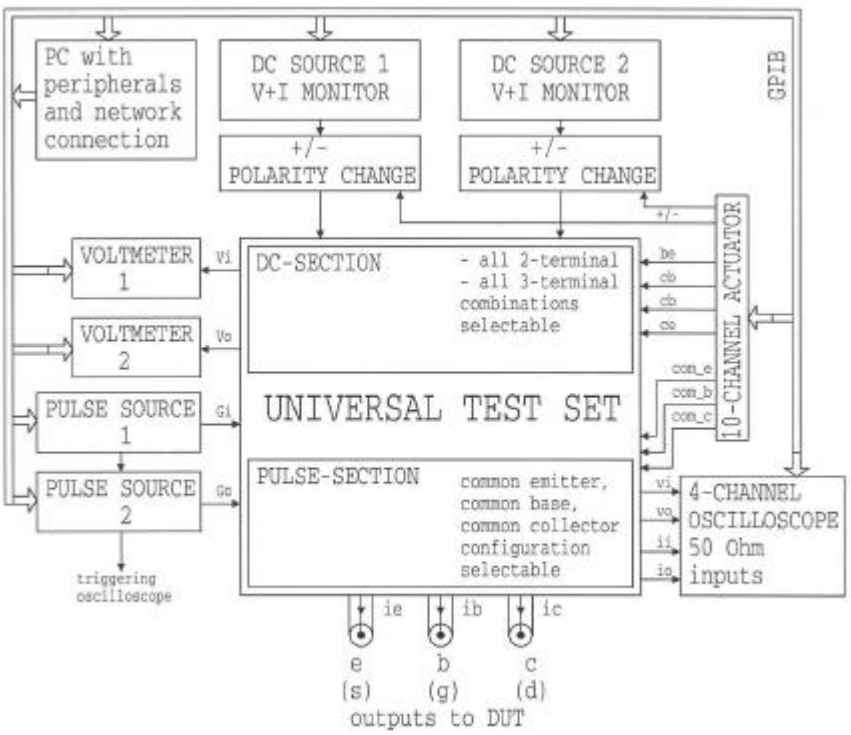

Fig. 1 Universal Test Set embedded in the overall measurement setup

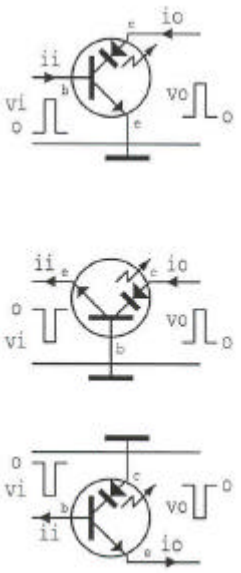

Fig. 2 Hot Electron Injection Laser symbol in common-emitter, common-base and common-collector configuration, with general current and voltage labels

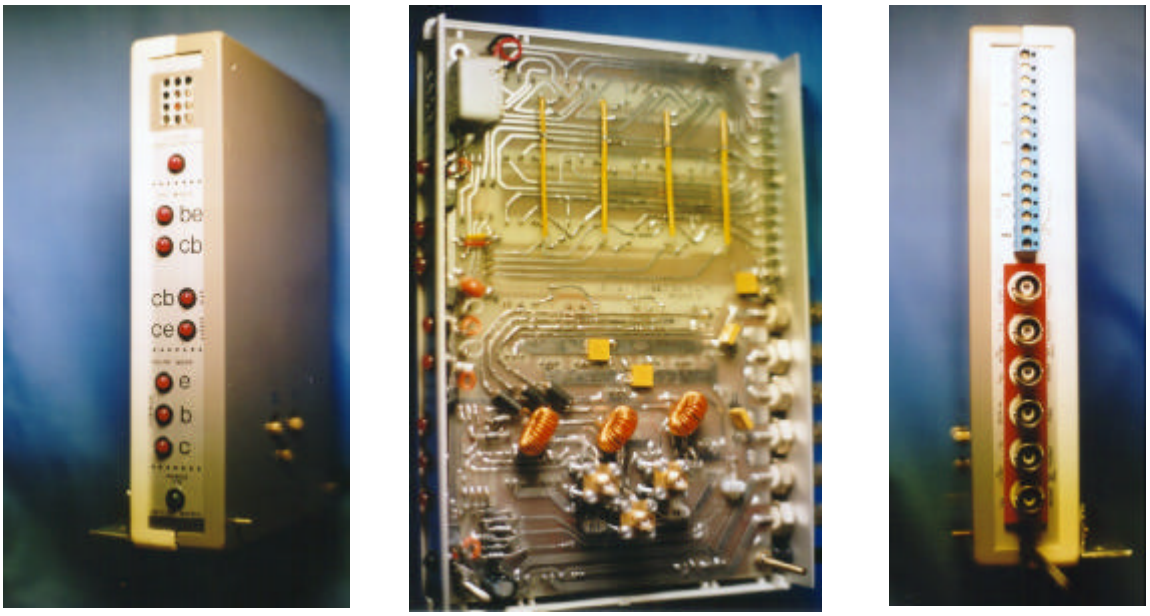

Fig. 3 Photographs of completed Universal Test Set

left: Front panel with function signalling and e-b-c- overlay
center: Interior view
right : Rear panel with voltmeter and DC-source terminals, BNC connectors for pulse sources and oscilloscope

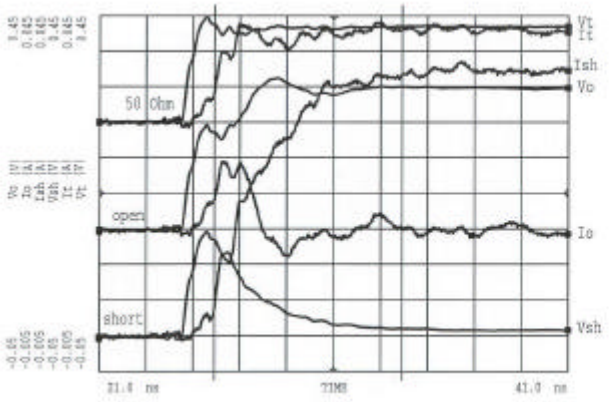

Fig. 4a Voltage and current pulses for a 50 Ohm load, an open and a short at the test set SMA output connector. Curves of 50 Ohm and open offsetted for clearity reason. Time scale 2 ns/div.

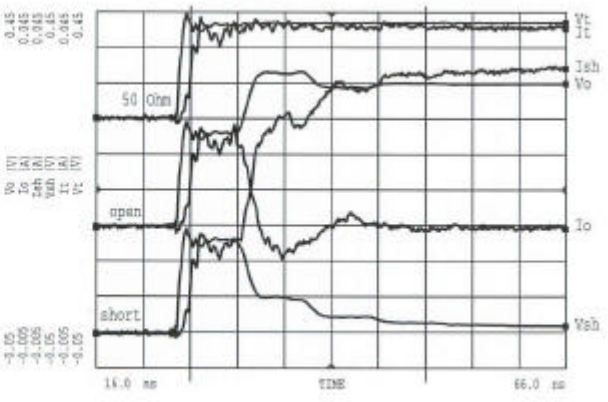

Fig. 4b Voltage and current pulses for a 50 Ohm load, an open and a short at the end of a 0.6 m coaxial cable connected to the SMA output connector. 50 Ohm and open curves offsetted. Time scale 5 ns/div.

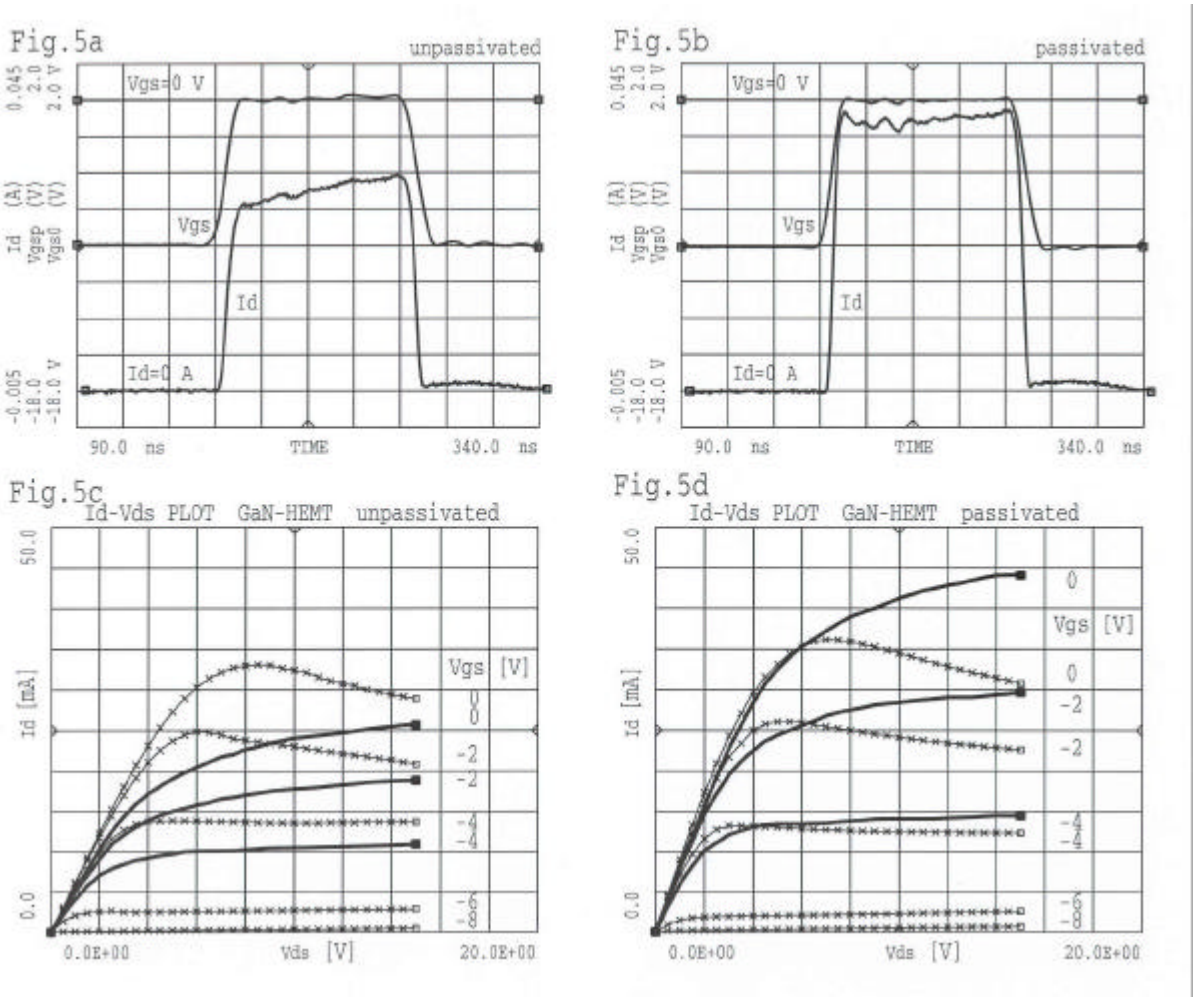

Fig. 5a,b On-wafer DC+pulse measurement on unpassivated (Fig. 5a) and passivated (Fig. 5b) AlGaN/GaN HEMTs of similar gate dimensions (l=2 um; w=2x40 um) on the same sample.
Vds(DC)=10 V; Vgs(DC)= -8 V. Input gate pulse: 20 kHz; pw=100 ns; rise time= 9 ns.

Fig. 5c,d On-wafer measured Id-Vds plots on those devices. Curves: xxx : DC conditions; __ : under pulsed gate bias. Sampling point at 15 ns from leading edge.