Current gain mechanism in planar GaAs MESFETs due to new photovoltaic self-biasing edge-effect.

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Abstract

A significant new internal gain effect, in planar MESFETs has been discovered which we call the "photovoltaic self-biasing edge-effect." The edge-effect can be exploited to attain up to a factor of ten improvement in detector photosensitivity.

Introduction

Under the conditions of photovoltaic self-biasing [1], we have observed that there is a sharp increase in drain current when the transistor edges are illuminated [2]. This new internal gain edge effect is promising for enhanced photosensitivity, by a factor of ten, for lower frequency devices such as GaAs motion detectors [3], XY array imagers [4], optoelectronic neural nets [5] and X-ray detectors [6]. The edge effect also has applications in device diagnostics and measurement – a new simple technique for determining SI substrate carrier diffusion length is demonstrated. Diffusion lengths of an order of magnitude lower than in silicon are observed – this is significant for improved spatial resolution in high definition television (HDTV) imagers. The edge-effect discovery is particularly suited to producing increased photosensitivity in a smart sensor array based on insect vision [3].

Results are displayed for measurements on planar D-MESFETs on SI substrate. It is observed that mesa structures do not display the effect. Furthermore the presence of a p-buffer layer diminishes the gain – therefore planar devices with no p-buffer layer give rise to the greatest photocurrent gain. These results are consistent with the hypothesis that photocurrent in the substrate has access to the gate, at the transistor edges, creating an increased voltage drop across the gate resistor, thereby modulating the drain current. 3-D electric field mesh plot simulations confirmed contiguity of electric field between the gate depletion region and channel/substrate depletion region, at the edge, that allows substrate photocurrent to flow into the gate. This is the first time that such interaction has been discussed in the literature.

The photoresponse mechanisms in GaAs MESFETs are presently under debate [7, 8, 9, 10, 11, 12]. This new edge mechanism has been hitherto unaccounted in the debate thus far, and thus must be included in future models. The practical applications are exciting as photosensitivity is increased by a factor of ten, and this can be exploited by appropriate design layout.

Two Dimensional Laser Scan Set Up

The planar MESFETs used have a fingered structure with 5 gates, $L = 0.8$ μm and overall $W = 400$ μm. The channel (depth, $d = 0.1$ μm and doping, $N_d = 1.2\times10^{17}$ cm^{-3}) is situated on a semi-insulating (SI) GaAs (EL2) substrate, with no buffer layer. The source-gate and drain-gate separations are both 1.3 μm.

The device was mounted on a computerised X-Y platform and illuminated by a 2 μm diameter CW laser spot with a wavelength of 678 nm. The laser power incident on the device was measured to be 1.4 μW. The X-Y platform was controlled to move the device through a 2-D raster sequence and the drain current was automatically logged so that a 3-D plot of the transistor response was generated.

Two Dimensional Scan Results

Example 3-D plots of transistor drain current response to laser illumination are shown in Figs. 1 & 2. For comparison, the case for no series gate resistor is shown in Fig. 1. Peak drain current is in the central region of the transistor, and the drain current rolls off towards the periphery of the transistor, as expected. However, with a 10 MΩ resistor in series with the gate, Fig. 2 shows dramatic drain current peaks at the positions where gate metal crosses the transistor edge. The five peaks, along an edge, correspond to the five gates. There are two sets of five peaks, as the gates overlap the transistor at both ends, of course. From the decay of these peaks, the carrier diffusion length in SI GaAs can be easily extracted

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and our initial estimate is ~10 μm.

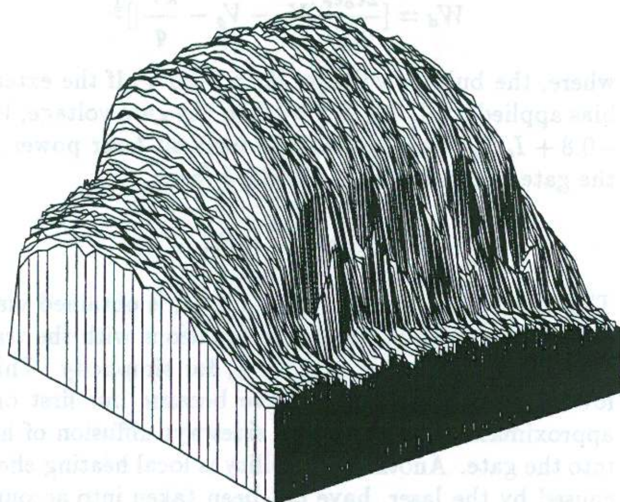

Figure 1: Measured MESFET drain current response (z-axis) to 2-D laser scan, max. current 3.7mA. No gate resistor.

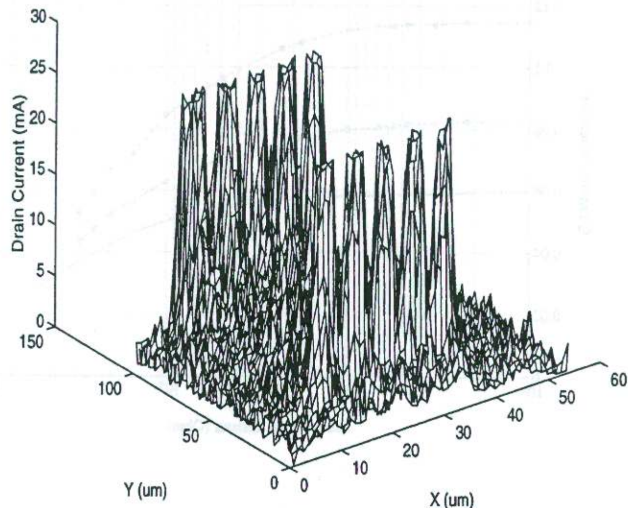

Figure 2: Measured MESFET drain current response (z-axis) to 2-D laser scan, max. current 29mA. With 10MΩ gate resistor. 3-D plot.

These plots were repeated for a number of devices and it was observed that the peak heights did not vary substantially, within each set of five. However, there were some cases when a set peaks at one end of the transistor was as much as four times the height as the set at the opposite end. This effect could not be correlated with any visible transistor layer misalignment.

Note that although the gates are opaque, the peaks actually correspond to a position where the laser spot is exactly centred on the gate. This is because the spot diameter is larger than the gate length and thus a central position maximises the amount of light to the gate edges, where the depletion region extends outwards, from under the gate, and is exposed. Also holes diffusing in the channel, that are generated close to the gate edges, can be collected by the gate depletion region. Even though the diffusion length of holes in the channel is 1.8 μm, holes that are far from the gate are more likely to be collected by the channel/substrate depletion region because the channel depth $d \ll 1.8$ μm – therefore there is a very narrow capture angle for gate collection. The Fig. 3 contour plot illustrates the integrity of the mechanical scanning system, showing no obvious smearing of data.

Discussion

We established that the peak drain current could be accounted for by an increase in gate photocurrent, as measured by an electrometer. Fig. 4 shows gate photocurrent versus R_g, when the laser spot is centrally placed on the gate, for a position at the transistor edge (high gain) and towards the middle of the transistor (low gain). The

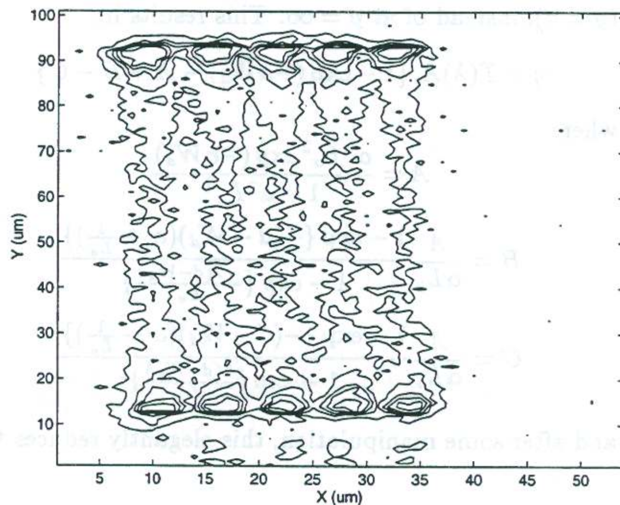

Figure 3: Measured MESFET drain current response (z-axis) to 2-D laser scan, max. current 29mA. With 10MΩ gate resistor. Contour plot.

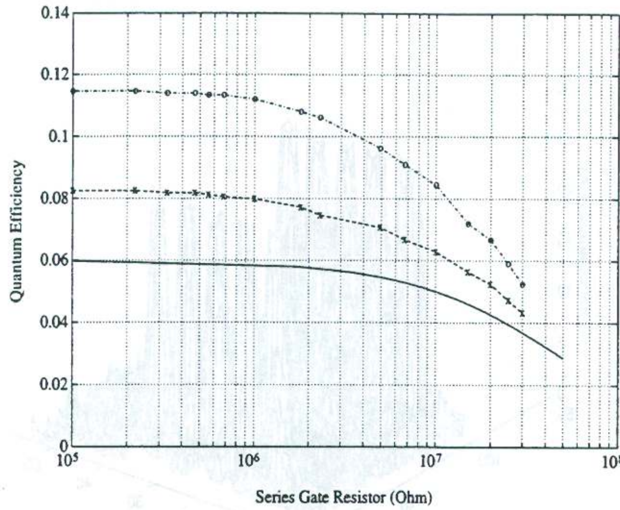

Figure 4: Quantum efficiency versus gate resistor. Solid line: internal quantum efficiency (T=1) from first order theory. Dashed line: measured (low gain). Chained line: measured (high gain).

theoretical curve is found by following the front illumination case of Seib [13], to evaluate the quantum efficiency, η. However, in a GaAs MESFET, the boundary conditions change and the equations are now solved with hole concentration $p = 0$ at the substrate/channel interface ($y = d$), instead of at $y = \infty$. This results in,

$$\eta = T(\lambda)A_o\{1 - \exp(-\alpha W_d) - A + B - C\} \quad (1)$$

where

$$A = \frac{\alpha^2 L_o{}^2 \exp(-\alpha W_d)}{1 - \alpha^2 L_o{}^2}$$

$$B = \frac{A}{\alpha L_o} \frac{1 - \exp\{-(d - W_d)(\alpha + \frac{1}{L_o})\}}{1 - \exp\{\frac{-2(d-W_d)}{L_o}\}}$$

$$C = \frac{A}{\alpha L_o} \frac{1 - \exp\{-(d - W_d)(\alpha - \frac{1}{L_o})\}}{1 - \exp\{\frac{2(d-W_d)}{L_o}\}}$$

and after some manipulation, this elegantly reduces to,

$$\eta = 1 - \frac{e^{-\alpha W}}{1 + \alpha L_o} - \frac{\alpha L_o e^{-\alpha W}}{\alpha^2 L_o^2 - 1} \frac{e^{-h/L_o} - e^{-h\alpha}}{\sinh(h/L_o)} \quad (2)$$

where L_o is the hole diffusion length in the channel and α is the absorption coefficient at the wavelength of interest. If we assume that the depletion region extension from under the gate is W_d and approximate that light is only captured in these regions, as a first order estimate, then the dimensionless geometry factor, $A_o = 2 \times 1.83 \times W_d/\pi$.

The depletion region width, W_d, is given by the standard relation for a Schottky barrier,

$$W_d = [\frac{2\epsilon_o\epsilon_r}{qN_d}|V_{bi} - V_g - \frac{kT}{q}|]^{\frac{1}{2}} \quad (3)$$

where, the built-in voltage, $V_{bi} = 0.85$ V. If the external bias applied to R_g is -0.8 V, then the gate voltage, $V_g = -0.8 + I_g R_g$. By knowing the incident laser power, P_o, the gate photocurrent is obtained from,

$$I_g = (\frac{q\lambda}{hc})\eta P_o. \quad (4)$$

The theoretical curve for η, in Fig. 4, is obtained via an iterative solution of the above equations with the transmission coefficient set at $T = 1$, for simplicity. This is lower than the measured curve because our first order approximation has neglected sideways diffusion of holes into the gate. Another possibility is local heating effects, caused by the laser, have not been taken into account – however initial calculations show that this effect is negligible. Future work could consider a full three dimensional solution to the diffusion equation. We consider the following hypotheses in order to explain the increase in gate photocurrent that produces the sharp increase in drain current at the transistor edges:

HYPOTHESIS 1: *Gate metal thinning over the edge.* Possibly the gate metal thins at the edge, enough to become partially transparent, thereby letting in more light. This hypothesis is easy to reject, as such thinning would effectively increase the area factor A_o by 30% at most – this can only modulate the drain current by 2-3 mA at the most. We need an effect that is ten times that order.

HYPOTHESIS 2: *Electric field at edge.* It is conceivable that the abrupt junction at the transistor edge is causing a region of high electric field that results in a higher current flowing through the gate. A 3-D electric field plot generated by G-PISCES-2B, that uses Spicer's unified defect model showed that at the edge, the field was smooth and well-behaved. Therefore we reject this hypothesis.

HYPOTHESIS 3: *Contiguous depletion regions.* G-PICES-2B plots show that the depletion region that supports an electric field under the MIS gate overhang is contiguous with the gate depletion region. It is also quite obvious that the channel/substrate depletion region must also connect here at the transistor edge. Therefore the large volume of depletion region, just outside the transistor edge, at the meeting point of the gate, MIS and channel/substrate depletion regions greatly increases the photocollection capacity. Photocharge generated in this region can flow into the gate, via connecting field lines, giving rise to an increased gate photocurrent. A conceptual diagram of how the field lines possibly flow is shown in Fig. 5. We estimate that the channel/substrate depletion region is of the order of 2 μm and thus the resulting collection volume is large enough to explain the

observed effect. Consequently this becomes our working hypothesis. According to our working hypothesis, the

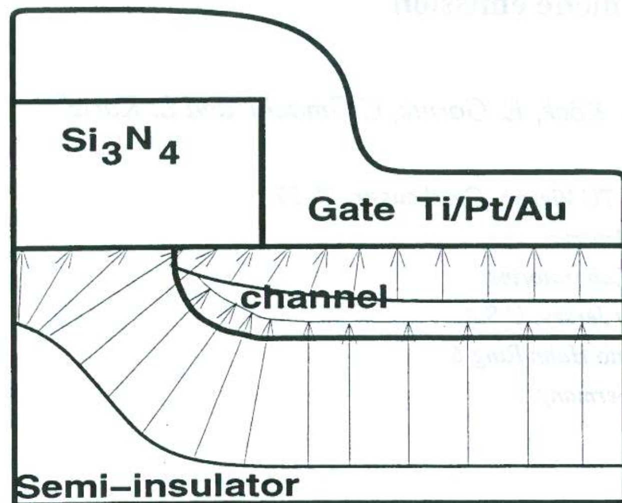

Figure 5: Exaggerated sketch showing electric field connectivity between, gate, channel substrate and MIS gate overhang depletion regions.

high gain curve in Fig. 4 can be explained if there are holes generated in the substrate, outside the transistor, being collected by the gate. Therefore we postulate the existence of a depletion region in the substrate that has connecting electric field lines with the edge of the gate depletion region. This new depletion region is assumed to be formed under the MIS structure, where the gate extends over Si_3N_4, outside the transistor. The channel/substrate depletion region must also connect at the edge and, given a depth of about 2 μm, we estimate that the depletion region would need to protrude from under the MIS electrode by about 0.2 μm to account for the high gain curve in Fig. 4.

Conclusion

In conclusion, we have reported a new optical edge gain effect in planar GaAs MESFETs, useful in low frequency applications, such as in an X-Y array imager. Photocollection under the MIS gate extension, outside the transistor, is suggested to explain the gain effect. Future models for the photoresponse in planar GaAs MESFETs, that attempt to generalise all operating conditions, must take into account this new effect.

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