Current instability and burnout under MESFET gate breakdown

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Abstract

The gate burnout (irreversible breakdown) of GaAs MESFET has been studied using two-dimensional (2-D) numerical simulation and experimental measurements of 10 ns pulsed gate-source I-V characteristics. It is shown, that at some critical level of gate avalanche current the gate current instability appears. The instability results in formation of a negative differential conductivity (NDC) region on the S-shape gate-source I-V characteristic, spatial instability of avalanche current and formation of high density current filaments.

Introduction

The instantaneous local burnout of small signal MESFET's have been observed at some critical pulsed input microwave power [1]. The burnout took place in a wide range of pulse duration from 1 ns up to static regime [1]. There were developed several thermal models for prediction of that breakdown [2,3]. Most of them are based on the assumption of the thermal overheating (that results in the structure melting and failure) occurs inside a certain "defect" sphere [2,3]. However physical mechanism of the local heat source formation was not clarified and dimension of the defect sphere was used in models as a fitting parameter. Meanwhile it is known, that local burnout of various semiconductor structures is the result of the electric or thermal current instabilities that lead to the current filamentation. For example isothermal current instability and current filament formation cause electrical drain - source burnout in the GaAs MESFET's and HEMT's [4-7]. Characteristic time of this electrical instability is less than 1 ns i.e. considerably smaller than characteristic time of the thermal instability evolution [3]. One can suppose that a current instability and filamentation could be the cause of "defect" sphere formation at the gate breakdown. Moreover, because gate breakdown is the major physical limitation of state of the art MESFET's and HEMT's output power [8-11] a proper understanding of its physical mechanism is helpful for reliability.

The purpose of this study is to demonstrate by the help of 10 ns pulsed measurements and 2-D simulation, that current instability and filament formation are observed in GaAs MESFET at some critical level of gate avalanche breakdown current.

Experimental and calculation procedure

Pulse gate-source I-V characteristics of the serial GaAs MESFET's AP608 were measured at 10 ns pulse duration and 0.0001 % duty factor using technique [4]. The MESFET's have the 3 μm drain - source spacing, 0.7 μm recess length, 0.5 μm gate length, 280 μm total gate width, 1 μm buffer layer, 0.15 μm active layer of 1.5×10^{17} cm^{-3} donor concentration, 0.2 μm contact layer of 1.5×10^{18} cm^{-3} donor concentration, Ti-Pt-Au gate and Au-Ge-Au drain and source metalization.

For numerical solution of the quasi hydrodynamic equations of MESFET model [6] the absolutely stable, completely conservative finite-difference scheme [13] was used. The scheme allows one to obtain an accurate solution on the rough spatial and temporal grids. To simulate MESFET's characteristics in the NDC region the equations were solved with "mixed" boundary conditions: fixed source and drain electrical potentials and fixed total gate current. To simplify the understanding of the NDC formation mechanism the simple planar structure (without recess and depletion layer) (Fig.1(a)) was calculated. Following structure parameters were used: the drain-gate spacing is L_{DG}=1μm, the gate-source spacing is L_{GS}=0.475 μm, the gate length is L_G=0.525 μm, the lengths of the source and drain n^+-contact region equal to L_s=L_D= 0,3μm, the thickness of the active layer is W_{AL}= 0.18 μm, the donor concentration in the active and contact layers are 1×10^{17} cm^{-3} and 1×10^{18} cm^{-3}, respectively, the thickness of the semiinsulating layer is W_{SI}=1 μm. The special M-i-n^+ structure with Shottky contact was used for simulation of the spatial instability and filamentation (Fig.1(b)).

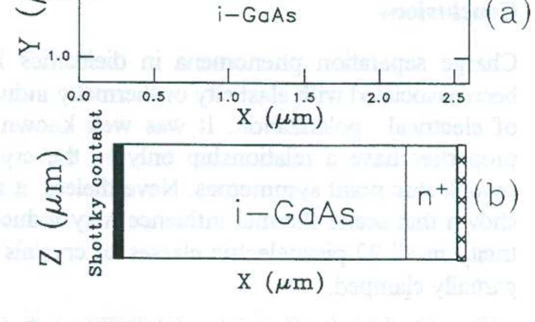

Fig.1. GaAs MESFET (a) and GaAs Shottky M-i-n (b) models.

Results

A. Experimental results

The typical pulsed gate-source characteristic is presented in Fig.2 by solid line. At some critical value of gate-source voltage the avalanche breakdown arises in the gate-source spacing near the gate metallization edge. Under high duty factor the evolution of avalanche breakdown may be observed by the help of optical microscope as uniform light strip at the gate edge. At a certain critical gate avalanche current the reversible switching into a new state took place (Fig.2). The light emission intensity in the switched state was too small for intensity distribution investigation. Considerable increase of current, duty factor or pulse duration in the switched state results in short-circuiting of the gate-source spacing and MESFET burnout. However visible destruction in the gate-source region of the burned MESFET's was not found in optical microscope. To indicate a short-circuited region localization in the burned MESFET the gate-source circuit was constant biased. This led to the gradual melting of the gate metallization around a region about 1 μm width. This allowed to conclude, that the cause of short-circuiting have been formation of the conducting channel of transverse dimension about 1 μm at certain depth under semiconductor surface. According to the experimental I-V-characteristic (Fig.2) current density inside this region was larger than 10^7 A/cm^2. So that dissipated in this channel power was enough to melt the MESFET structure during a very short time. Apparently, that short-circuit channel could be formed by the direct transport of AuGe-GaAs eutectic or metal-GaAs interdiffusion [1] between source and gate electrodes. Pulsed drain-gate I-V characteristics and burnout peculiarities were similar for source-gate characteristics.

B. Simulation results

The calculated MESFET gate-source I_G - V_{GS} characteristic for the drain - source bias V_{DS} = 4V is presented in Fig.2 by dashed line. For understanding of processes resulting in NDC formation the electric field, electron and hole density depth profiles are presented in Fig.3 for the high conductivity state (A). Initially evolution of the avalanche impact ionization results in the nonequilibrium carriers flow through the semi-insulating layer. In this state a picture of avalanche breakdown corresponds to the data presented in [10]. In the state (A) the density of the nonequilibrium carriers in a semi-insulating layer is larger and exceeds 10^{17} cm^{-3}. The electrons and holes form quasineutral region in the gate-source spacing (Fig.3(b, c)) and the additional region of avalanche multiplication is formed near source n^+-i junction (Fig.3(a)). Increasing of the carrier injection from the two avalanche region leads to the expansion of the

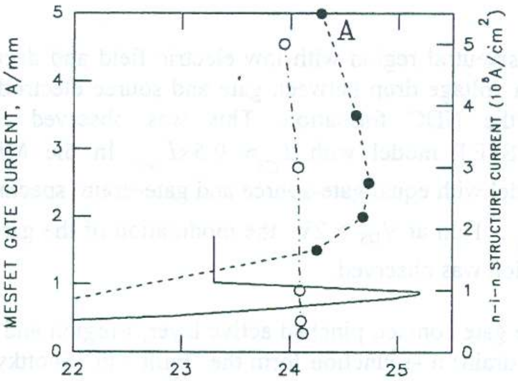

Fig.2. Experimental pulsed gate-source I-V characteristics of the AP608 MESFET (solid line) and the calculated gate-source I_G-V_{GS} characteristics of GaAs MESFET under V_{DS} = 4V drain bias (dashed line), M-i-n of Shottky structure with W = 10 μm (dashed-dotted line).

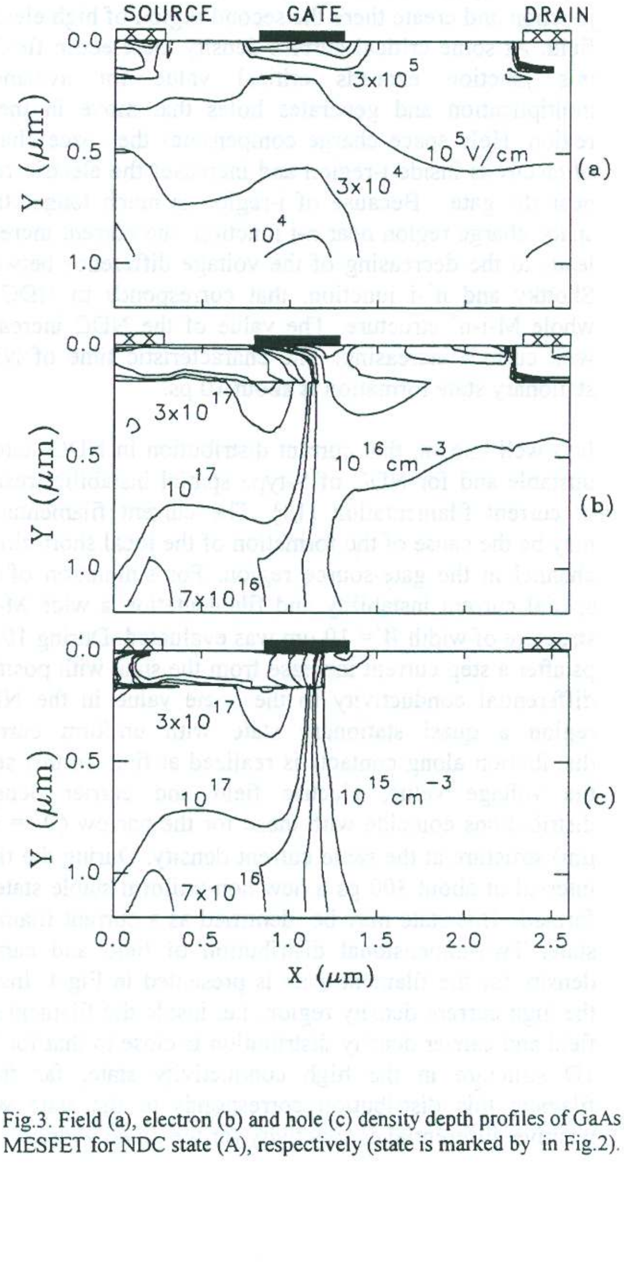

Fig.3. Field (a), electron (b) and hole (c) density depth profiles of GaAs MESFET for NDC state (A), respectively (state is marked by in Fig.2).

quasineutral region with low electric field and decreasing of a voltage drop between gate and source electrodes, i.e. to the NDC formation. This was observed for the MESFET model with $L_{GS} \approx 0.5 \times L_{DG}$. In the MESFET model with equal gate-source and gate-drain spacing $L_{GS} = L_{DG} = 1 \mu m$ at $V_{DS} > 2V$ the modulation of the gate-drain region was observed.

The gate contact, pinched active layer, i-region and source (or drain) n^+-i junction form the "built - in" Shottky diode structure. To demonstrate that I -V characteristic of such Shottky structure have NDC region due to conductivity modulation of i-GaAs layer the simple Shottky M-i-n structure with width W=0.5 μm was simulated. This narrow structure was treated as 1-D structure. For simplification the positive biased n^+-contact of the simulated structure will be lower referred to as a "source" and negative biased Shottky contact as a "gate". As bias increases the avalanche multiplication in the space charge region begins. Generated electrons move to the n^+-i junction and create there the second region of high electric field. At some critical current density the electric field at this junction exceeds critical value for avalanche multiplication and generates holes that move in the i-region. Hole space charge compensates the space charge of electrons inside i-region and increases the electric field near the gate. Because of i-region is much longer than space charge region near n-i junction the current increase leads to the decreasing of the voltage difference between Shottky and n^+-i junction, that corresponds to NDC of whole M-i-n^+ structure. The value of the NDC increases with current increasing. The characteristic time of NDC stationary state formation is about 10 ps.

It is well known, that current distribution in NDC state is unstable and for NDC of S-type spatial instability results in current filamentation [13]. The current filamentation may be the cause of the formation of the local short-circuit channel in the gate-source region. For simulation of the spatial current instability and filamentation a wide M-i-n structure of width W = 10 μm was evaluated. During 10-20 ps after a step current increase from the state with positive differential conductivity to the some value in the NDC region a quasi stationary state with uniform current distribution along contacts is realized at first. In this state the voltage value, electric field and carrier density distributions coincide with those for the narrow (W = 0.5 μm) structure at the same current density. During the time interval of about 300 ps a new non uniform stable state is formed. This state may be identified as a current filament state. Two-dimensional distribution of field and carrier density for the filament state is presented in Fig.4. Inside the high current density region, i.e. inside the filament the field and carrier density distribution is close to that for the 1D structure in the high conductivity state, far from filament this distribution corresponds to the state with positive differential conductivity for the given voltage.

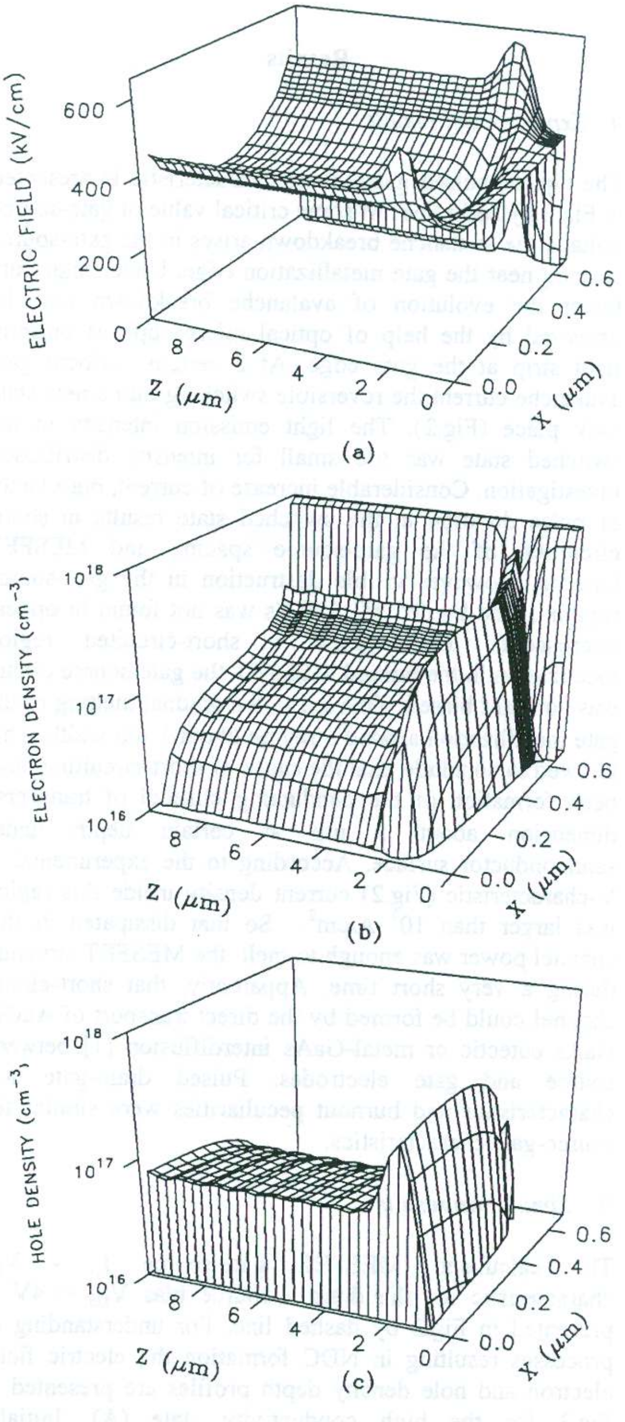

Fig. 4. Current filament in the GaAs M-i-n of structure of W = 10 μm gate width, L_i=0.6 μm L_n= 0.3 μm . Field (a), electron (b) and hole (c) density distribution for 3×10^5 A/cm^2 current density

Discussion

The results of the M-i-n structures simulation agree with dates of earlier studies [14-16]. The positive feedback that causes the S-type NDC formation and current filamentation in these structures is due to double injection of carriers, created by impact ionization near two contacts into an extended i-region with changes the electric field distribution along the whole structure. In the GaAs MESFET two "built-in" structures having NDC may be defined. The first M-i-n$^+$ structure is formed by Shottky gate, i-buffer layer and source (or drain for $L_{GS}= L_{DG}$) n$^+$-contact; the second M-n-n$^+$ structure is formed by Shottky gate, active n-layer and source (or drain for $L_{GS}= L_{DG}$) n$^+$-contact. The critical current density of NDC formation for M-i-n$^+$ is lower than for M-n-n$^+$ one, because of an additional current is needed in the last structure for compensation of space charge of ionized donors in n-layer. Besides, holes from the n-channel penetrated into the buffer layer.

Therefore the current filamentation, that causes the source-gate breakdown in the MESFET's, develops primary in the buffer layer. This explains why a gate-source burnout takes place in the depth of the MESFET structure. Simulation of spatial instability on the basis of the 2-D quasi hydrodynamic model without any source of fluctuations is possible due to presence of numerical fluctuations in the finite-difference scheme. Instabilities of spatial distribution of current of the semiconductor structures with S-type NDC have been analyzed in [13].

According to the simulation results a time of filamentation is about 10^{-10} s. Using obtained results a qualitative mechanism of instability of small signal MESFET's under some critical level of microwave power may be understand as follows. For high microwave frequency the duration of the gate breakdown state does not exceed 10^{-11} s. This time is much less than characteristic time of spatial instability evolution in structure. This allows to conclude, that at some critical level of pulsed microwave power the critical level of avalanche current will be determined by some integral avalanche current value slowly dependent upon microwave frequency. Exact solution of current instability evolution under high pulsed microwave power is interesting to complete. However it is possible to suppose that burnout mechanism will be also connected by current instability and filament formation.

For off-state breakdown of conventional power MESFET and HEMT maximum drain-source voltage is limited by drain-source current instability of avalanche-injection nature due to modulation of buffer layer [4-7]. The critical drain and consequent gate current for drain-source current instability in real off-state operation [6] are considerably lower than critical current for the gate-drain instability. However for understanding off-state or large signal burnout of arbitrary FET's structure in a condition of high gate avalanche current both mechanisms must be considered.

Conclusion

Using 10 ns pulse I-V characteristic measurement and 2-D numerical simulation the gate electrical burnout of GaAs MESFET was studied. It has been shown, that under some critical level of avalanche current through the gate the current instability in the gate-source (or gate-drain for $L_{GS}= L_{DG}$ and V_{DS}>2V) spacing is observed. The instability leads to NDC in the source-gate circuit and reversible switching of MESFET structure into a new non-uniform state with a current filament about 1 μm dimension located in a buffer layer. The mechanism of current instability is a "parasitic" modulation of buffer i-layer conductivity in the gate-source spacing. In the NDC state a spatial instability results in formation of a stable current filament of 1 μm dimension. The conductivity modulation mechanism presents itself as a double avalanche injection into i-layer and is similar to observed one in reverse biased p-i-n structures. The burnout of MESFET structure is the result of the local melting and formation of the eutectic leakage channel that short circuited gate with source in the buffer layer inside filament.

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