4C10 Gallium Arsenide Application Symposium GAAS®96 Paris CNAM
5-7 June 1996

A Novel Single-Bias Ultra-Wideband Monolithic Pulse Amplifier

Franco Giannini, Ernesto Limiti and Giancarlo Orengo

Department of Electronic Engineering - University of Roma "Tor Vergata"
Via della Ricerca Scientifica - 00133 Roma - ITALY

Abstract

A single-bias monolithic pulse amplifier realised in standard 0.5μm GaAs MESFET technology is presented. The amplifier features broadband operation from quasi-DC to 5.5 Ghz. Measured performances of the stage include 55 ps rise time, together with a variable gain ranging from 18 to 5 dB depending on the imposed bias. Input-output match is better than 12 dB on the entire bandwidth.

Introduction

Research in the field of wideband amplifiers both for analog and digital applications cannot be only based on more and more advanced technologies, but also on novel and tested circuit topologies, to yield the best results from a consolidated technology. This approach leads to achieve cheap solutions together with high performances, and has been adopted for the present work. The chosen technology is in fact a consolidated 0.5 μm MESFET one, as supplied from Alenia, and with low-noise features. From the application side, faster and faster signal processing techniques are actually demanding very wide band linear amplifiers: in particular, the handling of fast digital traffic [1], video amplifier applications such as radar or wideband analog communication systems, optical fibers communications are only a few examples of utilisation of wideband linear amplifiers. In the present case, the target application is in nuclear physics particle detection, a field in which fast electronics is nowadays compulsory [2].
An improved ultra-wideband pulse amplifier characterized by a 3dB bandwidth of 5.5 GHz from quasi-DC, with a bias-controlled dynamic gain from 5 to 18 dB is presented in this contribution.

Circuit topology

The amplifier, whose schematic is shown in Fig.1, is composed by a cascade of a non-inverting gain stage, also performing input matching to 50 Ω, a source-coupled stage with a compensation loop based on inductive peaking, and finally an output buffer with the same compensating network.

The further requirement of a more general-purpose usage of the amplifier for different pulse applications both in analog communications and digital links has yielded to simplify the bias network respect to previous approaches [3, 4, 5]: self-biasing MESFET's and simplified compensating networks with enhanced performance have allowed the usage of a single positive supply.

As it can be noted from Fig.1, high frequency compensation is performed by means of a LC positive feedback loop. The voltage drop across a spiral inductor, inserted between MESFET's drain and bias, is connected in-phase to the signal path, through a series capacitance. In this way the intrinsic gain roll-off of the amplifier is equalised by a pole-zero compensation, while another pole is inserted at a higher frequency. A schematic circuit for this type of compensation is shown in Fig.2. The gain of the complete circuit is therefore the sum of a source-follower transfer function with an inductive load on the drain, and a one zero-one pole function, where the pole frequency is much higher than the frequency of the amplifier's dominant pole. Moreover, the gain of the compensating function is modulated by a RC high-pass filter, and inverted to add in-phase to the signal. By mean of the resistor R, the high-pass filter cutoff frequency can be changed and the compensation level controlled, especially in the output stage, where a compromise between gain flatness and return loss is necessary. The series inductor is realised by means of a spiral inductor, but the external bonding wires, necessary for the final package, can be taken into account in the compensation scheme. No internal RF-filtering capacitors have been inserted in the amplifier: microstrip supply lines have been connected to the bias via an external planar ceramic capacitor by means of bonding wires. In this way, no degenerative effect due to the package is introduced in the overall amplifier's performance.

Measured results

The layout of the resulting amplifier is plotted in Fig.3, featuring reduced size: 1.1 x 1.4mm^2 excluding the coplanar test probes.

The gain behaviour *vs* frequency is presented in Fig.4. The different curves show the amplifier's response for a bias supply varying in the range 4.5-8 Volts, with a corresponding power consumption ranging from 400 to 850 mW. It is to note that the same bandwidth for different gain levels has been achieved.

Input and ouput return loss are plotted in Fig.5. It can be noted that output return loss increases at higher

frequencies, i.e. when the frequency compensation is effective.

The compensation control through the resistor R (fig.1) can be seen in Fig.6: enhanced gain flatness and a lower insertion loss can be achieved.

In order to perform pulse measurements, very fast rise time input pulses have been constructed by means of the TDR (time-domain reflectometer) outputs of a TEK11802 digitizing sampling oscilloscope (see Fig.7): a step with a 15ps rise time from one output has been added to a 500 ps delayed step with the same fall time from the other output. The resulting square pulse has been both sent to the input of the oscilloscope ad to the amplifier input to characterize the output response so obtaining the amplitude ratio, the time delay and the rise and fall times as squared root differences between measured output and input rise/fall times.
The results of the above measurements are plotted in Fig.8, for two different biases (5 and 8 V, fig.8b and 8c respectively): the rise time of the amplifier, deducted from such curves ranges from 55 to 65ps, so confirming the validity of the proposed approach.

Conclusions

Novel topological schemes have been introduced for the design of a single-bias monolithic MESFET pulse amplifier. Such design choices resulted in an improved design featuring improved performances, reduced chip size, ease of handling and bonding all using a consolidated and mature 0.5µm technology. Notable measured performances include broadband operation from quasi-DC to 5.5 GHz, variable gain from 18 to 5 dB depending on the bias and an input and output match better than 12 dB all over the bandwidth. Rise and fall times are close to 50ps.

References

[1] F.Giannini, "MMIC solutions for multigigabit-per-second optical preamplifiers," Proceedings of the 21th European Microwave Conference, Stuttgard, pp.40-51.

[2] F.Giannini, G.Orengo, G.Paoluzi, P.F.Magrini, "Multiproject array of GaAs MMIC front-end amplifiers for detection in accelerator physics," Proceedings of the European Gallium Arsenide Application Symposium, Torino, April 1994, pp.77-80.

[3] F.Giannini, E.Limiti, G.Orengo, "Monolithic GaAs Ultra Wide Band Amplifier For Pulse Applications," Electronics Letters, N°19, September 14th 1995, Vol.31, pp.1698-1699.

[4] A.A.Abidi, "On the operation of cascode gain stages," IEEE Journal of Solid-State Circuits, Vol.23, N°6, December 1993, pp.1434-1437.

[5] A.Armstrong, H.J.Wagner, "A 5 V p-p 100 ps GaAs pulse amplifier IC with improved pulse fidelity," IEEE Journal of Solid-State Circuits, Vol.27, N°10, October 1992, pp.1476-1481.

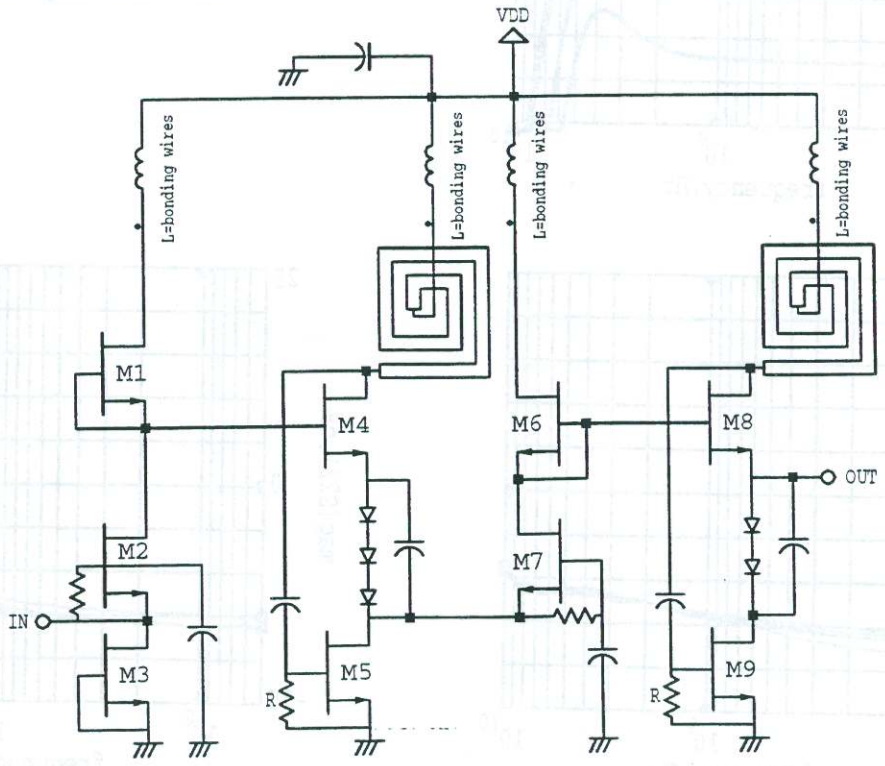


Fig.1: The schematic of the pulse amplifier

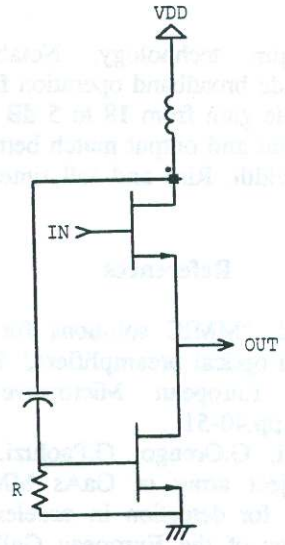


Fig.2:Principle of the high-frequency compensation scheme

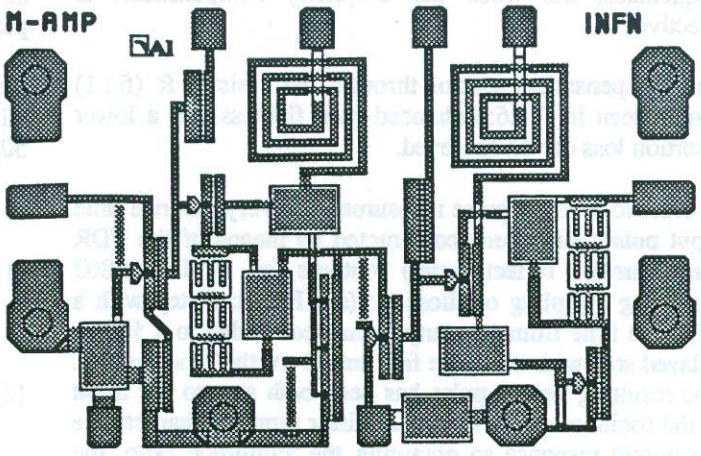


Fig.3: Layout of the complete amplifier (1.1 x 1.4 mm^2)

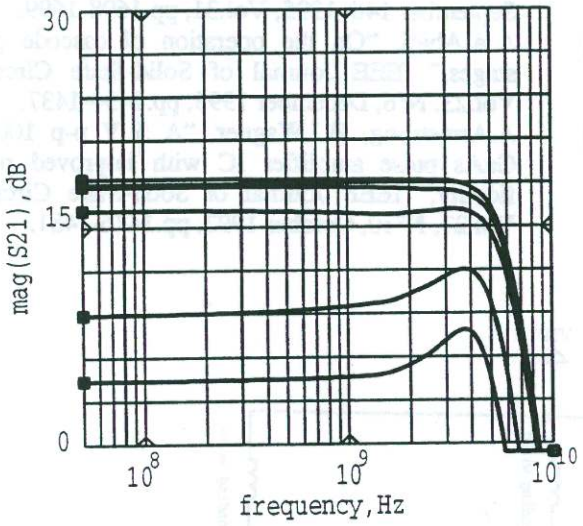
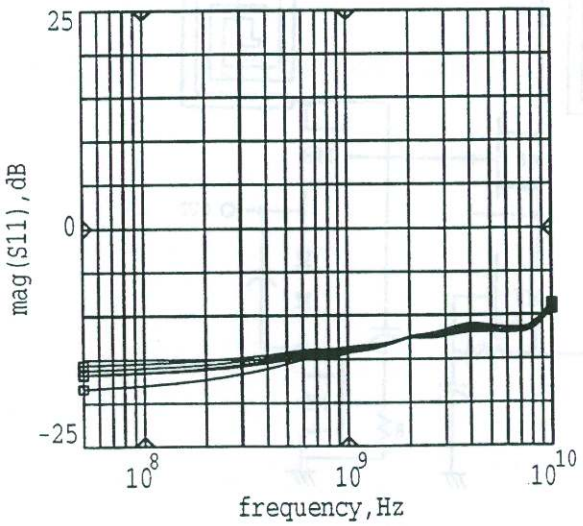


Fig.4: Amplifier's Gain vs frequency for different chip biases



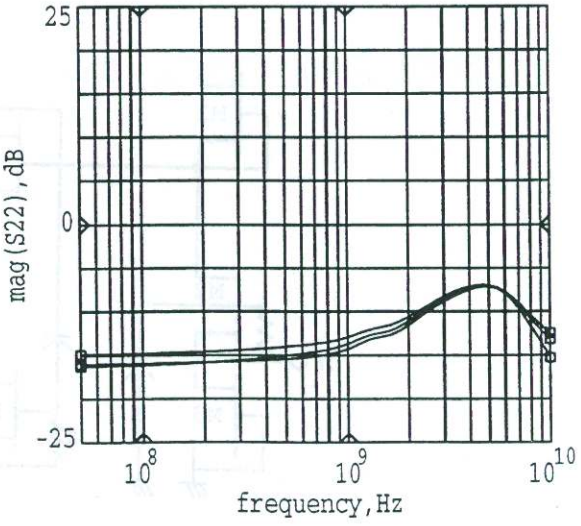


Fig.5: Amplifier's input (left) and output (right) match for different chip biases

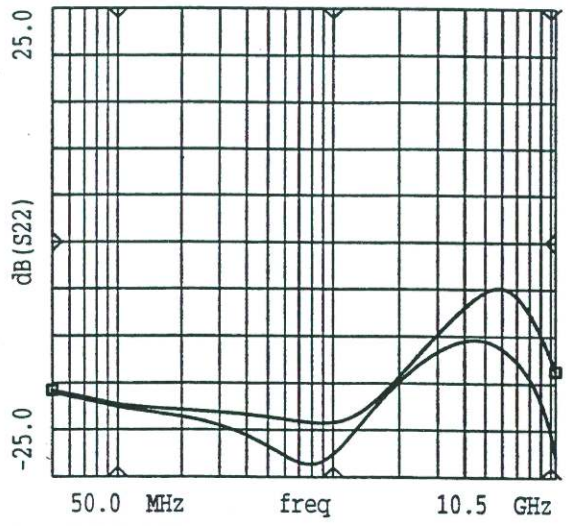


Fig.6: Effect of the resistive compensation

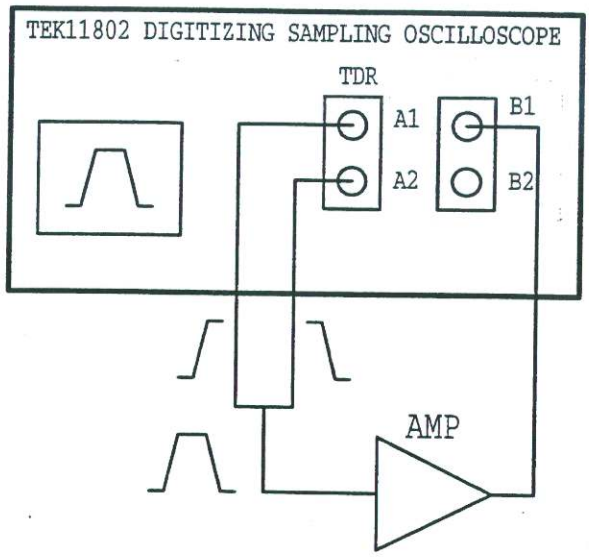
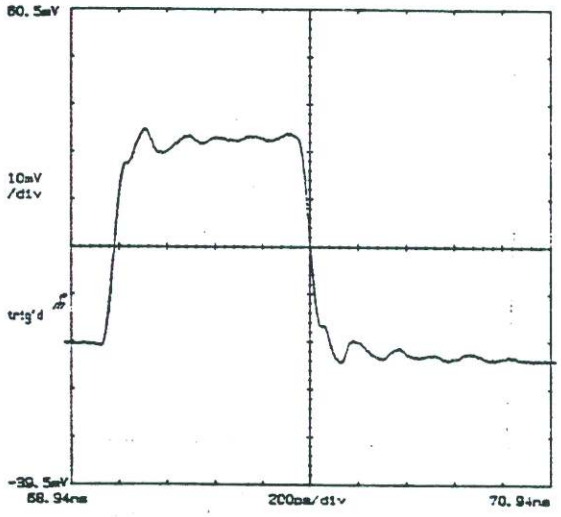
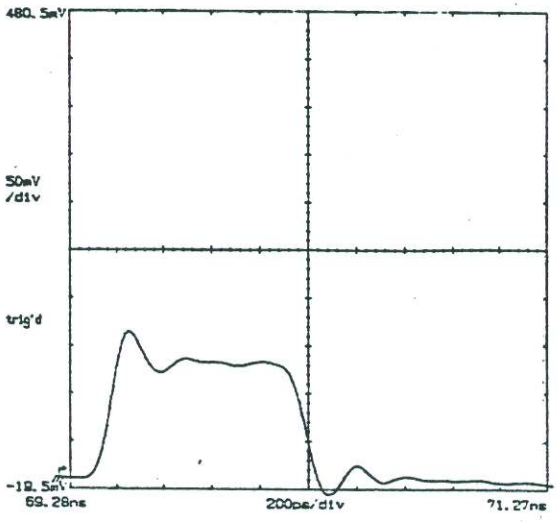


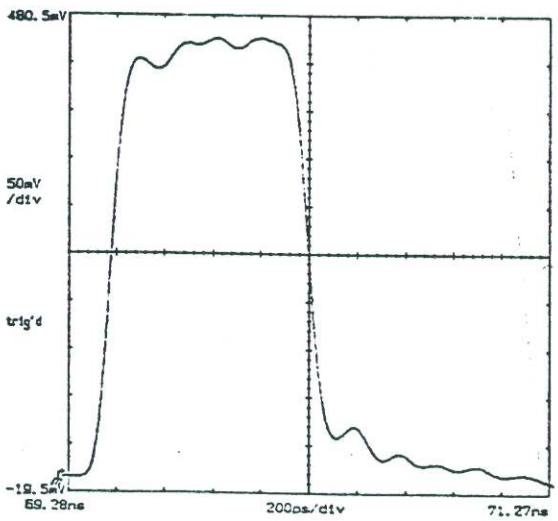
Fig.7: Pulse measurement setup



(a)



(b)



(c)

Fig.8: Response of the amplifier to an input pulse (a) for a bias level of 5 V (b) and 8 V (c)