Reduced Short Channel Effects In Selectively Dry Gate Recessed P-Doped Buffered Pseudomorphic HEMTs

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Abstract

We report both on the design by numerical simulation of pseudomorphic HEMTs with p-doped and undoped buffer layers and on their fabrication. We report that the p-buffer helps to reduce short channel effects in scaled 100 nm devices. To the authors' knowledge this is the first time that the application of p-doped buffer layers to HEMTs has been demonstrated.

Introduction

The development of mm-wave integrated circuits (MMICs) operating at frequencies of 100 GHz and beyond requires the introduction of fully scaled high elecron mobility transistors (HEMTs) with gate lengths of 100 nm or less. Transistors at this gate length typically exhibit short channel effects, due either to punch through of the drain field (or drain induced barrier lowering), or to de-confinement of hot electrons, or to a combination of both these factors. At dc short channel effects are manifest by increased output conductance and large negative shift in threshold voltage compared to long gate length devices. At mm-wave frequencies these effects can critically affect gate/source and gate/drain capacitance, transconductance and output conductance, all of which are key parameters in determining high frequency performance, particularly the cut-off frequency.

P-doped buffer layers have been widely applied to GaAs MESFETs but their application to pseudomorphic InGaAs/AlGaAs/GaAs HEMTs (pmHEMTs) has not been demonstrated previously. Typically undoped GaAs buffers are used to provide a confining step potential below the InGaAs channel. To increase the step potential AlGaAs buffer layers or GaAs/AlGaAs or GaAs/AlAs superlattice buffers have been widely applied. Such structures can be effective in confining hot electrons to the channel; for example, Thayne et.al proposed that mini-gaps in the GaAs/AlAs superlattice provide an effective barrier to electrons with energies up to 0.6eV.[1]

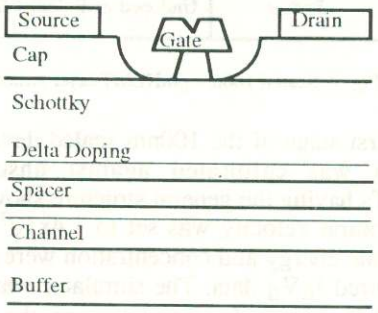

Fig. 1. General pseudomorphic HEMT layer structure.

We report here that the p-doped GaAs buffer also provides a confining step potential to hot electrons and in addition by reducing the electrostatic drain control on carriers in the channel offers a further mechanism by which short channel effects may be controlled. We also show that the p-buffer does not add unwanted parallel conduction or additional capacitance to the pseudomorphic layer. This type of buffer avoids the need to grow the InGaAs channel directly on an AlGaAs layer (for example) which can degrade the quality of the channel.

Systematic Design of pmHEMTs

We applied a systematic approach to the design of a 100 nm pmHEMT using full scale 2D device simulation with a finite element compound device simulator called H2F.[2] H2F is a 'classical' steady-state simulator which self-consistently solves Poissons' and the current continuity equations in a drift-diffusion approximation. The simulator permits device parasitics, such as source and drain resistance, to be included accurately and much attention has been paid to the proper handling of surface effects. The solution of Poisson's equation includes the space above the semiconductor surface providing for proper interaction between charge on the surface states and the spreading surface potential. The simulator uses a generalised surface trap model that allows for both acceptor and donor like traps whose enegy level can be set and whose occupation depends on both the quasi-fermi level and surface potential variation.

Although H2F is a serial code, a universal pipeline fileserver has been developed to run the program on a transputer system. Using this approach multiple copies of the program can be run for different bias conditions to simultaneously calculate a set of IV characteristics.[3]

Cap	20nm n-GaAs
Schottky	25nm i-$Al_{0.3}Ga_{0.7}As$
Delta doping	Si : $5x10^{12}$ cm^{-2}
Spacer	5nm i-$Al_{0.3}Ga_{0.7}As$
Channel	10nm i-$In_{0.3}Ga_{0.7}As$
Buffer	Undoped or P-doped GaAs

Fig. 2. Scaled 100nm pmHEMT layer structure..

For the first stage of the 100nm scaled device design the simulator was calibrated against unscaled 200nm pmHEMTs having the general structure shown in figure 1. The saturation velocity was set to $1.4x10^7$ cm/s and the surface state energy and concentration were adjusted to fit the measured I_dV_d data. The simulator was then used to predict the output characteristics as the gate-channel spacing and delta-doping concentration were scaled to find the optimum layer design.

The design procedure resulted in the layer structure shown in figure 2; the I_dV_d characteristics calculated for 100nm pmHEMTs with undoped and p-doped buffer layers with this structure are compared in figure 3. It is apparent that

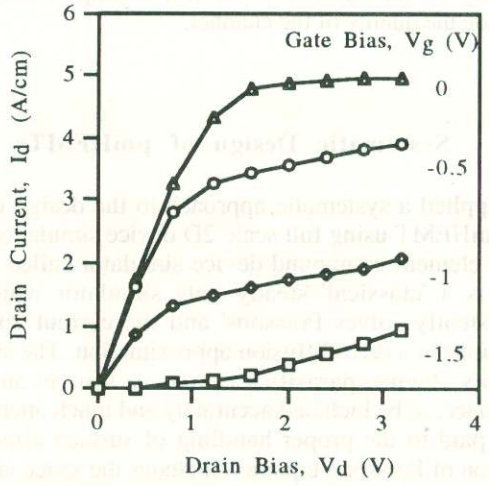

Fig. 3a. Calculated I_dV_d characteristic of a scaled 100nm pmHEMT with undoped GaAs buffer.

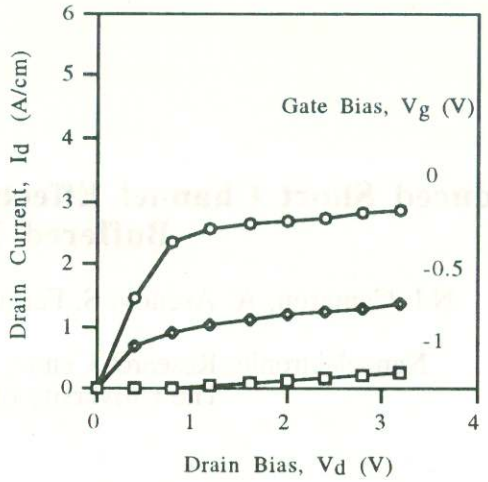

Fig. 3b. Calculated I_dV_d characteristic of a scaled 100nm pmHEMT with P-doped GaAs buffer.

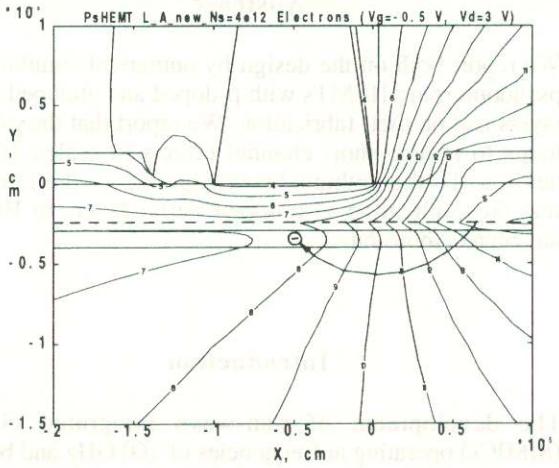

Fig. 4a. Potential distribution of a scaled 100nm pmHEMT with an undoped GaAs buffer, the drain field terminates on electrons in the channel. (Equi-potentials labelled 0-19 for -1.6 to 3.15 V step 0.25).

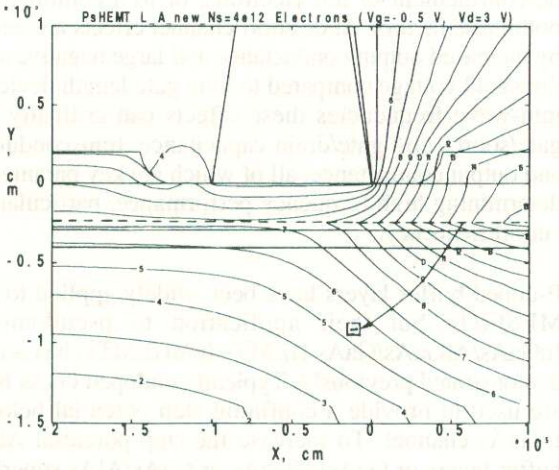

Fig. 4 b. Potential distribution of a scaled 100nm pmHEMT with a p-doped GaAs buffer, the drain field now terminates on ionised acceptors (Equi-potentials labelled 0-19 for -1.6 to 3.15 V step 0.25).

the undoped buffered device suffers from drain induced barrier lowering which is manifest by high output conductance and reduced transconductance particularly for large V_d. These effects are much reduced for the p-buffered device at the expense of reduced open channel drain current. The p-doped buffer plays several important roles : (i) it improves the carrier confinement, localising carriers close to the upper boundary of the InGaAs well and (ii) it reduces the hot carrier space transfer by providing a step potential

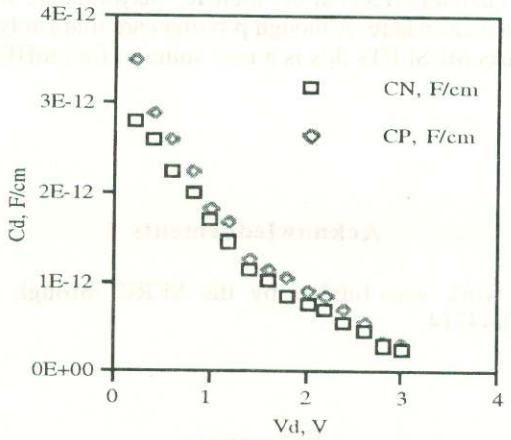

Fig. 5. Calculated drain capacitance for undoped (CN) and P-doped (CP) buffer layers.

which reflects electrons back into the channel and (iii) it reduces the lateral electrostatic drain control on the carriers in the channel, because, as shown in figure 4, the drain field now terminates on ionised acceptors in the p-buffer rather than on electrons in the channel. If the buffer acceptor concentration is properly designed the p-buffer does not critically affect gate-source and gate-drain capacitances, figure 5.

Scaled pmHEMT Fabrication

Devices were fabricated on the layers shown in figure 2 with both p-doped and undoped GaAs buffers. All levels were written by electron beam lithography using a Leica-Cambridge EBPG-5HR or Beamwriter. The process comprised : registration marks; ohmic contacts having <0.1 Ωmm contact resistance and 1 μm seperation between source and drain; wet etched mesa isolation; a selectively dry etched gate recess and mushroom shape gate with a range of gate lengths from 125nm to 345nm; and a final wiring level for on wafer probing. The selective dry gate recess etch process has been described elsewhere.[4,5] Threshold voltage uniformity as good as 1σ = 10 mV was obtained for 250nm undoped buffered devices. The gate recess depth is fixed at the interface between the GaAs cap and the AlGaAs Schottky layer and unlike a wet etched recess is independent of gate length. The gate length was measured by SEM. The aspect ratio of gate length to gate-channel spacing was therefore accurately known, allowing a systematic study of short channel effects to be made.

Short Channel Effects

Threshold voltage and subthreshold current were studied to examine the influence of the p-doped buffer layer on short channel effects. The result of the threshold voltage study is shown in figure 6. The p-doped buffer is highly effective, particularly at low drain bias, in reducing the large negative shift in threshold voltage observed for the undoped buffered pmHEMTs. At V_d=0.25V the threshold voltage shift from 255nm to 125nm is -0.795 V for the undoped buffered devices and only -0.288 V for the p-buffered HEMTs.

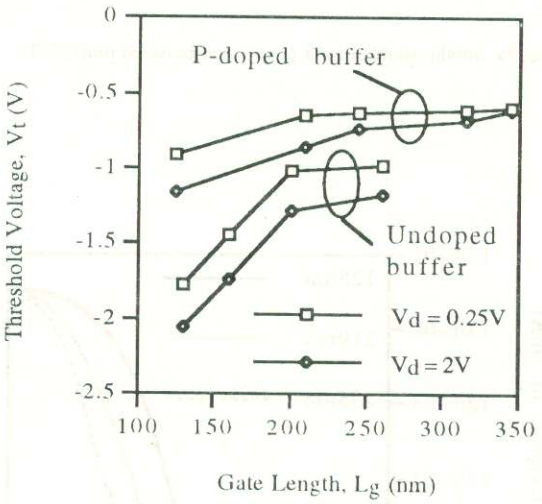

Fig. 6. Threshold voltage of undoped and p-doped buffered pmHEMTs.

Subthreshold current is shown in figure 7. Similar behaviour is observed for devices with 200nm and longer gates with both types of buffer. At 125nm larger subthreshold current is observed for the undoped buffered device indicating the onset of drain induced barrier lowering. Below subthreshold an interesting difference in the characteristics of the differently buffered devices is observed. In the p-buffered HEMTs I_d increases below pinch off while no such increase is observed for undoped buffered devices. When the p-buffered HEMT is pinched off, the depletion regions extending from the gate and buffer merge which may allow the applied gate potential to lower the barrier between the gate and the p-buffer. The gate, p-buffer and drain could then be considered as

a camel or npn diode, where the gate/p-buffer junction is forward biased and the drain/p-buffer is reverse biased.

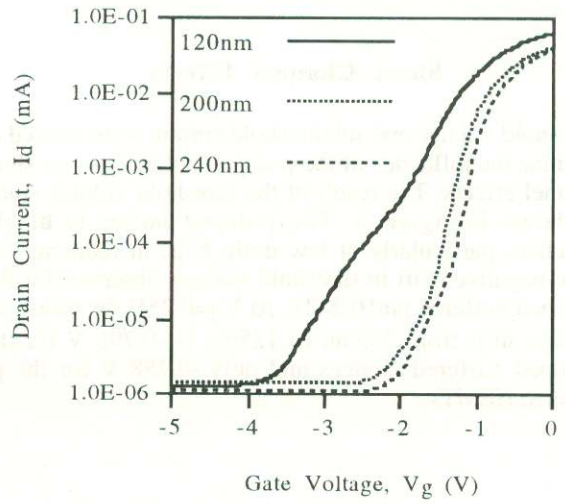

Fig. 7a. Subthreshold current in undoped buffered pmHEMTs.

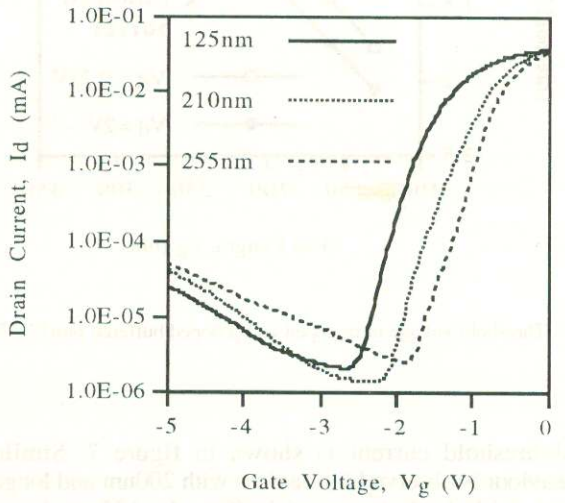

Fig. 7b. Subthreshold current in P-doped buffered pmHEMTs.

Conclusions

We have shown that proper scaling of pseudomorphic HEMTs requires not only a reduction of the separation between the channel and gate but also the introduction of a p-doped buffer layer below the channel to reduce the electrostatic drain control of electrons in the channel. Devices with p-doped buffer layers show much reduced short channel effects at dc; their RF performance will be reported elsewhere. Although p-buffers are frequently used in GaAs MESFETs this is a new solution for pmHEMTs.

Acknowledgements

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References

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