High-power and high-efficiency ion-implanted GaAs MESFETs with buried p-layer

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Abstract

High-power and high efficiency GaAs power MESFETs have been developed using a Carbon co-implantation technique.The active channel layer is realized by multiple Silicon implantation with and without Carbon co-implantation in the tail region of the Si donor distribution. Measurements performed on a 4 Watt power devices in the 5.9÷6.4 GHz band show typical P.A.E of 29% with an intercept point of 47.8 dBm in class A operation compared to the values of 22% and 46.5 dBm of the same devices realized without any p-buried layer.

Introduction

As shown in various computer-aided analysis and in further experimental studies, the introduction of a buried p-layer at the backside of the donor implant on the semi-insulating substrate is effective to reduce short-channel effects and to improve the DC transfer characteristic linearity and the drain efficiency [1-3]. To create p-type implanted layers in semi-insulating GaAs the more common acceptor species are Beryllium and Magnesium. Probably because of the low activation efficiency that Carbon (C) seemed to show since the earlier reports, it has been seldom employed [4-6], although C presents the advantage of a diffusion coefficient some orders of magnitude lower than the other acceptor species and a low amphoteric behaviour, as it has been confirmed in various studies on C implants, where the question of the possible compensating species,responsible of the lower activations, is still open [7-9]. Furthermore the low atomic mass together with the availability from gaseous sources and the non-toxicity make attractive the use of C. We have investigated the behaviour of C both in semi-insulating GaAs and co-implanted with Silicon (Si) to form a buried p-layer and compensate the tail of Si-implant, since C activation strongly depends on post-implant thermal treatment we have developed a proper capless thermal annealing capable to get good activation for both the implanted species Si and C. The developed channel structures with and without C co-implant have been used to fabricate high-power devices. In this paper the comparison of the electrical performances,both DC and RF,is given to show the improvements obtained introducing the C co-implant in terms of Power Added Efficiency (P.A.E.) and linearity, thanks to the better carrier confinement and suppression of substrate leakage current. At this purpose a complete on-wafer Load-Pull characterization over the whole C-band has been performed on MESFETs devices having 1.2 mm total gate width. Moreover,internally matched devices,using a 12 mm gate width chips, have been characterized in the 5.9÷6.4 GHz band.

Device fabrication and structure

The starting substrates are 2-inch undoped LEC semi-insulating GaAs wafers. The n-type channel layer is realized by multiple Si implantation at different energies and doses, the obtained peak carrier concentration is 1.6x10E17 cm^{-3}. The buried p-layer at the backside of the donor implant is formed by a single C implant, whose energy and dose have been optimized to considerably increase the maximum slope of the carrier profile without modifying the peak carrier concentration in the channel. Capless post-implant thermal annealing is performed in arsenic overpressure using a hot wll type reactor: annealing time and temperature were previously adjusted in order to get the best activation at 870°C for 10 minutes.

The developed power MESFET has 0.6x120μm single gate fingers, 12 mm total gate width and chip size of 0.62x2.230mm^2. The top view of this device is shown in Fig. 1. It consists of ten unit cells, each cell having ten gate fingers, one drain and one gate pad with two source pads. The gate to gate spacing (16.4μm) and the unit gate width (120μm) have been determined on the basis of experimental data in order to have low thermal resistance and enough gain up to 8GHz. The unit cell number, compatibly with gate and source pad dimensions, has been chosen in order to reduce gain losses due to the phase delay of too long gate bus line. The chip is thinned to 30μm and backside processed with P.H.S. technology for thermal improvement and for handling. A scaled MESFET device, having 1.2mm total gate width and the same layout structure of the above described power device, has been used to perform on-wafer Load-Pull characterization, its top view is shown in Fig. 2. The source and drain ohmic contacts and gate electrodes are defined by conventional photolithography and lift-off process.

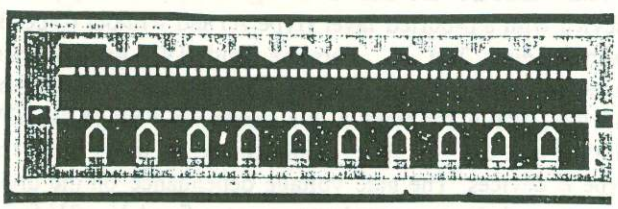

Fig. 1 - 12mm chip

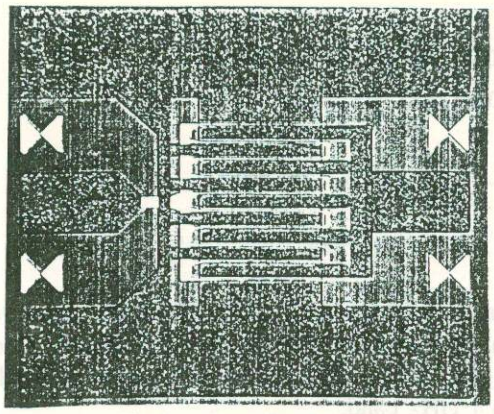

Fig. 2 - 1.2mm Test Pattern

Plated air bridge connections among source pads are used to reduce parasitic source inductance. Via holes source grounding technology is also available for higher frequency application.

The active layer carrier concentration profiles determined by capacitance-voltage technique for the same multiple Si implant with and without C co-implant are shown in Fig. 3. It is seen that C co-implantation significantly improves the abruptness of carrier concentration , this results effective in reducing substrate current and improving transconductance, as described elsewhere. Peak carrier concentration remains almost the same for wafers having the same multiple Si implant, proving that the C co-implantation can steepen the the tail of the carrier profile without reducing the concentration in the channel. Moreover mobility values are not heavily affected by the introduction of the C co-implant, they are respectively about 3600 cm^2 / V s for the channel structure having the buried p-layer and about 3950 cm^2 / V s for that without it. After mesa isolation and ohmic contact alloying, the saturated drain-source current I_{dss0} is approximitly ~600mA/mm for channel structure with C co-implant and ~720mA/mm without C co-implant due to the different sheet resistance of ~540Ω/□ and of ~420Ω/□ respectively. For the above explained reasons this decrease is mainly due to the different maximum slope of the two carrier profiles. Great attention has been paied to the optimization of gate recess depth accordingly with the doping profile and the two channel structures have been recessed to the same final current.

DC Performances

The measured drain I-V characteristics of the 1.2 mm gate width MESFET are shown in figure 4(a) and 4(b) for a device with a p-buried layer (type A) and without (type B) respectively. The I_{dss} currents and DC gate-to-drain breakdown voltage are about the same for both the devices, while for type A the threshold voltage is 0.2V higher and the DC drain conductance is lower than the type B devices. The gate voltage dependance on the drain current and the transconductance at a fixed V_{ds}=3V,for a 200μm MESFET, are shown in figure 5. The pinch-off characteristics are better for type A MESFET in the sub-threshold region.

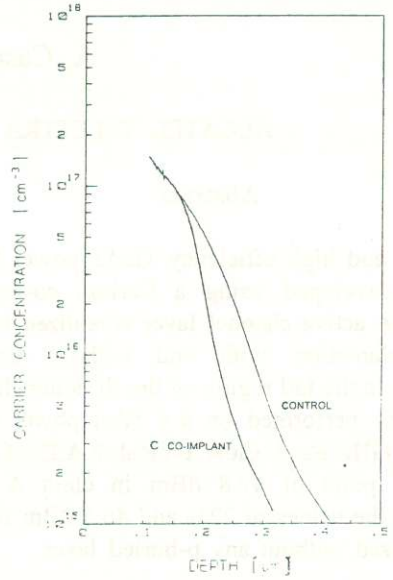

Fig. 3 - Carrier concentration profiles with and without C co-implant

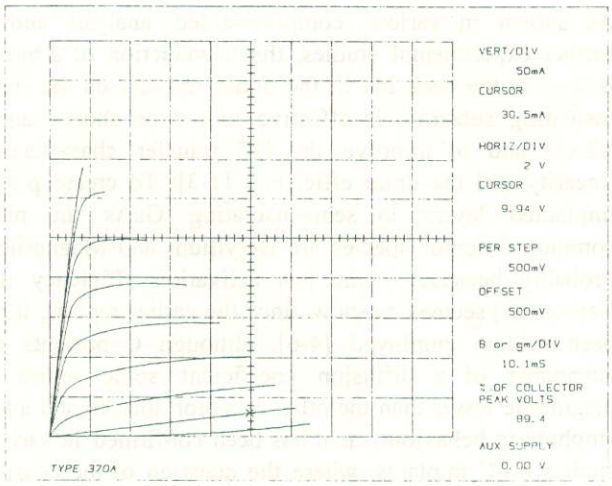

Fig. 4(a) - Type A 1.2mm DC I-V curves

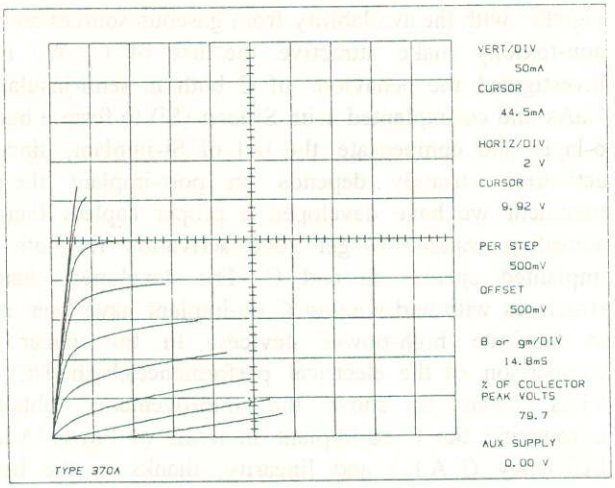

Fig. 4(b) -Type B 1.2mm DC I-V curves

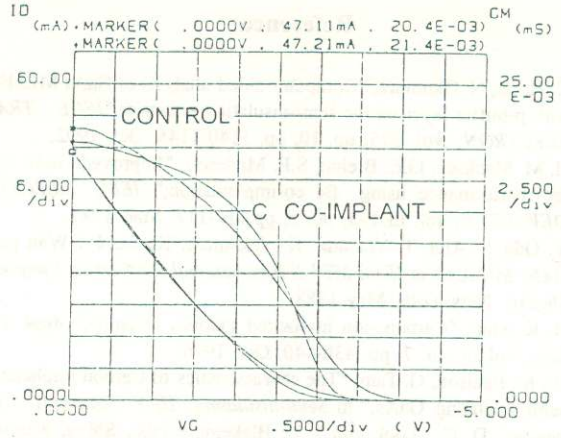

Fig. 5 - I_{ds} and g_m v.s. V_{gs} at V_{ds}=3V for 200μm MESFET

RF Performances

The 1.2 mm type A and type B thinned MESFETs have been on-wafer tested at the same bias conditions (V_{ds}=10V, $I_{ds}\approx I_{dss}/2$), in C-band, from 4.4 to 7.2 GHz, via a Load-Pull test bench. In table 1, the mean values for the measured power (P_{1dB}),gain (G_{1dB}),current (I_{dsr}) and P.A.E. at 1dB gain compression, with tuned load for maximum P_{1dB}, for both type A and type B MESFETs are reported. As it can be seen, with the introduction of the buried p-layer a quite large improvement can be obtained in terms of P_{1dB},I_{dsr} and P.A.E.

A packaged internally matched device, with the 12mm chip from type A and type B channel structures, has been developed. The matching circuits have been projected to work in the 5.9÷6.4 GHz band. The input/output WSWR requirements for the 12.3% band, have led to a double L-C ladder lumped low-pass network with an high dielectric costant (ε_r=80) for the input while a 25Mils Alumina substrate single distribute network for the output. In table 2, the measured performances of type A and type B 4 watt power MESFETs are reported. Better performances are obtained for type A in terms of P.A.E. and 3rd order intermodulation distorsion produdts (IM_3). The improvement tipically pass, over the band,from 22% to 29% for P.A.E. while from -43dBc to -45.6dBc for IM_3 and this means an improvement of the intercept point value from 46.5dBm to 47.8dBm for class A operation.

Table 1 : 1.2mm MESFETs performances
at V_{ds}=10V I_{ds}=143.5mA

Freq.	Item	Type B	Type A
4.4GHz	P_{1dB} [dBm]	27.1	28.2
	G_{1dB} [dB]	12.9	12.8
	I_{dsr} [mA]	174	167
	P.A.E. [%]	28	38
5.0GHz	P_{1dB} [dBm]	27.2	28.2
	G_{1dB} [dB]	12	12.1
	I_{dsr} [mA]	174.3	169.5
	P.A.E. [%]	28.4	36.6
5.9GHz	P_{1dB} [dBm]	27.4	28.2
	G_{1dB} [dB]	11.1	10.9
	I_{dsr} [mA]	171	163.6
	P.A.E. [%]	30.1	37.2
6.4GHz	P_{1dB} [dBm]	27.4	28.2
	G_{1dB} [dB]	10.3	10
	I_{dsr} [mA]	170.5	163.2
	P.A.E. [%]	29.6	37
7.2GHz	P_{1dB} [dBm]	27.5	28.3
	G_{1dB} [dB]	9.3	9.17
	I_{dsr} [mA]	168.8	163.8
	P.A.E. [%]	29.3	36.1

Table 2 : 4 watt MESFETs performances
at V_{ds}=10V , I_{ds}=1.4A
*[P_{out}=25dBm S.C.L. Δf=10MHz]

Frequency	Item	Type B	Type A
5.9GHz	P_{1dB} [dBm]	37.2	37.4
	G_{1dB} [dB]	8.5	8.5
	P.A.E. [%]	23.7	31.5
	IM_3 [dBc] *	- 41.1	- 45.2
6.15GHz	P_{1dB} [dBm]	37.1	37.3
	G_{1dB} [dB]	8.4	8.4
	P.A.E. [%]	23.2	30.6
	IM_3 [dBc] *	- 42.7	- 46.4
6.4GHz	P_{1dB} [dBm]	36.3	36.2
	G_{1dB} [dB]	8.3	8.3
	P.A.E. [%]	19.5	24.3
	IM_3 [dBc] *	- 45	- 45.4

Conclusions

The developed channel structure using C co-implantation technique, has been demonstrated effective to reduce short-channel effects and to improve DC transfer characteristic linearity.

1.2mm gate-width devices fabricated with the developed channel structure having the buried p-layer, efficiently characterized via a Load-Pull test bench, over the C-band, have shown P_{1dB} and P.A.E. values higher than the corresponding devices without buried p-layer.

The comparison between internally matched 4 Watt MESFETs on 5.9÷6.4 GHz band, fabricated with and without the buried p-layer, has shown an increase of P.A.E. and intercept point values for the buried p-layer.

The new developed buried p-layer channel structure is suitable for high-power, high-efficiency commercial devices.

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