

A monolithic HEMT distributed amplifier using a low cost spacer technology

Heinz J. Siweris, Thomas Grave, Lothar Schleicher

Siemens AG, Corporate Research and Development
Munich, Germany

Abstract

The design, fabrication, and performance of a monolithic HEMT distributed amplifier are described. Over the 0.5 - 30 GHz frequency range a gain of 9.5 ± 0.7 dB has been achieved. The HEMT gate process is based on a spacer technology without using electron beam lithography. Thus, the process is suitable for high volume low cost production of HEMT MMICs.

Introduction

The distributed amplifier offers flat gain and good return loss over multi-octave bandwidths and thus is a key element for broadband microwave systems. In conjunction with monolithic HEMT technologies, amplifier circuits with operating frequencies up to 100 GHz have been demonstrated, e.g. [1-3]. However, up to now all MMICs of this type rely on electron beam lithography for the critical definition of the gate structure. This expensive technique prevents a low cost fabrication and widespread use of HEMT MMICs.

In this paper we present a monolithic distributed amplifier fabricated by a HEMT technology which makes use of optical lithography for all processing steps including the gate formation. As a result, a significant reduction of fabrication costs can be expected making this MMIC a candidate for a general purpose microwave amplifier not only for broadband applications.

Technology

The process technology is based on 3-inch-wafers with a pseudomorphic AlGaAs/InGaAs/AlGaAs single quantum well layer sequence formed by molecular beam epitaxy. The active devices are isolated by boron damage implantation. Optical lithography by an I-line wafer stepper is used throughout the whole process. Since the minimum line width of the stepper is approximately $0.5 \mu\text{m}$, a special spacer technique is applied to fabricate refractory-metal gates of $0.25 \mu\text{m}$ length. The gates are subsequently reinforced by a low resistivity overlay metal. Fig. 1 shows a schematic cross section of the HEMT device. The gate is placed within a double-recess structure with nonequal distances to the source and drain metals, respectively. These features yield a high gate-to-drain breakdown

voltage and enable medium output power levels of the device with only a slight degradation of the noise performance compared to devices with completely self-aligned contacts. The measured minimum noise figure of these HEMTs was 0.9 dB at 12 GHz, the maximum current gain cut-off frequency is approximately 60 GHz.

The complete MMIC process includes MIM capacitors, precision thin film resistors, air bridges, and via holes. After completion of the front side process the wafers are thinned to a final thickness of $100 \mu\text{m}$.

Circuit design

Fig. 2 shows a schematic diagram of the HEMT MMIC. The distributed amplifier consists of six identical stages each with a HEMT device of $80 \mu\text{m}$ gate width. The drain nodes of the HEMTs are loaded by small MIM capacitors to increase the stability of the circuit. This is necessary since the dielectric spacers lead to a relatively high gate-to-drain capacitance of the active devices making it difficult to achieve high gain and stability simultaneously. The gate transmission line is terminated by a single resistor, whereas the drain line ends in a resistor-capacitor network. All network elements were optimized using a linear circuit simulation program.

A photograph of a fabricated amplifier is shown in Fig. 3. Each HEMT has two gate fingers of $40 \mu\text{m}$ width. The source nodes are grounded by via holes. The transmission lines are realized as microstrip sections. The input and output pads are arranged in a ground-signal-ground configuration to facilitate RF on-wafer measurements. The dimensions of the chip are $1.2 \text{ mm} \times 2.8 \text{ mm}$.

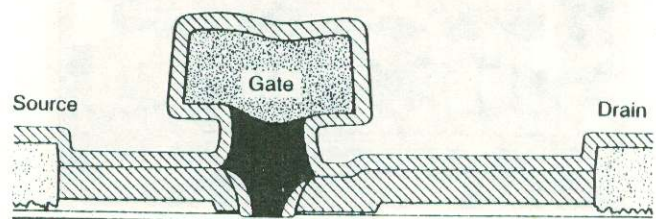


Fig. 1. Schematic cross section of the HEMT device.

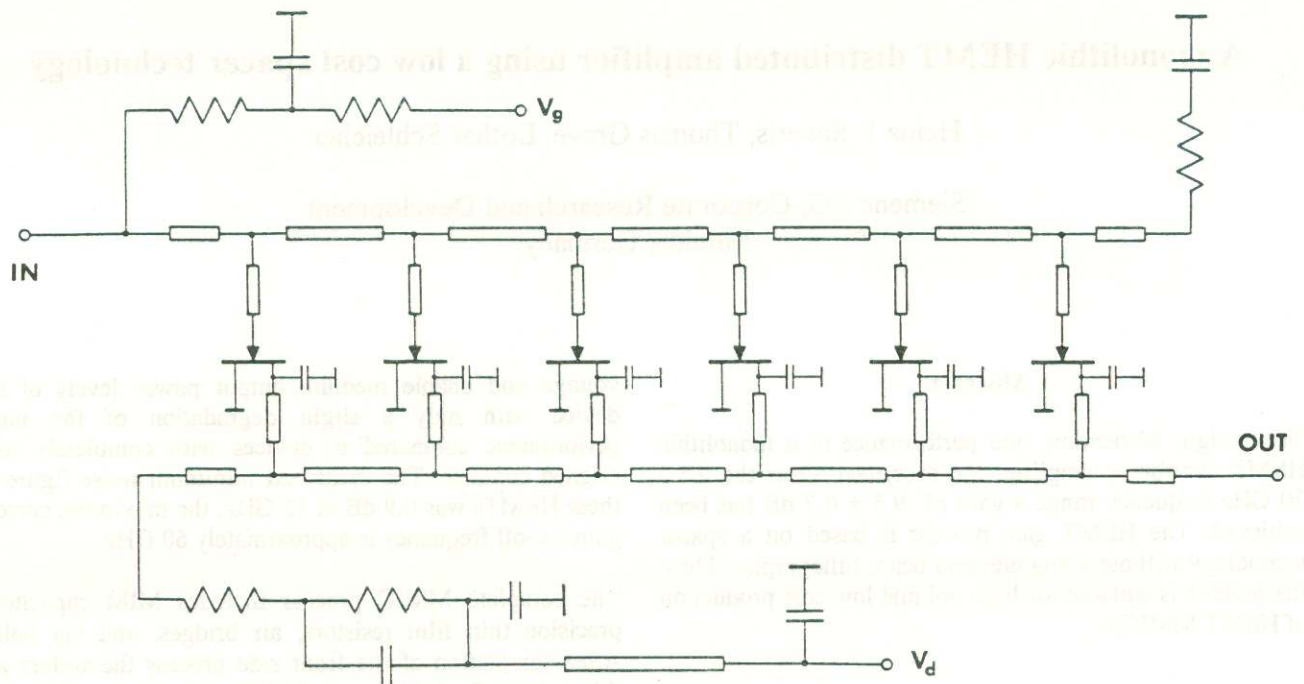


Fig. 2. Schematic diagram of the distributed amplifier

Measurement results

The amplifier was characterized by on-wafer measurements of the S- and noise parameters. A first observation during the measurements was that, in spite of a high DC yield, the RF measurements were frequently corrupted by spurious oscillations. The reason for these problems is that the amplifier, due to the internal feedback capacitance of the HEMTs, had to be designed with a narrow stability margin in order to meet the gain and bandwidth objectives. Moreover, some improvements of the fabrication technology and, consequently, of the active device properties took place after the design was completed. These modifications, in conjunction with the normal spread of the process parameters, caused a relatively high number of amplifiers to oscillate, a problem which will be tackled within the next design.

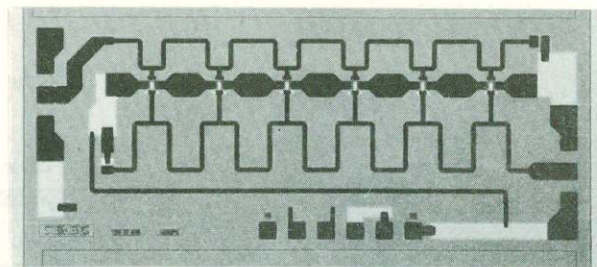


Fig. 3. Photograph of the monolithic HEMT distributed amplifier.

The results of a S-parameter measurement under stable operating conditions are summarized in Figs. 4 and 5. The circuit was biased at 5 V drain-to-source voltage and a total drain current of 95 mA. Fig. 4 shows that a gain of 9.5 ± 0.7 dB has been achieved over the 0.5 - 30 GHz frequency range. The input return loss is better than 10 dB in this frequency range (Fig. 5). The same holds for the output return loss, except for a slightly higher reflection at the upper end of the band.

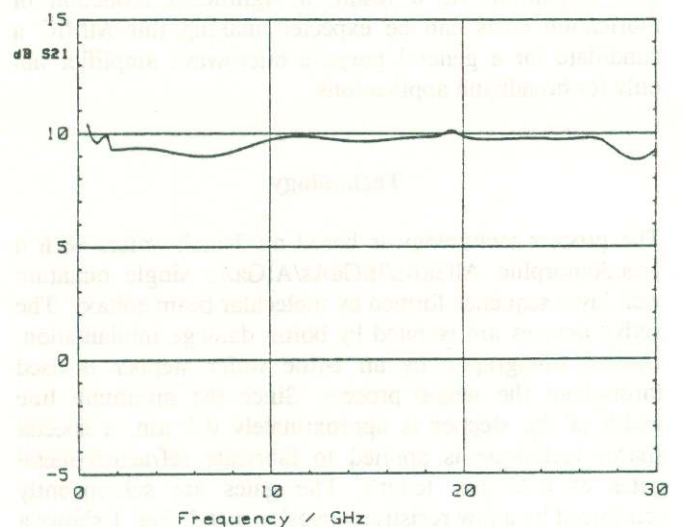


Fig. 4. Measured gain of the distributed amplifier.

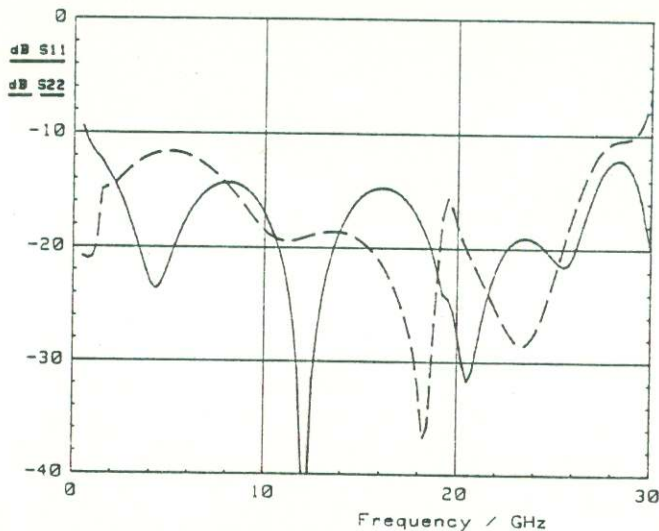


Fig. 5. Measured input (—) and output (---) return loss of the distributed amplifier.

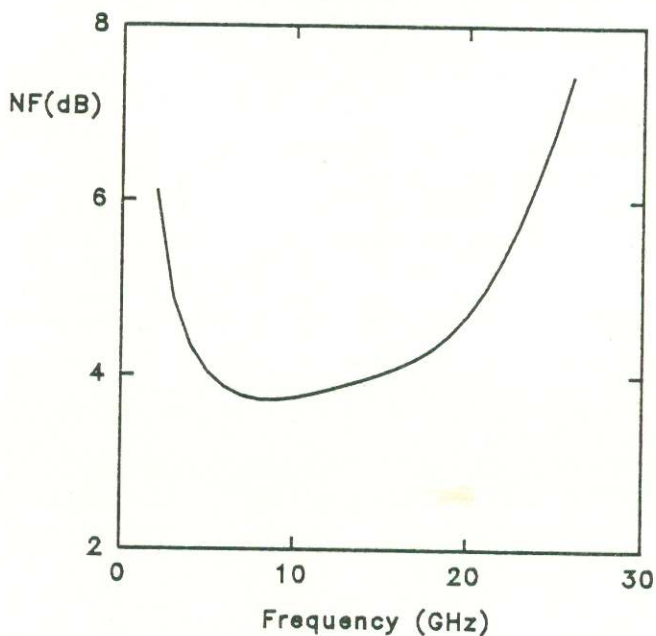


Fig. 6. Measured noise figure of the distributed amplifier.

Fig. 6 shows the measured noise figure of the amplifier in the frequency range 2 - 26 GHz. The total drain current was reduced to 60 mA for this measurement. The noise figure ranges from 3.7 dB to 7.4 dB with values below 5 dB in the frequency range 3 to 21 GHz. Due to the lower drain current, a reduced gain of 8.8 ± 0.4 dB was measured for this bias condition.

Conclusion

A monolithic HEMT distributed amplifier with 9.5 dB gain in the frequency range 0.5 - 30 GHz has been described. The MMIC was fabricated by a low cost production process without using electron beam lithography.

It turned out, however, that this combination of gain and bandwidth poses stability problems due to the internal feedback of the active devices. For the next design it is planned to use a cascode connection of two HEMTs in the sections of the distributed amplifier. This approach improves the reverse isolation, thus enhancing the stability and enabling a higher gain or a larger bandwidth of the amplifier.

Acknowledgements

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References

- [1] J. Perdomo, M. Mierzwinski, H. Kondoh, C. Li and T. Taylor, "A monolithic 0.5 to 50 GHz MODFET distributed amplifier with 6 dB gain," 1989 IEEE GaAs IC Symposium Technical Digest, pp. 91-94.
- [2] R. Majidi-Ahy et al., "5-100 GHz InP CPW MMIC 7-section distributed amplifier," 1990 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest, pp. 31-34.
- [3] J. Braunstein et al.: "Very broad band TWAs to 80 GHz on GaAs substrate," Proc. 23rd Europ. Microwave Conf., pp. 372- 373, 1993.