Power P-HEMT Realization on MOVPE Structures

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Abstract

The paper presents the fabrication of power P-HEMTs on epitaxial structures grown by low pressure MOVPE technology featuring a Si planar doped (δ doped) $Al_{0.22}GaAs$ supply layer. The use of such a doping technology whose great potential has already been demonstrated by MBE grown structures, has been successfully applied (to our knowledge) for the first time to P-HEMT devices realized by LP-MOVPE, showing substantially improved device characteristics.

Introduction

Pseudomorphic GaAs based HEMTs have emerged as the winning technology for advanced microwave and millimetre wave system applications due to their lower noise and higher efficiency and power than GaAs MESFETs and conventional lattice matched HEMTs in a wide range of frequencies, from C to W band.

Their realization predominantly rely on Molecular beam epitaxy (MBE) as growth technology, due to its high quality materials and excellent structural and doping control (see for example [1]).

However, Low Pressure Metallorganic Vapour Phase Epitaxy (LP-MOVPE) has recently achieved maturity and become a viable and economic growth technology for heterostructure devices including P-HEMTs.

We report on the growth of P-HEMT structures with a Si planar doped $Al_{0.22}GaAs$ supply layer and on the fabrication and characterization of power P-HEMT devices fabricated on these materials.

Planar doping in the AlGaAs supply layer of the HEMT structure is considered necessary to obtain higher current densities and transconductances than uniformly doped supply layers.

A fair amount of research has been done by LP-MOVPE on Si delta doped GaAs [2], but to our knowledge little or no effort has been done on AlGaAs.

Growth

We examined the growth aspects concerning the planar doping incorporation in $Al_{0.22}GaAs$ layers by studying the growth interruption time and SiH_4 partial pressure effects on the 2D electron concentration and its Full Width at Half Maximum (FWHM) as measured by C-V technique.

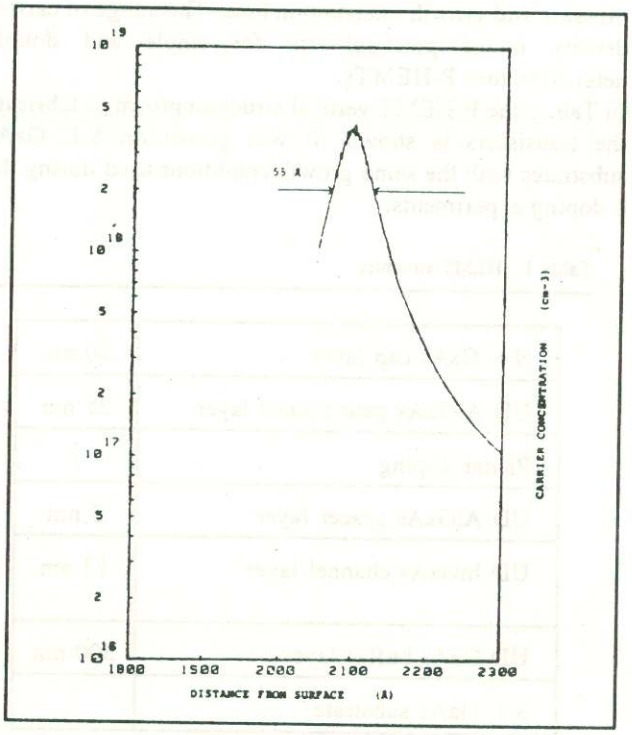

Fig.1 δ doped C-V profile for AlGaAs layer

The test samples were grown on n+ GaAs 2° off (100) towards (110) substrates in a horizontal LP-MOVPE reactor.

The reactant gases used were AsH_3, TMGa, TMAl and SiH_4 (1% in H2). The growth conditions for all the experiments were a temperature of 650 °C, a V/III ratio of 175 and a pressure of 20 mBar. An AsH_3 partial pressure of 2.3E-2 mBar was maintained during growth interruption.

The test structures consisted of 100 nm GaAs buffer layer/ 100 nm $Al_{0.22}GaAs$(i)/ δ doping/ 200 nm $Al_{0.22}GaAs$(i)/ 10 nm GaAs(i) cap layer.

The characterization of δ doped structures was undertaken by C-V technique and High Resolution X-Ray Diffractometry (HR-XRD) was used to check the crystalline quality.

The Si planar doping did not alter the crystal structure, as expected for the relatively low Si on group III surface coverage, calculated to be around 2.5% for a full Si activation.
A typical sharp C-V profile of a δ doped $Al_{0.22}GaAs$ layer is reported in Fig. 1. The FWHM of 5.5 nm corresponding to a N_{2D} of 3.6E12 cm-2, obtained by integrating the C-V curve, is in close agreement with the theoretical FWHM calculated from a self consistent solution of the Poisson and Schroedinger equations, assuming no Si diffusion. The profile shape does not change appreciably after several minutes of annealing under the same growth conditions.
2D carrier densities between 1E12 cm-2 and 3.6E12 cm-2 could be reproducibly obtained by adjusting SiH_4 partial pressure and growth interruption time. This range of carrier density is of practical use for single and double heterostructure P-HEMTs.
In Tab. 1 the P-HEMT vertical structure grown to fabricate the transistors is shown. It was grown on S.I. GaAs substrates with the same growth conditions used during the δ doping experiments.

Table 1 HEMT structure

N+ GaAs cap layer	50 nm
UD AlGaAs gate contact layer	25 nm
Planar doping	/
UD AlGaAs spacer layer	3 nm
UD InGaAs channel layer	13 nm
UD GaAs buffer layer	300 nm
S.I. GaAs substrate	

The δ doped layer was grown with conditions to obtain a carrier density of 3.5E12 cm-2.

Device fabrication

The vertical structure design and optimization was carried out on a monodimensional simulator solving autoconsistently the Poisson and Schroedinger equations. This simulator was extensively checked on uniformly doped P-HEMT structures and was found to be in good agreement with the experimental results.
A mesa etching technique was used to isolate the active areas of the transistors and the ohmic contacts of the source and drain electrodes were realized by Electron Beam (EB) evaporation and lift off of a Au-Ge-Ni alloy followed by a rapid thermal annealing process.
The gate electrode had a length of 0.5 microns and was defined by optical lithography. The gate metals (Ti/Pt/Au) were deposited by EB evaporation and lifted off using a triple resist level technique. The gate recess was obtained by a wet selective etching. A Si_3N_4 passivating layer was deposited by PECVD and galvanic gold air bridges were used as interconnection metal.
The process was finally completed by the wafer thinning down to 60 microns and the realization of dry etched and electroplated via holes as grounding connections.

Electrical characterization

The lay-out of the processing mask set was drawn including structures for on wafer microwave probing, using a CASCADE coplanar probe. The distance of the source ohmic contact from the gate edge was 1 micron. This value represents a good compromise between the need to get a reasonably low value of the access resistance from the source contact to the channel region, and the control of the distances that can be obtained using the optical lithography. The devices have a gate multifinger lay out, so that the source pads are connected each other through metallic air bridges passing over the gate feeder.
The measurement of the DC characteristics showed the following results:
- maximum extrinsic transconductance g_{mmax} = 400 mS/mm
- drain saturation current I_{DSS} = 360 mA/mm
- pinch off voltage V_p = -1.2 V
- gate to drain breakdown voltage V_{BR} = 10 V

The pinch off voltage was measured referring to a drain current equal to 1/100 I_{DSS}, and the maximum of transconductance g_{mmax} was reached around V_{GS} = -0.5 V.
In Fig. 2 the measured I-V characteristics for a device of 200 micron gate periphery are shown. The upper curve

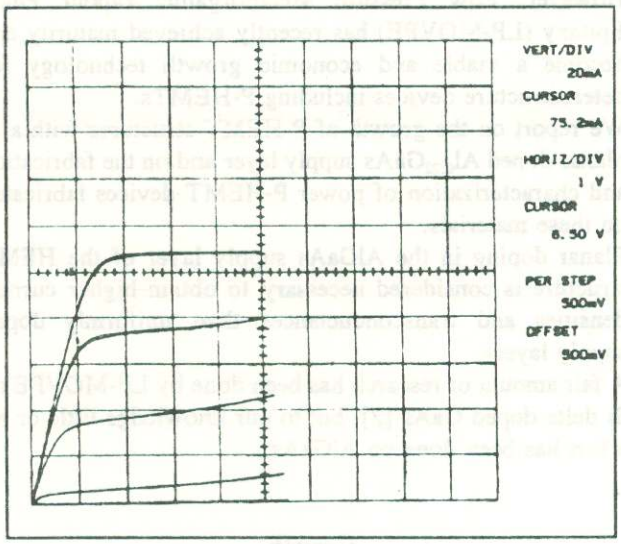

Fig. 2 200 μm width I-V characteristics.
Vert/div = 20 mA Horiz/div = 1 V

refers to a 0.5 V gate voltage.
The AC small signal characterization was performed up to 26.5 GHz by biasing the devices in different conditions.
For a 200 micron width device biased at 4 V drain - source voltage and $I_{DSS}/2$ drain current, the following results have been obtained:
- maximum frequency of oscillation f_{max} = 60 GHz
- cut off frequency f_T = 30 GHz
- maximum stable gain at 18 GHz = 11.5 dB

The device was conditionally stable up to 21 GHz and its maximum available gain at 26 GHz was 7.3 dB.
To obtain the evaluation of the power capability of our δ doped structure, several devices have been tested by a load pull measurement system able to perform on wafer measurements; it is based on an active load loop technique [3], [4] in order to cover almost the whole Smith chart.
The measurement was done at 18 GHz and, in order to exploit the whole available current range, the bias point for the devices was V_{DS}= 5 V and I_{DS}= $I_F/2$, where I_F is the drain current for +0.5 V gate voltage.
In Fig. 3 the measured load pull contours are shown: they represent the load loci for constant output power at 1 dB gain compression point. The measured power was 19 dBm for a 200 micron width device, corresponding to about 380 mW/mm; the associated linear gain was 8.2 dB.

Conclusions

Power transistors have been fabricated on Si δ doped P-HEMT structures grown by LP-MOVPE. This work demonstrated the feasibility of δ doped AlGaAs supply layers by the LP-MOVPE technique with 2D carrier sheet densities comparable to those obtained by MBE . The device performances are extremely encouraging showing power densities as high as 380 mW/mm and associated linear gains of 8 dB. Presently the device performances seem to be seem to be limited by the gate length, but state of the art devices are expected from quarter micron gate designed transistors.

References

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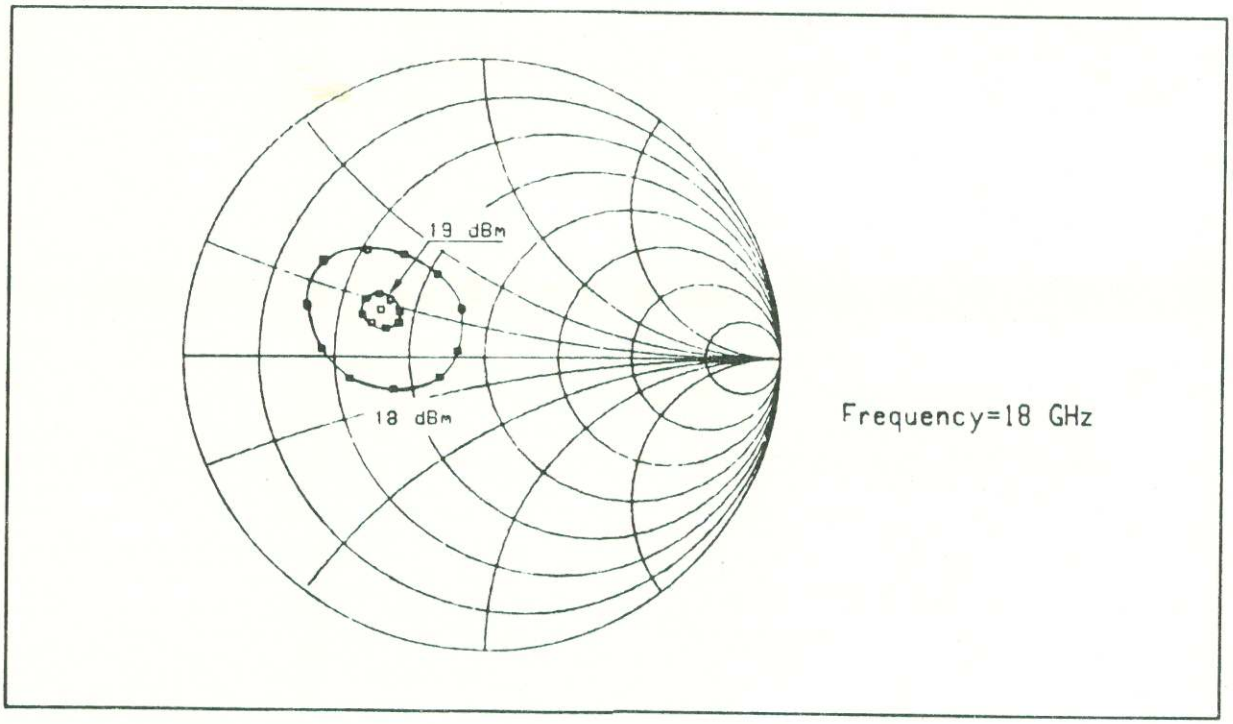

Fig. 3 Load pull contours for constant output power at 1 dB gain compression