# Delay, power and area expressions for GaAs DCFL circuits and their applications to optimization

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## Abstract

This work addresses the problem of analytical multiobjective optimization of combinational DCFL/SDCFL GaAs MESFETs IC. The critical path is determined by means of the GASTIM timing analyzer. The optimization strategy takes into account the slope dependency, the fan-out and the wiring capacitances. The results show that is possible to decrease the power consumption without degrading the propagation delay. We are not aware of any automatic tool able to solve the optimization task when designing circuits on GaAs material.

## Introduction

The DCFL/SDCFL family is up to now the dominant technology in designing VLSI Digital ICs on GaAs. This technology is utilized to design high performance circuits with high operating speed, low power consumption and small chip area. This paper presents an optimization strategy to deal with this logic. An automatic prototype tool is also described.

## Delay, power, and area models

This section is devoted to summarize the properties and the operation of the delay, power and area models used in the optimization methodology. The models are heuristics and technology independent.

### A. Delay model

The propagation time is calculated by using a simple polynomial expression [1],

$$\begin{aligned} T_P(T_I,\beta,C_L) &= (k_{11}+k_{12}\beta+k_{13}\beta^2)+(k_{21}+k_{22}\beta+k_{23}\beta^2)C_L + \\ &+[(k_{31}+k_{32}\beta+k_{33}\beta^2)+(k_{41}+k_{42}\beta+k_{43}\beta^2)C_L + \\ &+(k_{51}+k_{52}\beta+k_{53}\beta^2)C_L^2]T_I \end{aligned} \quad (1)$$

where $T_I$ represents the input slope, and $C_L$ a "linearized" output load capacitance. The coefficients $k_{ij}$ are calculated to minimize the sum of squared errors between this expression and simulations with HSPICE. The same polynomial can be applied to compute the output slope. The estimated relative error is less than 15 % over the evaluated cases (compared to HSPICE [3] simulations).

### B. Power model

The power dissipated by the circuits under consideration is lower than the power consumed by other logic families widely known (as the case of NMOS, CMOS, or ECL circuits). This is mainly due to the supply voltage values used, which are around 1.4 volts. In this way, the dissipated power by a typical SDCFL gate is, approximately 0.5 mW, and a typical DCFL gate consumes about 90 $\mu$W. As has been demonstrated [4], dynamic power can be neglected.

Power is estimated by only considering the static power consumption. To do that, we handle polynomial expressions to evaluate the $P_{OH}$ (power consumed by the logic gate when its output is in a high logic state) and the $P_{OL}$ (power consumed by the logic gate when its output is in a low logic state).

The logic activity of the whole circuit is taken into account by means of the $q$ parameter which indicates the frequency in the measured interval in which the output voltage node of the gate is in a high state [4]. Therefore, power consumption is estimated as follows,

$$P_{dis}=qP_{OH}+(1-q)P_{OL} \quad (2)$$

The use of this expression (2) requires knowing the values of the parameters $q$, $P_{OH}$, and $P_{OL}$ for the typical configurations used by designers. From HSPICE simulations we measured those values and stored into look-up tables. The estimated relative error is less than 15 % over the evaluated cases (compared to HSPICE).

### C. Area model

Based on the fact that active chip area increases roughly linearly with the transistor width, a simple area model can be implemented. Given a logic circuit, the calculation

methodology consists of evaluating the expression,

$$A_i(\beta_i) = \phi \cdot [\beta_i + \alpha] \quad (3)$$

where $\alpha$ and $\phi$, are design rule dependent coefficients. The $\beta$ variable is the aspect ratio corresponding to the transistor placed at the $i$ position in a circuit. The area of each transistor is determined from the layout design rules. Due to the fact that every transistor contributes to the final chip area with a portion of area occupied by its connections (which is proportional to its width), this methodology is not strongly dependent on how the buses are outlined.

Our area formulation is a transistor level methodology, in contrast to the traditional gate-level approaches [2]. The estimated relative error is less than 15 % over the evaluated cases.

## Optimization methodology

The optimization problem to be resolved can be classified as a nonlinear multivariable one. The objective function to be optimized is the one regarding delay, power and area estimation:

$$H(\beta) = H(D(\beta), P(\beta), A(\beta)) \quad (4)$$

In the above expression, it is assumed that the propagation delay $D(\beta)$ is given by the weighted average of both propagation delay, $T_{PHL}$ and $T_{PLH}$.

To include the differences on the timing behaviour we introduce two extra parameters, $\vartheta_{HL}$ and $\vartheta_{LH}$ which allow a relative value to be assigned to them. In a similar way, the power consumption to be optimized is given by the average of both consumption states, $P_{OH}$ and $P_{OL}$. As non periodical signals are assumed, it is required to introduce new parameters ($\kappa_{OH}$ and $\kappa_{OL}$) for the power case. As a main difference with MOS circuits, in the GaAs context the minimum delay occurs from the design having the minimum dimensions (widths) for all the switching transistors.

Optimal sets of gate dimensions $\beta = \{\beta_n\}$ are called noniferior solutions; $\beta'$ is a noninferior solution if there exits no feasible design alternative $\beta$ that improves at least one design objective without degrading another [2]. The optimal set of gate widths are calculated by minimizing the weighted sum $H\{\beta\}$ of the cost functions:

$$H(\beta) = \delta_D \cdot D'(\beta) + \delta_P \cdot P'(\beta) + \delta_A \cdot A'(\beta) \quad (5)$$
$$\delta_D + \delta_P + \delta_A = 1$$

where $D'$, $P'$ and $A'$ are dimensionless cost functions normalized to convenient area, power and time units. It can be demonstrated that it is possible to obtain the optimal solution by the methodical alteration of the weight coefficients [5].

### A. Global Optimization Strategy

The global optimization strategy consists of two well defined phases; the first one involving analytical sizing and the second one regarding buffering. As we have already presented, changes regarding the sizes of the drivers transistors are allowed; this is carried out by the sizing algorithm.

So far, an analytical model to implement buffering is not available. This is because the closed solution for the DCFL gate is quite complicated. To solve the problem we have decided to apply an empirical local buffering technique with the purpose of reducing the power-area trade-off. To do that, an exhaustive analysis of a set of different geometries for the source-follower has been carried out. From this, a reduced number of geometries were obtained [5]. The overall cases satisfied two characteristics: i) the noise margin was always within the constraints and ii) there was no important degradation in the speed by using these buffers.

### B. Algorithms

The whole set of the noninferior solutions are obtained by minimizing the objective function as we have already quoted. From the analytical study of the objective function we resolve the optimization problem by means of a gradient-method algorithm [5] instead of using a lagrangian [2] The algorithm has been implemented in a C code and it runs on an UNIX environment. The examples we present in the next section were run on a SUN SPARC2 machine.

### C. Boundary conditions

To fully solve the problem some boundary conditions are needed. There are some technological design rules that must be satisfied. Thus for each gate type, there exists a lower boundary (width) and an upper boundary (width). The constrictions can be written in the following way:

$$\{\forall\{logic\ gate\}\} \cap \{\forall\beta \in [\beta_{allowed}]\}\ thus:\ \beta \geq \beta_{min}$$
$$\{\forall\{logic\ gate\}\} \cap \{\forall\beta \in [\beta_{allowed}]\}\ thus:\ \beta \leq \beta_{max} \quad (6)$$

It is important to note that either the power consumption or the area occupied can define a certain maximum transistor width as well. Besides, the designer can fix some transistor width in order to avoid hot points and in this way to distribute in a more effective manner the dissipated power (or area). The definition of the problem is complete and the methodology to detect the optimal solution is presented in the next section.

Table 1: Comparison with the minimum-maximum values.

| Propagation delay | Power consumed | Area occupied |
|---|---|---|
| + 39.04 % (delay min.) | + 3.54 % (power min.) | + 9.47 % (area min.) |
| - 31.10 % (delay max.) | - 9.72 % (power max.) | - 10.40 % (area max.) |

## Examples

This section reports on obtaining the whole set of noninferior solutions for two significant cases. On the one hand, the sizing algorithm is applied to a full-adder critical path in order to find the optimal solution for the delay-power conflicting criteria.

On the other hand the strategy (sizing+buffering) is used for optimizing the 4-bits carry look-ahead critical path.

### *A. Sizing: Noninferior solutions diagram*

This circuit consists of a path containing eleven logic gates (simple inverters and 2-NOR gates) and the capacitance value due to the interconnections having been fixed to the typical value usually found from the extracted layouts (10 fF). A 200 ps input slope has been adopted. The description of the circuit is fully completed by adding an additional load gate at the end of it.

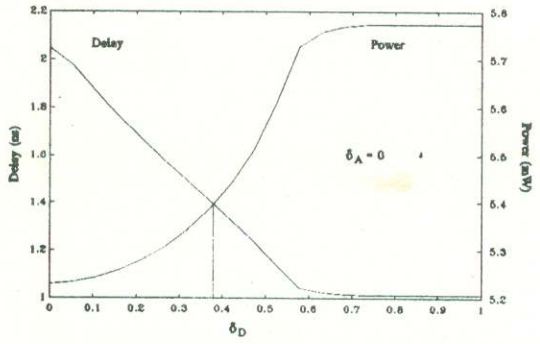


Fig. 1. Noninferior solutions for example 1.

Fig. 1 represents the best possible delay-power trade-offs for this case. It can be seen how power consumption increases very rapidly when the minimum delay is approached. From the analysis of this plot, the designer can choose from among the complete set of noninferior solutions; the optimal solution is given by the cross-point and it occurs for a $\delta_D \approx 0.4$ (it means a value $\delta_P \approx 0.6$, this is because $\delta_A = 0$).

However the optimal solution is not always the one the designer is looking for. By inspecting this plot, the designer can decide by a minimum-consumption power design (looking for $\delta_D$ values on the left side of the axis) or by a minimum-delay design (moving in the opposite direction).

It is evident that to find the optimal solution by means of using an electrical simulator (SPICE) is practically an impossible task.

The performance estimation for the optimal solution case is compared to the estimation for the maximum-minimum delay and power trade-offs in table 1.

### *B. Sizing and Buffering*

A 4-bit CLA (Carry Look-Ahead) circuit has been chosen as an example to demonstrate the possibilities the optimization strategy holds itself. The delay critical path is given by GASTIM [1] and it corresponds to a chain of six 2-NOR gates.

Once the gates are reduced to the equivalent inverters and an additional load gate has been added, the formulation of the problem is achieved with the following aspects: a 200 ps input slope is taken, the capacitance values are held at a 15 fF, and both 12 $\mu$m and 30 $\mu$m are accepted as the boundary constrictions for the transistor widths. In this case a truly multiobjective optimization is attained, this means that the trade-off established through delay-power-area is explored in a simultaneous way. This is done by fixing a value for the weight coefficient associated to the area cost function ($\delta_A = 0.12$). The noninferior solutions sort can be seen in fig.2.

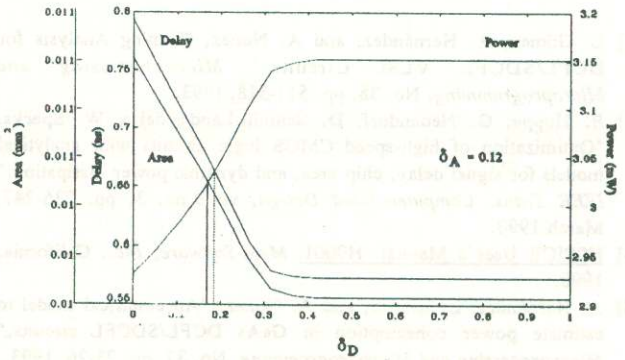


Fig. 2. Noninferior solutions for example 2.

Besides, in this example the proximity between both optimal solutions allows considering them as if they were common. The results obtained are presented in table 2. It is important to emphasize that an excellent improvement in the power

Table 2: Comparison of the results before applying the optimization strategy.

| Optimization type | Propagation delay | Power consumed | Area occupied |
|---|---|---|---|
| *sizing* | 0.68266 ns | 3.013946 mW | 0.0105 ($mm^2$) |
| *sizing + buffering* | 0.69469 ns | 2.663691 mW | 0.0099 ($mm^2$) |
| relative difference | + 1.76 % | - 11.62 % | - 5.68 % |

consumption (and in the area occupied) is gained while the delay propagation experiments a non significative increase, which is consistent with the assumptions used.

The noninferior solutions sort can be seen in figure 2. It is important to emphasize that an excellent improvement in the power consumption (and in the area occupied) is gained while the delay propagation experiments a non significative increase, which is consistent with the assumptions used (see table 2).

## Conclusions

An analytical gate-power model and an analytical gate-area model have been introduced. Both models are based on polynomial expressions and therefore estimations are obtained fast at low computational costs. By handling these estimation models, an efficient optimization technique for DCFL/SDCFL has been introduced.

This technique has been implemented in an algorithm. The optimization can be done either to reduce the path delay to its absolute minimum for a given technology or to explore the whole set of noninferior solutions for the delay-power-area trade-off.

## References


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