An Electro-Optic Sample and Hold Circuit Using GaAs MESFET Technology

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Abstract

This paper presents a fully integrated optically controlled sample and hold circuit (OS/H) which is fabricated in a commercial GaAs MESFET technology. The OS/H will find applications in many high-speed sampled data systems where high speed, high levels of parallelism and low timing jitter are important. Measured results are presented which demonstrate the operation of the circuit at sample rates approaching 500Ms/s at 7.6-bits resolution.

1. Introduction

Sample and hold (S/H) circuits play an important role in many signal processing applications in which the acquisition of analogue signals and their conversion into quantized forms is required. An example of such a system is the time-interleaved architecture, which has been used to obtain high sampling rates in, eg., analogue to digital conversion (ADC) systems [1]. All-electronic S/H systems have been demonstrated on both silicon and GaAs substrates at sample rates in excess of 1Gs/s [1,2,3]. However, it is difficult to realise the maximum potential of the interleaved architecture using all-electronic techniques due to the extreme timing accuracy requirements of clock generation and distribution [1,4]. For example, in order to sample a sinewave of frequency 1GHz at 8 bits resolution, clock jitter must be less than about 0.5ps r.m.s and in an interleaved structure this level of accuracy must also apply to errors in *relative* clock phasing (clock skew). By contrast, optical techniques can be employed in systems requiring high levels of parallelism, to obtain very low jitter and excellent isolation from electronic switching transients [5,6]. The use of such methods has been greatly facilitated by recent rapid developments in optical components and systems. For example, mode-locked lasers are available as sources of high-energy, short duration pulses with very low levels of jitter (0.1-0.5ps, see ref [7]) and optical fibres or, alternatively, more sophisticated techniques using integrated optical waveguides can be used to provide jitter-free clock distribution and delay [5]. For example, using a mode-locked semiconductor laser and single-mode optical fibre delay lines, optical clock distribution has been demonstrated with levels of jitter less than 0.4ps rms [8]. Since at present no satisfactory three-terminal optical switch exists, it is not possible to construct an all-optical S/H circuit and current research in this area has been directed to the development of hybrid optoelectronic S/H (OS/H) systems. These systems use the advantageous properties of optics in the generation and distribution of clock waveforms, while employing electronics in those parts of the system which are less sensitive to noise and jitter [9,10].

The application of electro-optic techniques to high-speed, high resolution A/D conversion using interleaved architectures was discussed in reference [6]. This discussion included the introduction of an OS/H circuit suitable for such applications. Since this circuit requires only *one* optical address, it is particularly well suited to higher levels of optoelectronic integration. This circuit has now been fabricated in 0.5μm gate length, 20GHz f_T, −1.0V threshold GaAs MESFET technology. Some preliminary measured results have been published recently [10] and the proposed new contribution will present complete measured data.

2. Architectures for optically triggered sample and hold circuits

The use of a photoconductor employed as a series sampling switch (Auston switch) has been proposed as a candidate OS/H [9,11] and is illustrated in Fig. 1. Although attractively simple, the maximum sampling rate of this circuit is severely limited by the relatively high series resistance of the illuminated photoconductor and by the slowness of the turn-off transition. The latter problem arises from the fact that in the absence of a static electric field across the device, the on-to-off transition is brought about by thermal recombination of electron-hole pairs, which is a relatively slow process. In practice, this difficulty is exacerbated by a reduction in the extinction ratio of the laser pulses at high repetition rates.

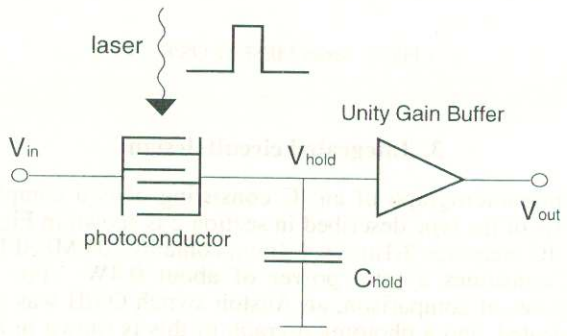

Fig. 1. Optically triggered sample and hold circuit using a series photoconductor (Auston switch).

As an alternative to the Auston switch OS/H, the use of a current-steering bridge has been proposed [9]. This circuit is familiar from all-electronic S/Hs [3] and in principle this arrangement has several main advantages over the series switch OS/H described above. For example, it is possible to achieve much higher sampling rates than can be attained with the series switch arrangement. On the other hand, the relatively high complexity of the arrangement and, in

particular, the requirement for *four* independent optical clocks reduces the attractiveness of the current steering bridge for higher levels of optoelectronic integration [5].

In the proposed new paper we describe an alternative OS/H circuit requiring only one optical address, the elements of which have been outlined in references [6,10] and this is shown in Fig. 2. As in the Auston switch, this circuit employs a series analogue switch element to charge C_{hold} from the voltage source V_{in}. Unlike the Auston switch, however, the switching device is a GaAs MESFET (M1) operated in its linear region rather than a photoconductor operated under zero bias conditions. The separation of the functions of photodetection and switching allows the components representing both functional blocks to operate under more nearly optimal conditions than is possible with the Auston switch.

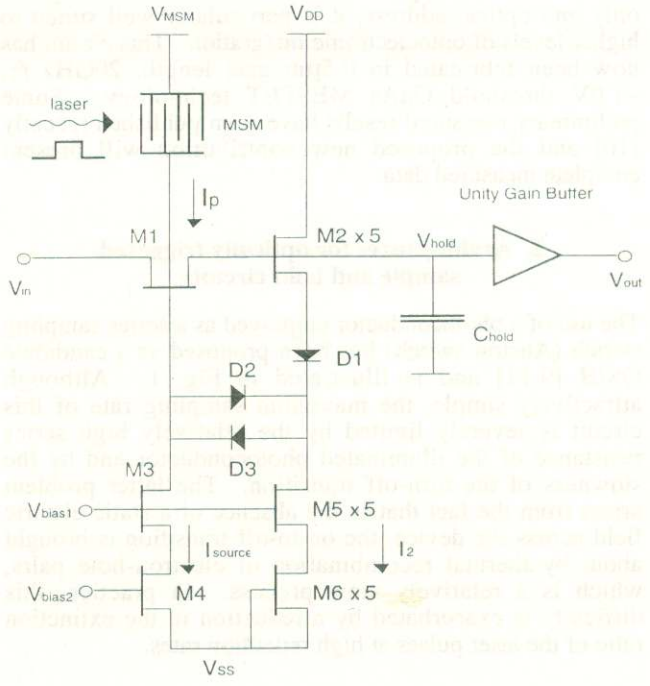

Fig. 2. Series MESFET OS/H.

3. Integrated circuit design

A photomicrograph of an IC consisting of two complete OS/Hs of the type described in section 2 is shown in Fig. 3. The IC measures 2.1mm x 1.4mm, contains 104 MESFETs and consumes a total power of about 0.4W. For the purposes of comparison, an Auston switch OS/H was also fabricated, and a photomicrograph of this is shown in Fig. 4. To prevent the optical clock from interacting with the electronic devices, in both designs the photodetectors are positioned at least 500μm away from the electronic circuitry. Each IC is gold-wire bonded to a high frequency ceramic package and all DC supplies are decoupled using surface-mount capacitors.

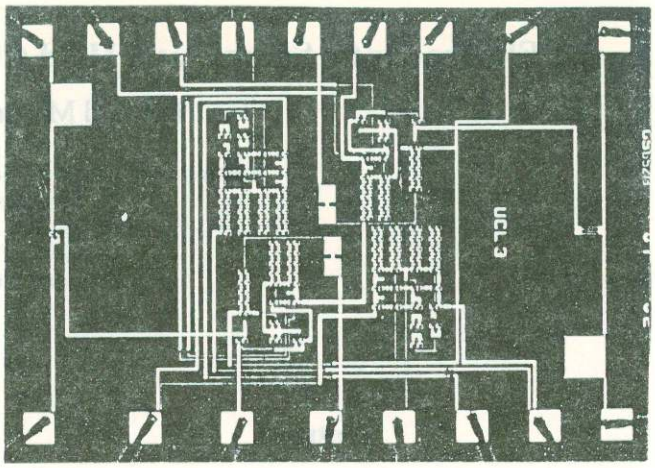

Fig. 3. Photomicrograph of a series MESFET OS/H chip.

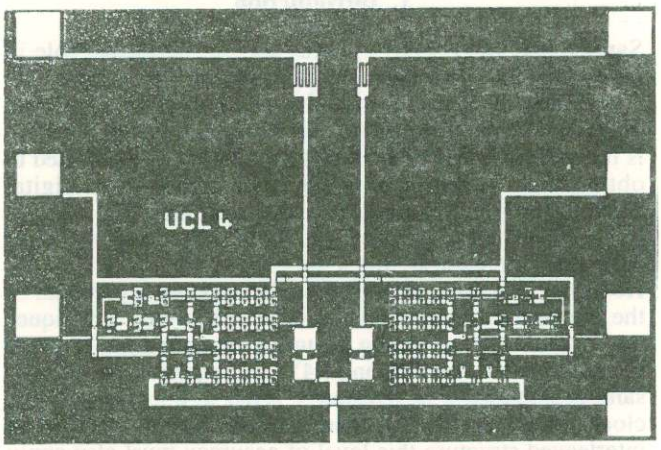

Fig. 4. Photomicrograph of series photoconductor OS/H (Auston switch).

4. Measured results

A. Experimental arrangement

The experimental arrangement used to evaluate the two OS/H ICs described above is shown in Fig. 5. The optical source was provided by an 830nm laser diode connected to a driver circuit which provided on-off modulation up to 250MHz and adjustable mean output power. For the pulsed measurements described below, a duty-cycle of 50% was employed corresponding to mean power incident on the photodetector of 5mW. The light from the laser was launched into a 50μm core, multi-mode optical fibre, by means of a microscope objective. The resulting light spot, when brought close to the surface of the die, is compatible with the 60μm x 60μm MSM photodetector used in the design. Accurate alignment of the optical fibre with the integrated photodetector was achieved using a 3-way micropositioner with piezoelectric adjustment and a long working-distance microscope.

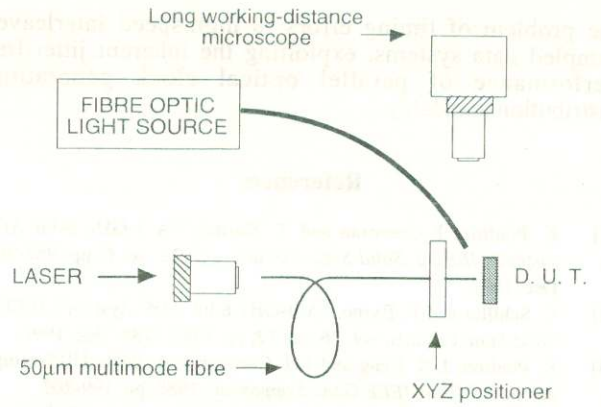

Fig. 5. Experimental arrangement.

B. Acquisition time and settling time

Fig. 6 shows the measured performance of the OS/H of Fig. 3 with a 62.5MHz sinusoidal input of 0.4V rms, sampled at 250Ms/s (ie., 4 samples/period). The acquisition time, τa, for an accuracy equivalent to 8-bits, was determined from a measurement of the rise time from 10%-90%, assuming an exponential characteristic. By this method, a value of approximately 2.0ns was obtained for τa and the settling time, τs, was found to be negligible. This implies an absolute maximum sampling rate, $f_s max$, for this input signal, approaching 500Ms/s.

$$f_{smax} = 1/(\tau a + \tau s). \qquad (1)$$

For the purpose of comparison, the above tests were repeated using the series photoconductor (Auston switch) OS/H shown in Fig. 4. The measured results are shown in Fig. 7 and the value for $f_s max$ of 13MHz emphasises the limitations of this approach.

C. Pedestal and droop

In order to measure *pedestal* and *droop*, and to be able to distinguish accurately between these effects, the input signal frequency (0.4V rms sinewave) was reduced to 1MHz, which was sampled at 5Ms/s. A number of measurements of the pedestal were made, which revealed a constant value (ie. DC offset) of 15mV and a signal dependent component of 3mV, which corresponds to an effective resolution of 7.6bits. This arrangement was also used to measure *droop* of the OS/H, whose value was found to be about 200μV/ns, which is quite large compared to that reported in [1]. Nevertheless, the error due to droop in a period of 2ns is only 400μV, which is small compared to the effect of the pedestal.

D. Analogue Frequency Response (Bandwidth and THD)

For this measurement, the OS/H photodetector was illuminated with CW laser light of 5mW, ie., the same as the mean power used for the pulsed measurements, and the OS/H was connected to a network analyser. The measured amplitude of the frequency response was found to be flat to within 0.5dB across the frequency range DC-500MHz. The total harmonic distortion (THD) of the OS/H was measured using the same experimental arrangement with a sinewave input of frequency 100 MHz and amplitude 0.4V rms. Using this method, a value of 0.9% THD was measured which agreed closely with the HSPICE simulation.

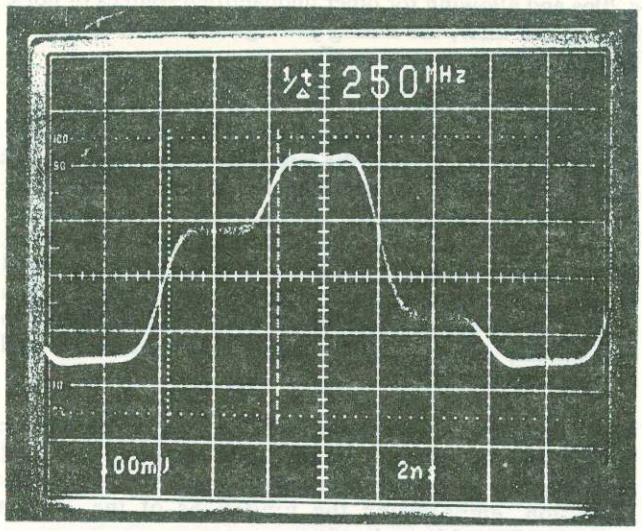

Fig. 6. Output of a series MESFET OS/H when sampling a 62.5MHz sinusoid at 250Ms/s.

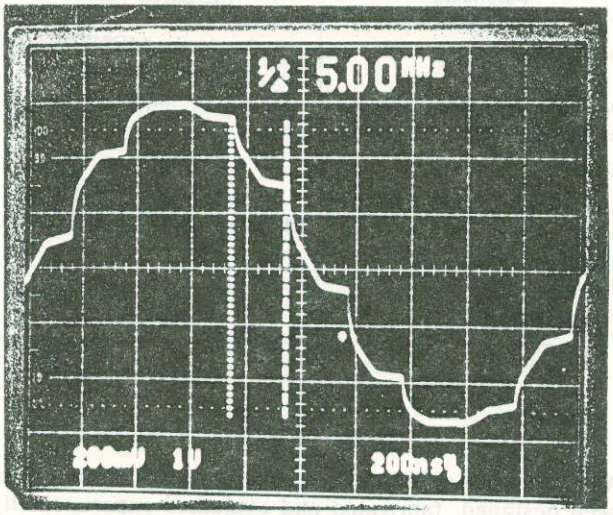

Fig. 7. Output of the Auston switch OS/H when sampling a 500kHz sinusoid at 5Ms/s.

E. Aperture Jitter

Since the minimisation of timing jitter is such a fundamental issue, it is important to estimate the contribution from the OS/H itself. The acquisition time measurement described in section 4B was repeated but with the input sinewave locked at exactly half the clock rate. The input and clock frequencies were 50MHz and 100Ms/s respectively. The phase angle between the two signals was adjusted so that the transition from sample to hold occurred precisely at the zero-crossing points of the sinewave. In the absence of timing jitter, the OS/H should record no output in the hold phases except random noise originating from the buffer amplifier, etc. This random noise contribution was measured by repeating the experiment with the input of the OS/H shorted to ground. After eliminating the random noise component, the residue, when translated into timing jitter at the zero-crossing points of the input sinusoid, amounted to about 20ps rms. Since the pulse generator used to trigger the laser has a timing jitter specification of

< 20ps and allowing for other unquantified sources of noise such as the laser, the timing jitter generated by the OS/H itself is likely to be very small.

F. Aperture Adjustment

As described in [6], the sampling instant depends on the ratio of I_p to I_{source} and the rise time of I_p, which in this case is dominated by the 200ps rise time of the pulse generator. By adjusting the DC gate-source voltage of M4, it was possible to delay the sampling instant by about 130ps, corresponding to about 25mm of fibre. If the OS/H of Fig. 2 were used in an interleaved architecture, such a degree of adjustment would be more than adequate to dynamically compensate for component mismatches and environmental variations.

These results are summarised in Table 1. The data for the OS/Hs suggest absolute maximum sampling rates of 500Ms/s and 13Ms/s respectively at approximately 8-bits resolution, emphasising the limitations of the Auston switch OS/H in this application.

TABLE 1
SUMMARY OF MEASURED OS/H PERFORMANCE

Parameter	Measured Value
Acquisition Time	2ns (series MESFET) 40ns (Auston switch)
Pedestal (0.4V rms sinewave, f=1MHz)	3mV
Droop	200μV/ns
Gain Flatness (to 500MHz)	–0.5dB (series MESFET) (Auston switch f_{-3dB} = 23MHz)
THD (0.4V rms sinewave, f=100MHz)	0.9%
Aperture Jitter	<1ps rms

5. Conclusions

A fully integrated GaAs optoelectronic OS/H circuit has been designed, fabricated and evaluated experimentally. The measured results indicate that sample rates approaching 500Ms/s for a 400mV rms input sinusoid are possible, with a resolution of 7.6 bits. This OS/H is intended to form the basis of an optoelectronic solution to the problem of timing errors in high-speed interleaved sampled data systems, exploiting the inherent jitter-free performance of parallel optical clock generation, distribution and delay.

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