Ku-band modular MMICs for up to 5W power blocks for VSAT applications

Laurent Potteau, Pierre Quentin, Marc Parisot

THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES
RD 128 / BP46 / 91401 ORSAY CEDEX (FRANCE)

Abstract

An innovative approach to a quick design of multi-watts Ku-band power amplifiers for VSAT up-link applications is proposed. Starting from a set of specifically developed MMIC power macrocells, a modular implementation is used to combine them into power modules requiring no adjustment and delivering up to 5W with 24dB associated gain in the 14-15.5GHz frequency band. The basic MMIC single chips exhibit a 1dB gain compression output power of respectively : 200mW, 500mW and 1.6W.
3W and 5W power modules are presented as examples.

Introduction

The availability of low cost Solid State Power Amplifiers (SSPA), is an important factor in the development of small VSAT mobile and ground stations. Existing hybrid solutions are challenged by MMICs in terms of size, manufacturability and reliability. Moreover, a single MMIC design can cover different frequency bands, allowing a system cost reduction.
Using MMICs for a greater integration implies also a straightforward methodology to design and implement them as building blocks meeting the system performance requirements according to the predicted values.

Technology

All the power MMICs have been realized using the standard TCS foundry process HP05. This process features a half-micron E-Beam written TiAl gate evaporated on a MBE grown active layer. The Low-High-Low profile has been specially optimized for the best compromise between the transconductance, the breakdown voltage and the intermodulation distortion. The 100µm thick substrates include also air bridges and via holes through the substrate. The basic FET typical electrical characteristics are listed below :

Threshold voltage : -2.8V
Saturation current : 350mA/mm
Transconductance : 145mS/mm
Breakdown voltage : 13V
Power capability (-1dB GC @18GHz) : 500mW/mm
Associated gain : 6.5dB
Drain power efficiency : 40%

Device modelling

MMIC macrocells were designed using the non-linear model available in the HP05 foundry manual.

The non linear FET model shown in Fig. 1 is a Tajima type specific to the design of power amplifiers [1].

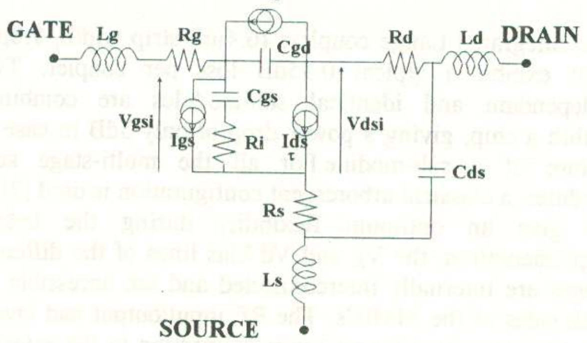

Fig. 1 : FET large signal model topology

In this amplification mode the main non-linearities are :
- The drain to source current Ids,
- the direct gate to source current Igs,
- the drain to gate avalanche current Idg.

These currents are deduced from I(V) pulse characteristics obtained by excursions around a bias point, thus taking into account the thermal effects. Measured small signal S-parameter are also used for the extraction of the linear elements.

Circuit design

MMIC design has been completed with a primary objective of performance insensivity to the integration process in cascade or parallel mode. The main causes of degradation are :
- The RF access bonding wires which modify the input/output reflexion coefficients (cascade) and the circuit symetry (paralleling).
- The bias networks which may induce instabilities through reactive coupling loops.

To overcome these problems, Lange couplers are integrated on chip giving an input and output return loss better than 15dB. Associated to these couplers, a low loss FET output matching network has been used which reduces the loss to 0.3dB (Fig 2b) compared to the 0.6dB of the usual network (Fig. 2a).

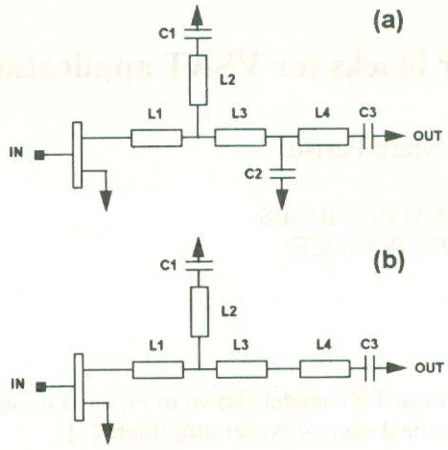

Fig. 2 : FET output matching networks
(a) Usual network
(b) Utilized network

The integrated Lange couplers (6.4µm strip width, 7.8µm gap) exhibit a typical 0.35dB loss per coupler. Two independant and identical sub-modules are combined within a chip, giving a power drop of only 3dB in case of failure of a sub-module.For all the multi-stage sub-modules, a classical arborescent configuration is used [2]. To give an optimum flexibility during the hybrid implementation, the Vg and Vd bias lines of the different stages are internally interconnected and are accessible on both sides of the MMICs. The RF input/output pad layout are also optimized for an easier connection to the external hybrid circuit.

MMIC performance

Three MMIC power macrocells have been designed and realized :

- A two-stage Driver (Fig. 3),
- a single stage Medium Power Amplifier (MPA) (Fig 4),
- a two-stage High Power Amplifier (HPA) (Fig. 5).

After the technology process, the amplifiers were measured on-wafer, S-parameter for the Driver and pulse power for the MPA and the HPA. The full characterization including temperature measurement was completed after an appropriate packaging. Main results are summarized in table 1.

Table 1 : CW main chip performance
F=14-14.5GHz, class A, T=20°C

Chip	Driver	MPA	HPA
-1dB gain comp. output power, dBm	23	27	32
Linear gain, dB	15	7	12
Power added efficiency, %	22	20	18
Gate periphery, µm	6x50 (x2)	6x50 (x4)	16x50 (x2) 12x75 (x4)
Chip size, mm²	2.8x2.3	2.8x2	3.5x2.8

HPA gain and power performance as a function of frequency are plotted in Fig. 6 and Fig. 7 for three different temperatures.

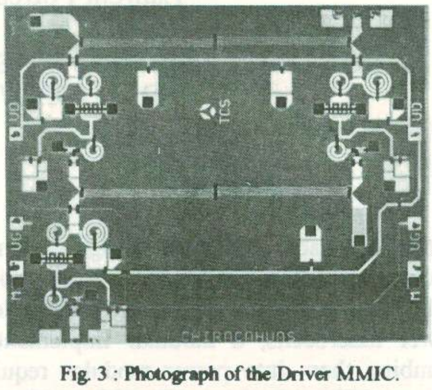

Fig. 3 : Photograph of the Driver MMIC.

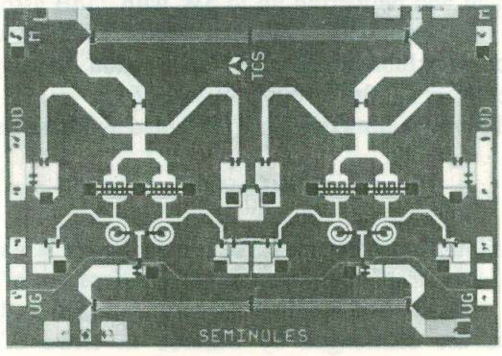

Fig. 4 : Photograph of the MPA MMIC.

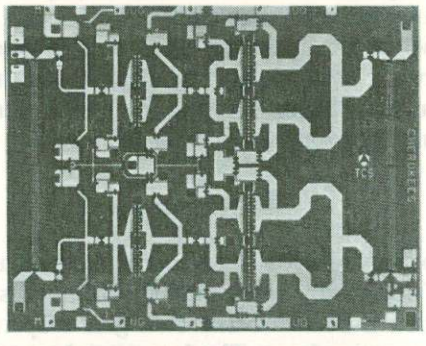

Fig. 5 : Photograph of the HPA MMIC.

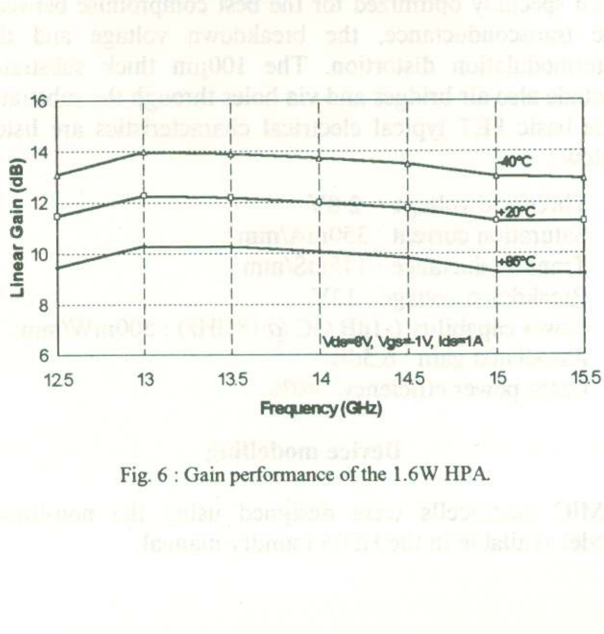

Fig. 6 : Gain performance of the 1.6W HPA.

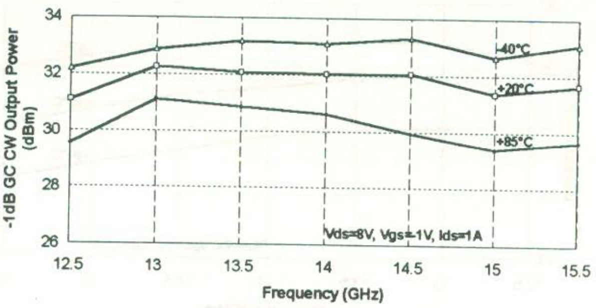

Fig. 7 : Power performance of the 1.6W HPA.

Modular implementation

The different MMIC macrocells, can be used as single cells or combined in a cascade or parallel configuration with a quick design and predictable performance. The paralleling is done through Lange and/or hybrid Wilkinson combiners since the MMIC layout have been optimized for this purpose. Some possible combinations are illustrated in Fig. 8.

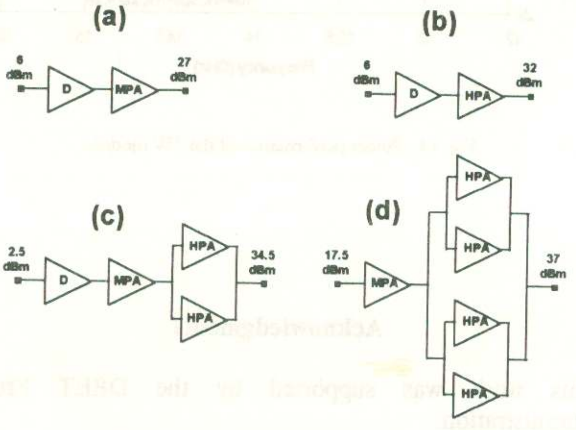

Fig. 8 : Possible macrocell combinations.
D : Driver
MPA : Medium Power Amplifier
HPA : HighPower amplifier

3W power module

To illustrate the modular concept, 3W and 5W power modules have been assembled and tested.
The 3W module is realized with two HPA macrocells mounted directly on a 10x10mm² Copper-Molybdenum base, including also two alumina subtrates with the Lange couplers, the RF paths and the MMIC bias circuitry. This module is plugged into a connectorized package and is represented in Fig. 9.

Results
At 20°C, a 35 ±0.4dBm CW output power at 1dB gain compression was obtained with 11 ±1dB associated gain in the 12.5-15.5GHz frequency range; the power added efficiency is 19.6% at 8V, 1.9A. Gain and power measured results are respectively plotted in Fig. 10 and Fig. 11 as a function of frequency and temperature.

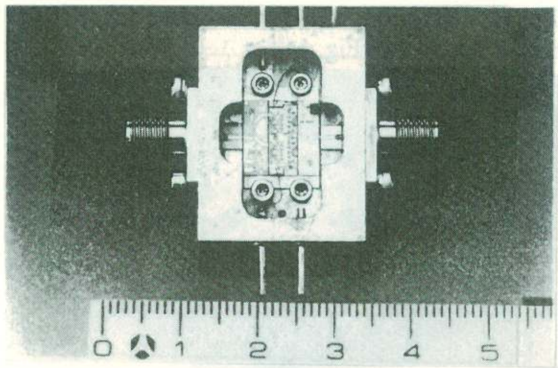

Fig. 9 : Photograph of the 3W power module.

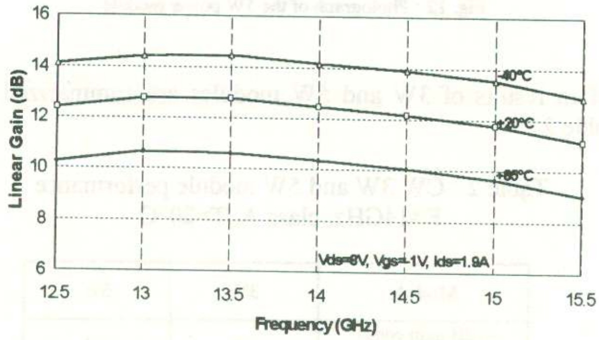

Fig. 10 : Gain performance of the 3W module.

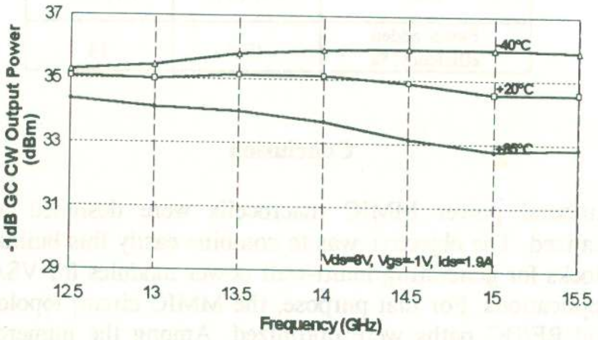

Fig. 11 : Power performance of the 3W module.

5W power module

The 5W power module has been assembled by paralleling two 3W modules through a pair of Wilkinson combiners. The four HPAs are driven by a single HPA but could have been driven by a MPA macrocell as well with a lower gain. The connectorized package includes three 10x10mm metal bases for the single and dual HPAs and two ceramics including the Wilkinson combiners also mounted on metal bases to insure a full modularity as illustrated in Fig. 12.

Results
More than 37dBm CW output power at 1dB gain compression was obtained with 25 ±0.5dB associated gain in the 13-14GHz frequency range; the power added efficiency is 14% at 8V, 4.5A. Gain and power measured

results as a function of frequency and temperature are plotted in Fig. 13 and Fig. 14 .

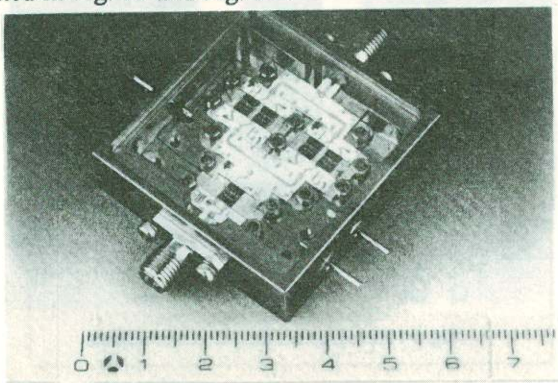

Fig. 12 : Photograph of the 5W power module.

Main results of 3W and 5W modules are summarized in table 2 .

Table 2 : CW 3W and 5W module performance
F=14GHz, class A, T=20°C

Module	3W	5W
-1dB gain comp. output power, dBm	35	37
Linear gain, dB	12.5	24.7
Bias	8V, 1.9A	8V, 4.5A
Power added efficiency, %	19.6	14

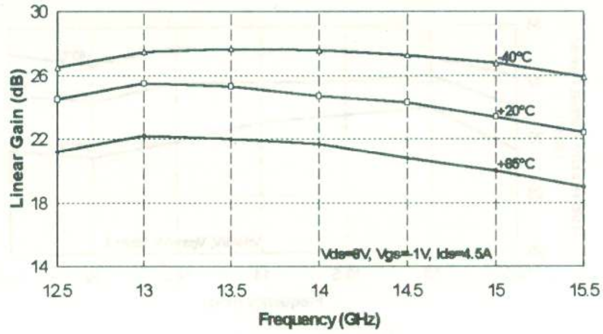

Fig. 13 : Gain performance of the 5W module.

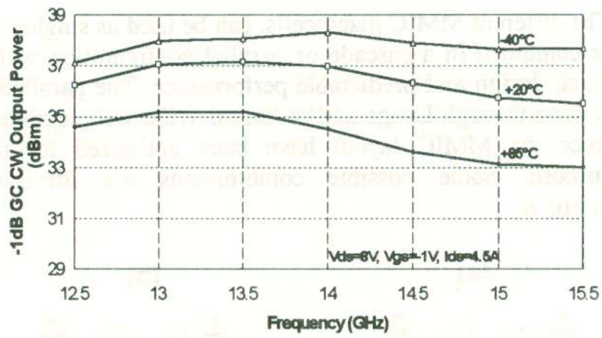

Fig. 14 : Power performance of the 5W module.

Conclusion

Ku-band power MMIC macrocells were designed and realized. The objective was to combine easily this building blocks for generating multi-watt power modules for VSAT applications. For that purpose, the MMIC circuit topology and RF/DC paths were optimized. Among the numerous realized macrocells, a 200mW Driver, a 500mW Medium Power Amplifier and a 1.6W High Power Amplifier are presented in this paper.

To demonstrate the modular capability, a 3W and a 5W power modules were assembled and measured with results in very good agreement with the predicted values.

Acknowledgments

This work was supported by the DRET French administration.

References

[1] MMIC FOUNDRY HP05 Design Manual

[2] G. Montoriol, I. Telliez, C. Rumelhard, "Optimum design and realization of MMIC power amplifiers", *Proceedings of the 19th European Microwave Conference*, 1989.