# MMICs for Satellite Ku Band TLC Repeaters

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## Abstract

This paper focuses on the development by Alenia Spazio of several GaAs MMICs and their application in miniaturised equipments for on-board satellite TLC repeaters.

## Introduction

Present satellite applications demand for optimisation of costs, masses, performance, and reliability of on-board equipments. In recent years increasing effort has been spent in development of MMICs suited for such applications, because of their advantages over the hybrid approach , in terms of: repeatability of performance (due to low parameter spread over a wafer lot; reduction of the size and mass; reduction of interconnections (yielding higher repeatability); broader potential bandwidth (due to lower parasitics) thus ability to use the same circuit in different applications. This paper will describe a set of MMICs which have been developed by Alenia Spazio, keeping in mind the previous considerations, with the aim to be used as building blocks of several satellite payload subsystems with versatile configurations.

## Technologies

As well known, GaAs technology is a mandatory choice for microwave communications applications: moreover, it is attractive in space on-board applications because of its characteristics in terms of radiation tolerance. Although a variety of new promising technologies have been proposed up to date, the choice of the fabrication process must fall within the limited range of reliable technologies such as:

standard MESFET;
pseudomorphic HFET;
InP based HFET;
HBT;

accounting for a variety of electrical requirements and types of circuits (e.g. either low noise or medium power).

The miniaturisation requirements for several on board and terrestrial radio link equipments has brought many researchers to develop multifunction MMICs [1-3] with the aim to reduce parasitics and overall dimensions. Such approach requires however the choice of a single process not always suitable for each electrical performance. On the other hand a modular approach, implying the use of simpler MMICs, allows application in several different subsystems, if the design is versatile enough or adjustable (e.g. by selectable bonding pads), and allows use of dedicated processes thus improving performance.

In this work the latter approach has been chosen and two technological processes were selected in order to get the best overall yield using a relatively simple technology:

- a low noise 0.25 μm pseudomorphic HEMT based process;
- a low pinch-off general purpose MESFET based process, with 0.5 μm gate-length and self-aligned technology.

For this work we chose the Raytheon ADC MMIC Foundry for the experience already shared with Alenia Spazio on space applications MMICs.

## Applications

Our work concerned mainly the development and implementation of three equipments for satellite repeater subsystems:

- a channel amplifier (CAMP) operating in the 10.7 to 12.7 GHz range;
- an upper Ku-to-X band Downconverter (DBSD);
- a lower Ku-to-X band Downconverter (FSSD).

The three equipments have been realised making extensive use of MMICs together with high-density hybrid MIC technology. The analysis of the requirements has shown that the three RF modules can be implemented using seven different types of MMICs:

- Two Low Noise Amplifiers (LNA) optimised in the 18 and 14 GHz range respectively;
- A 10.7 to 12.7 GHz Variable Gain Amplifier (VGA);
- A 10.7 to 12.7 GHz Flatness Corrector (FC).
- Two Mixers for downconversion from 14 to 12 GHz and from 18 to 12 GHz respectively.
- A 10.7 to 12.7 GHz Medium Power Amplifier (MPA).

In the CAMP seven VGAs are used both as fixed gain blocks and for gain and output level control (Fig. 1).

The same component is used in the IF section of the FSSD and the DBSD, allowing gain setting and temperature compensation.

The MPA is the output stage in both FSSD and DBSD; use of the MPA is optional in the CAMP to allow a higher output level and linearity. The FC is used in all three equipments for gain slope compensation after integration of the assemblies.

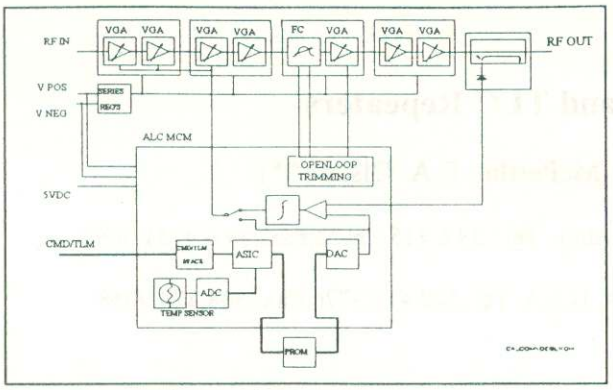


Fig. 1 : CAMP Architecture Block Diagram.

The RF front-end for the DBSD and the FSSD employ the LNAs and mixers optimised over the appropriate band. The circuits have also found application on satellite Ku Band Telemetry Transmitters and Command Receivers presently being developed in Alenia Spazio.

## MMICs Design

*1. Low Noise Amplifiers.*

Two PHEMT LNAs have been developed for the 14 and 18 GHz bands. Both designs employ a multistage self biased configuration with inductive source feedback on the first stage in order to achieve optimum noise figure associated to good input VSWR. A trade-off was necessary in dimensioning the inductive feedback, in order not to heavily reduce the gain of the first stage, since an insufficient gain would imply a higher contribution of the second stage in terms of noise figure.

The FETs' periphery and bias condition have been selected in order to optimise noise figure performance. Raised gate bias is employed through resistor dividers connected to supply voltage and bypassed with capacitors. Gate to source voltage can be reduced or enhanced using bondable pads which allow to insert or drop off a resistor in the source to ground path. This allows to compensate for pinch-off voltage variation or simply change the devices' bias condition for total performance optimisation.

The noise figure analysis has been done inserting two correlated current sources in the device small signal model, following Van Der Ziel equations [4] in which the process dependent parameters P and R have been extracted from the measured data with a simple optimisation routine over the bandwidth of interest.

The 14 GHz LNA is a two-stage design whereas the 18 GHz uses three stages to achieve the required gain and bandwidth. The gain is 14 dB typ. over 6 GHz BW with 2.0 dB and 2.4 dB noise figures respectively. The 18 GHz LNA layout and measurement are shown in fig. 2 and fig. 3 respectively. The NF measurement shown includes a 0.2 dB contribution of the test jig to be deembedded.

*2. Variable Gain Amplifier (VGA).*

The VGA is composed of three self-biased stages of amplification with an embedded analog attenuator. The

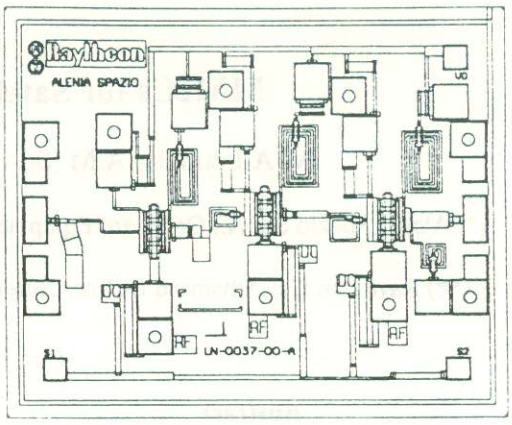


Fig. 2 : 18 GHz LNA Chip Layout.

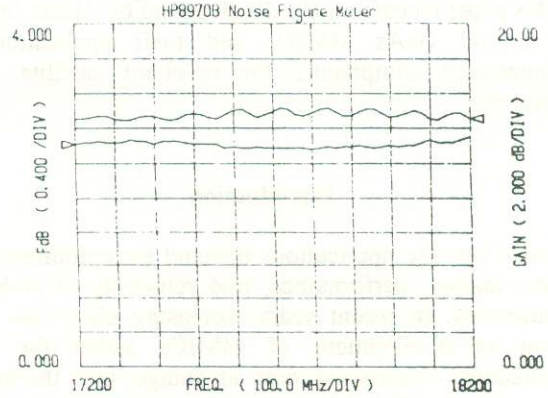


Fig. 3 :14 GHz LNA Measured Performance.

wide range of applications for this circuit imposed strict performance requirements on each of the three stages. Choice of FET periphery and bias conditions were critical throughout the circuit in order to meet all electrical specifications while simultaneously minimising DC current consumption. A 200um final stage biased for class A performance, and 150um driver stage and 100um input stage biased at 25% Idss were chosen to realise these requirements. Design of the output matching network and second interstage was governed by the overall gain and compressed output power requirements. The input matching network was designed to meet the input return loss and noise figure specifications. Concurrently meeting these two sets of requirements resulted in nearly all gain shaping (needed to achieve a gain ripple of less than .5dB over the BW) having to be done in the first interstage, which in turn placed a heavy burden on the performance of the first stage FET. The analog attenuator design was based on a broadband extended T design. This approach was chosen because of its minimal VSWR variation and flat gain response over the attenuation range. The effects of the intrinsic variations of the attenuator were further reduced by inserting it between the second and the third stage of the amplifier. Since dual voltages are needed to drive the attenuator a low current driving circuit has been also incorporated on the chip. The maximum measured gain and ripple for the VGA are 12 dB and 0.5 dB over the whole bandwidth. The attenuation dynamic is greater than 21 dB over 3 V control voltage range. Figg. 4 and 5 show the chip layout and measured performances respectively.

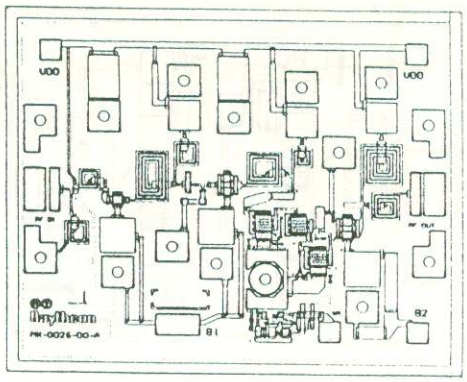

Fig. 4 : VGA chip Layout

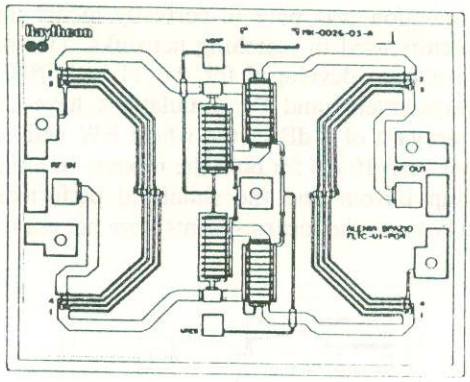

Fig.6 : FC Chip Layout.

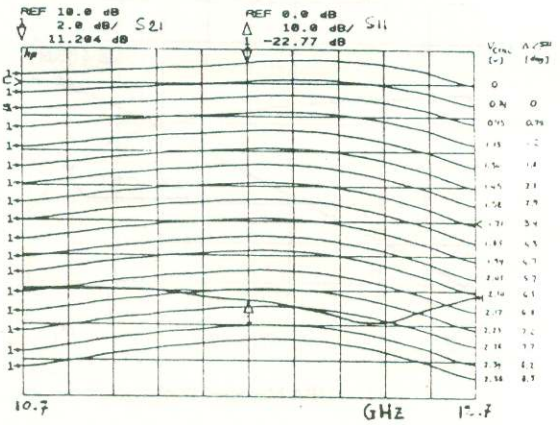


Fig.5 : VGA Measured Performance at several control voltages.

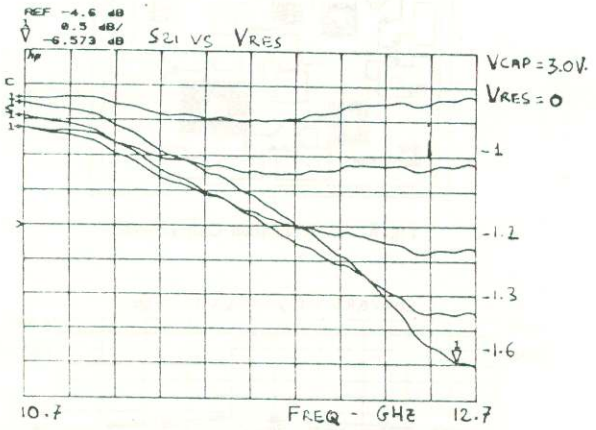


Fig.7 : 10.7-12.7 GHz FC measured response.

*3. Flatness Corrector (FC).*

As already stated above this circuit must be able to control the gain slope variation consequent to the complete system assembling. Therefore it has to be versatile and simple enough to allow a complete slope control inside the bandwidth and to preserve the system electrical performance.

Keeping in mind these considerations, the circuit has been conceived as a simple RCL resonant circuit in which a variable "Q Factor" and a variable resonance allow to obtain a slope value control in several points of the bandwidth. A sort of balanced configuration with two such circuits inserted between two Lange couplers has been used in order to get a good isolation.

A cold MESFET approach has been used to implement the variable capacitor and resistor. An appropriate choice of the MESFET's areas allows to make the capacitor to resonate a small microstrip line between 10.7 GHz and 12.7 GHz thus obtaining the control of the maximum slope position in the bandwidth, and to dimension the resistor in order to vary the slope value up to 2.5 dB/500 MHz. As shown in Fig.6, The two Lange couplers have been folded in order to make the chip dimensions compatible with the other chips. The measured performance is shown in Fig.7.

*4. Mixers.*

A gaining mixer solution has been chosen with the aim to optimise the overall front-end noise and gain performance. A Dual-gate MESFET was preferred as active device because of its inherent capability to obtain isolation between LO and RF inputs without using large size filters, and a little gain with respect to a Single-gate approach. A self-biased configuration with both gates connected to ground and an inductive load for the drain has been used. The IF matching network has been optimised to get the maximum conversion gain while the inductive load assures a low impedance at LO frequency. An image filter has also been studied and incorporated in front of the RF input. The main drawback of this circuit is represented by the presence of strong spurious near the IF spectrum (due to the low LO frequency) which can not be eliminated with the usual optimisation techniques[4]. On the other hand a double balanced approach would increase power consumption and complexity without a great improvement in spurious rejection.

For a successful design it was essential to accurately model both active and passive elements. The dual gate structure has been modelled with a cascode configuration and Materka equations have been used to model the single device. The intrinsic model was then modified to fit measured behaviour under RF operation and at various bias conditions. As far as concern the passive structures,

special attention was paid to correctly model the large size inductors used in matching networks. Two different chips have been developed for the 14 and 18 GHz RF bands respectively, and the simulations have shown a conversion gain of 4 dB in the whole BW with a return loss better than 10 dB for both the mixers. In Figg. 8 and 9 the chip Layout and the simulated performance are reported because the measurements were not ready.

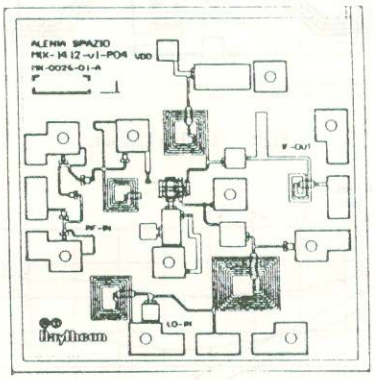

Fig. 8 : 14 GHz Mixer Chip Layout.

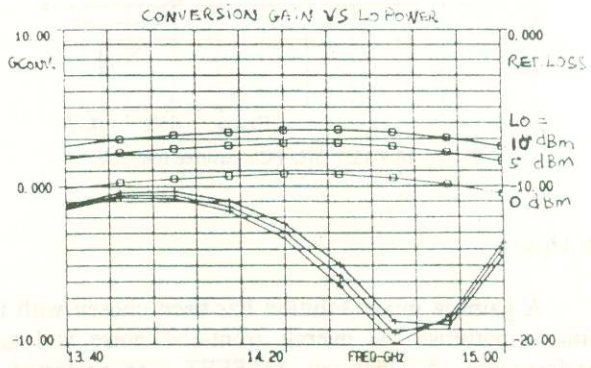


Fig. 9 : 14 GHz Mixer Simulated Performance.

*5. Medium Power Amplifier.*

The circuit design is single-ended and consist of a two stage amplifier over a 34% bandwidth centered at 11.75 GHz. Output FET gate periphery was selected to achieve a 32 dBm third order intercept point and was to have a channel temperature below 110 °C. A lossy reactive matching network approach was necessary to simultaneously provide an input/output return loss better than 20 dB, a peak to peak gain ripple less than .5 dB, and a minimum gain of 11 dB over a temperature range of -10 to +75 °C. The amplifier is self biased in order to compensate gain variation with the temperature, and is intended to operate from a 7.0V. supply. A 600um and 1200um FET periphery has been chosen for the first and second stage respectively and a semi-lumped approach has been used to implement input, output and interstage networks. A plot of the circuit layout is shown in fig. 10 whereas the measured performance are reported in fig. 11.

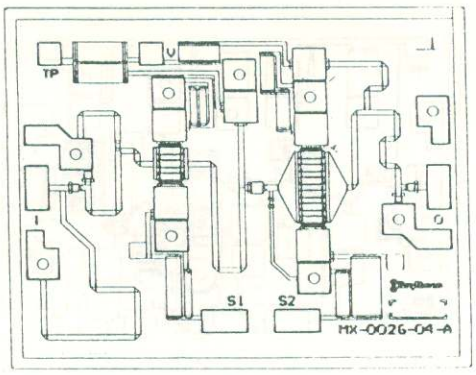


Fig.10 : MPA Chip Layout.

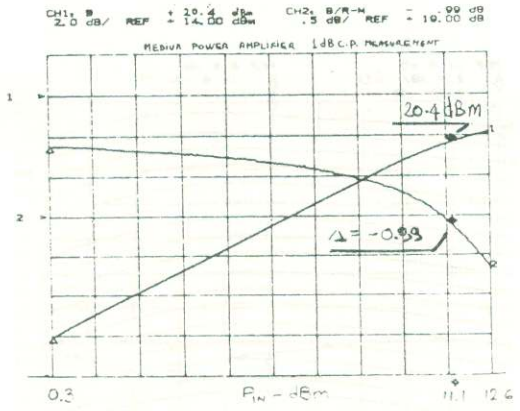


Fig.11 : MPA Measured Performance.

## Conclusions

A modular rather than multifunction MMICs approach has been used to help miniaturised satellite TLC equipments realization. A set of seven suitably designed GaAs MMICs has been shown to cover the needs for the development of three such equipments and finds application in several other areas. All chip dimensions are 2.0x1.6mm (except for the mixers). The measurements shown have been done using "test-jig" arrangement rather than probed on wafer, and include the interconnection effects, accounted for in the design.

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