SUB-MILLIWATT DC POWER INJECTION LOCKED QUADRATURE LOCAL OSCILLATOR AT 950 MHZ

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Abstract

A low power local oscillator with a free running frequency of 950 MHz and a DC power consumption of less than 1 mW has been designed. It can be locked with a single or differential -30 dBm lock signal on the second harmonic and uses no dedicated lock transmission gate. The fully differential circuit employs a two stage ring oscillator and provides the possibility of using differential I- and Q-outputs.

Introduction

In image rejecting down converters or direct conversion receivers for mobile communication the first LO has to provide accurate quadrature outputs. Any difference in phase and/or amplitude of the two LO outputs will degrade the image rejection. By using a two stage ring oscillator with identical stages providing an accurate 90° phase shift each, such errors can be reduced. The rejection of the unwanted sideband will then mainly depend on the matching of the two stages.

The ring oscillator can be locked by a signal on the second harmonic of the free running frequency f_0. This locking brings the problem of generating a reference signal at twice the operating frequency ($f_{ref}/2=f_0$), which is not very power efficient in most cases. The lock mechanism also works with a signal only having harmonics at the desired lock frequency ($n*f_{ref}/2=f_0$). Using the odd n-th harmonic as a reference signal allows a reference with no harmonics on the final oscillation frequency. This is very important when designing sensitive coherent receivers where any leakage of the reference oscillator into the signal path could block the receiving amplifiers.

To allow operation on different channels, the lock range must be wide enough to pull the oscillator to the desired frequency.

For battery operation, a very low DC-power consumption was a major design goal.

Design

The circuit consists of two identical differentially amplifying inverter stages connected in series. The non-inverting output of the second amplifier is connected to the inverting input of the first amplifer. This topology provides an extra 180° phase shift (Fig. 1) and prevents any oscillations or lock up at low frequencies or DC where the inverters could have an exact 180° phase offset.

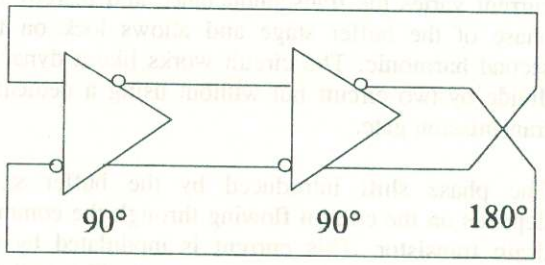

Fig. 1: Two stage ringoscillator

The realized circuit is designed with two identical differential enhancement FET (E-FET) amplifier stages with an active/passive load combination. A source follower with diode level shifters acts as an output buffer of the differential stage. Because of the small diode dimensions (3 µm) and the resulting high parasitic resistance, the level shifters are bypassed with capacitors (Fig. 2).

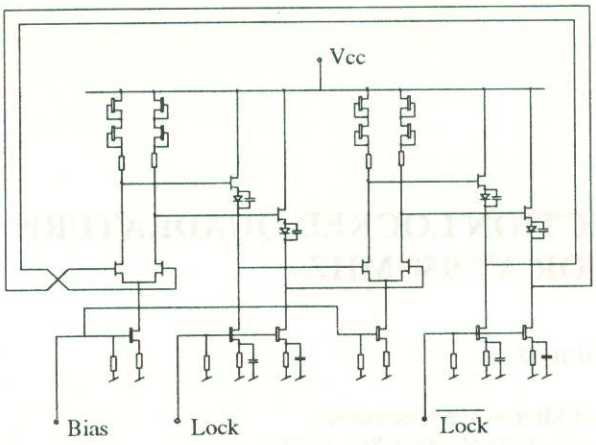

Fig. 2: Oscillator circuit schematic

The differential E-FET's combined with the output conductance of a single depletion FET (D-FET) load provide a relatively low gain. To increase the gain, a special load combination is requested. Two D-FET's are placed in series with a load resistor providing high load resistance as well as a low voltage drop.

The design of the current source of the differential amplifier requires special attention. If the output conductance of the current source transistor is twice as large as the conductance of the load, the full circuit enter a state where the outputs of the first stage both remain high and the outputs of the second amplifier remain both low. To avoid this problem, the common mode amplification must be reduced by resistive feedback in the current source.

The lock signal is fed into the circuit via the current source transistors of the common drain buffers. This current varies the transconductance and thereby the phase of the buffer stage and allows lock on the second harmonic. The circuit works like a dynamic divide by two circuit but without using a dedicated transmission gate.

The phase shift introduced by the buffer stage depends on the current flowing through the common drain transistor. This current is modulated by the injection of the lock signal current. The variable phase shift ϕ_{buffer} of the buffer stage is

$$\phi_{buffer} := \phi_{max} \cdot \sin\left(\omega_{lock} \cdot t + \phi_0\right) \qquad (1)$$

where ϕ_{max} is the maximal possible phase shift, ϕ_0 is a constant offset and ω_{lock} is the frequency of the lock signal. ϕ_{max} depends on the amplitude of the lock current and limits the locking range. The total phase ϕ_{tot} of the two inverter stages is

$$\phi_{tot} := 2 \cdot \phi_{diff} + \pi + \phi_{buffer} \qquad (2)$$

where ϕ_{diff} includes the phase shift of one differential stage and the constant part of the phase shift introduced by one buffer stage.

The time t needed to pass once through the ring is

$$t := \frac{\phi_{tot}}{\omega_{osc}} \qquad (3)$$

Form the equations (1) and (3), we can see that (2) only becomes constant for several passes through the ring if ω_{lock} is a multiple of ω_{osc}. This constant phase shift indicates that the oscillation is locked to the reference, because at all other frequencies, the phase condition $\phi_{tot}=k \cdot 2\pi$ for sustained oscillation is not fulfilled.

The sources of the current source transistors are blocked with 0.1 pF on chip capacitors. This results in a higher lock range because of the amplification of the lock signal. Locking on a harmonic of the lock signal is possible as long as this signal is strong enough to produce the desired harmonic by using the nonlinear transfer characteristic of the current source transistor.

The bias points of the circuit may be adjusted by accessing the gates of all the current source transistors. With access to these gates, the constant part of the phase shift introduced by the buffer stages can be adjusted and therefore the free running frequency of the ring oscillator is varied.

In the implemented test circuit no off chip output was provided, in order not to add any additional parasitic capacitances. The chip was analyzed by measuring the AC feedthrough in the unblocked power supply line (Fig. 3).

The simulated single ended internal voltage swing of 400 mVpp is enough to modulate an E-FET Gilbert cell mixer.

Measurements

The circuit presented in this paper was designed using the TriQuint QED/A process with GaAs E- and

D-FET's. The FET gates measure 0.7 µm x 3 µm. The chip size is 0.5 mm x 0.5 mm.
The measurements were made using a HP 70900 spectrum analyzer connected via a bias tee to the Vcc pin and a Marconi 2042 Signal generator as lock signal source (Fig. 3).

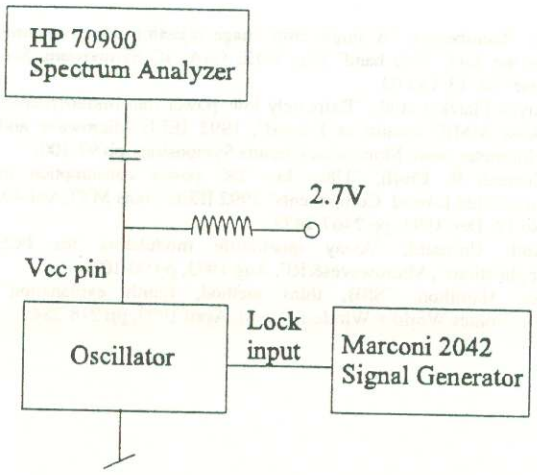

Fig. 3: Measurement setup

First, the chip was measured with no lock signal applied. The chip has a free running frequency of 950 MHz with a jitter of approx. 5 MHz (Fig. 4). This large jitter leads to the conclusion that the Q of the resonance is fairly low. This is a disadvantage only when using the oscillator as a free running device. When a lock signal is used, the low Q of the circuit enlarges the lock range considerably because the lock signal can vary the phase of the common drain buffer stage only for a limited number of degrees.

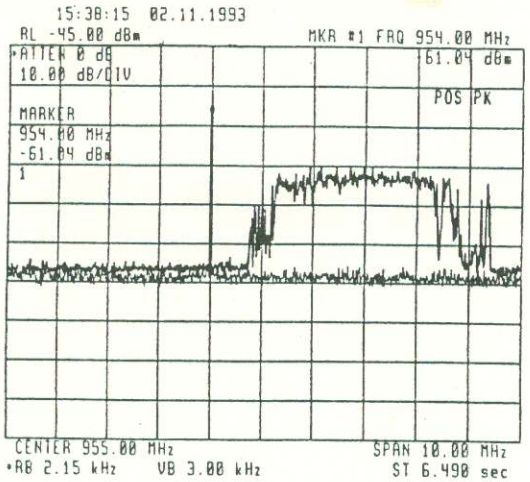

Fig. 4: Free running and locked oscillator

By injecting a single ended signal of -30 dBm at 1908 MHz, the oscillator is locked. The locked signal can be seen in Fig. 4 as a peak to the left of the free running signal.

Fig. 5 shows the jitter free output of the locked signal at half of the lock frequency. It was measured with a single ended -30 dBm lock signal at 1908 MHz applied at the lock input of the chip.

With a single ended lock signal power of -30 dBm, -20 dBm and -10dBm, the lock ranges at 950 MHz measure 16 MHz, 60 MHz and 200 MHz respectively.

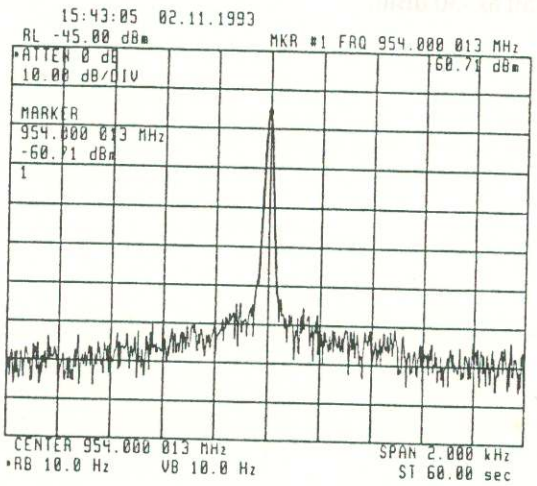

Fig. 5: Jitter free output of the locked signal

The chip was also measured with a subharmonic lock signal. A Colby Instruments 1000A pulse generator was used to generate harmonics of the lock signal coming from the Marconi 2042 signal generator. With this method the oscillator can be locked by a signal with a frequency which lies at the free running oscillation frequency divided by a factor of 3.5. For an even higher division factor, the lock signal must be high pass filtered. This way, the division ratio of the lock signal frequency to the free running frequency can reach 8.5. Thus, for a 950 MHz oscillation frequency a reference signal at 111 MHz in conjunction with a harmonic generating circuit may be used. Such a low power circuit makes the use

of power consuming high frequency prescalers no longer necessary.

Additionally, the reference signal and its harmonics have no signal energy at the frequency of oscillation.

The chip draws 318 µA from a single 2.7 V power supply. The total DC power consumption is therefore 860 µW.

Conclusions

A very low power injection locked local oscillator circuit with a free running frequency of 950 MHz has been fabricated using a standard MESFET process.

This circuit has a lock range of up to 200 MHz and can be locked with a frequency that is a factor of 8.5 times below the oscillation frequency. The DC power consumption is 860 µW while the lock signal may be as small as -30 dBm.

This type of oscillator could be used in image rejecting and zero-IF downconversion systems because of the 90° phase relationship of the two oscillator stages.

References

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