Expert System Techniques Applied to MMIC Layout Including Intercomponent Coupling

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Abstract

This work reports research progress on **GALA** (**G**allium **A**rsenide **L**ayout **A**ssistant), a novel knowledge based system for MMIC layout, which has the aim of reducing GaAs real estate usage thereby increasing yield and reducing cost. The blackboard architecture using multiple knowledge sources has been combined with design rules derived from electromagnetic simulation to assist the layout engineer.

Introduction

The application of AI techniques to GaAs chip layout will have the advantage of a higher probability of right first time design. This will prove attractive to small companies or academic institutes who lack experienced GaAs MMIC engineers. Prior work within our research group has concentrated on applying artificial intelligence techniques to two key areas of MMIC design; (i) **ADAM** (**A**mplifier **D**esign **A**ssistant for **MMIC**s)[1] is an expert system operating at the circuit synthesis level and (ii) **GALEDA** (**G**allium **A**rsenide **L**umped **E**lement **D**esign **A**ssistant) [2,5], which post processes the synthesised circuit schematic to account for foundry dependent MMIC component parasitics.

When laying out a MMIC an engineer has several constraints to adhere to and must use expert advice and a variety of commercial software packages to find the optimum solution (figure 1). By combining GALA with the other MMIC expert system tools already developed, ADAM and GALEDA, a design suite is created which operates on one platform. This takes account of expert opinion and process constraints and brings versatility and flexibility to the existing design methodology (figures 2 and 3).

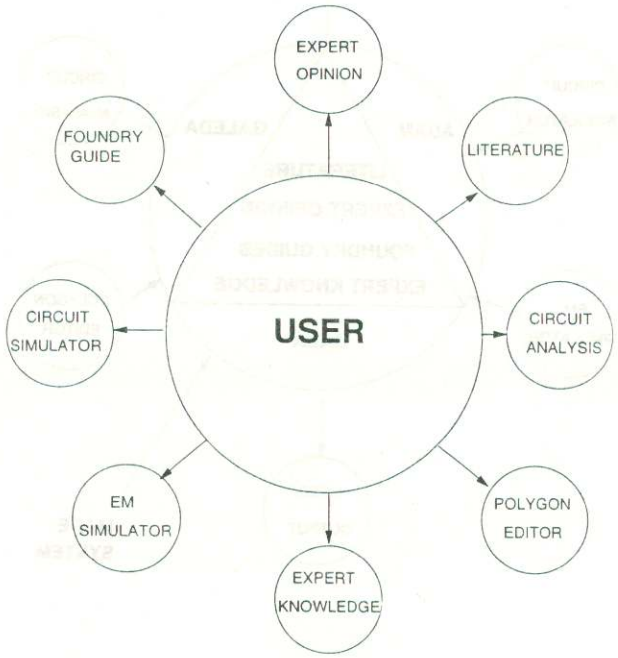


Figure 1. Current design methodology requiring familiarity with a range of software combined with knowledge harvesting from experts under foundry constraints

Application of Artificial Intelligence to Layout

The knowledge sources which make up MADE (MMIC Automated Design Environment) are shown in figure 2. Knowledge has been harvested from a variety of sources to develop the top down design rules; including experts, literature and foundry guides. Circuit synthesis, design and layout do not make use of either circuit or electromagnetic simulators but instead make use of heuristic design rules held in the knowledge base [3].

Each expert system knowledge base covers one particular aspect of the MMIC design process. Figure 3 shows how the layout tool, GALA, forms the last phase in closing the design loop to produce MMIC artwork ready to go for mask generation. GALA has been written using PROLOG under the UNIX operating system on a SUN workstation. This permits simple integration with GALEDA and ultimately with ADAM which was developed on a PC under the Windows™ environment.

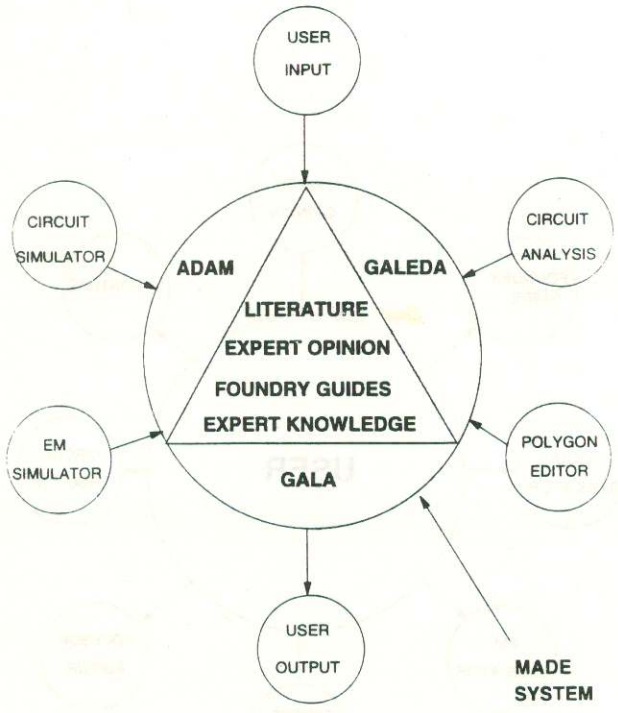
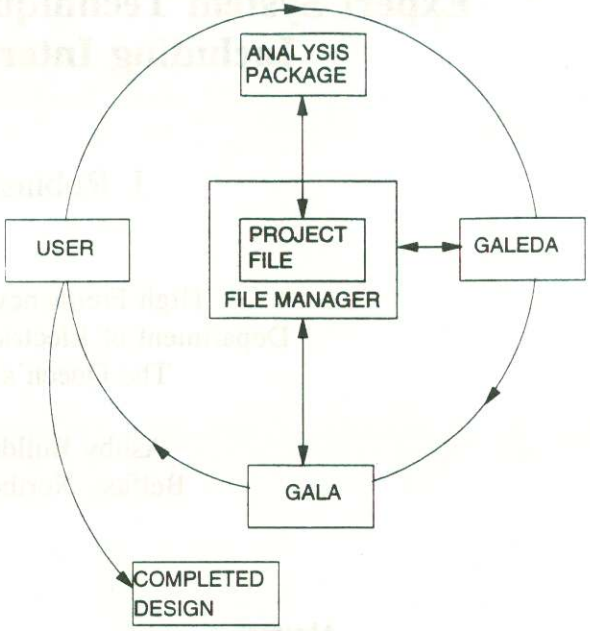


Figure 2. Development of three interrelated expert systems for MMIC Designs illustrating the sources for knowledge harvesting and integration with third party software.



SYSTEM LOOP FOR MODELLING AND LAYOUT
SECTION OF MADE

Figure 3. Inclusion of the user in a design/layout loop involving the expert systems GALA and GALEDA. A MMIC layout including the effects of parasitics and intercomponent coupling is synthesised.

The blackboard architecture [4] offers GALA the best solution to the difficult MMIC layout problem. Multiple knowledge sources are each dedicated to different aspects of the layout problem for which they have specific rules. For example KS1 is dedicated to finding connections of L and R in the circuit schematic supplied by GALEDA and KS2 is dedicated to connecting L and C and so on.

The results from the knowledge sources are then placed on the blackboard (figure 4) indicating size and orientation of placement for observation by the other knowledge sources. The monitor/scheduler controls access to the blackboard by each knowledge source.

Each combination of two components forms a supercomponent. At a higher level other knowledge sources connect supercomponents together to produce the final layout which is back annotated in the netlist.

Expert system tools have the advantage that they can be applied to different foundries using alternative knowledge bases. The problem of knowledge harvesting has been

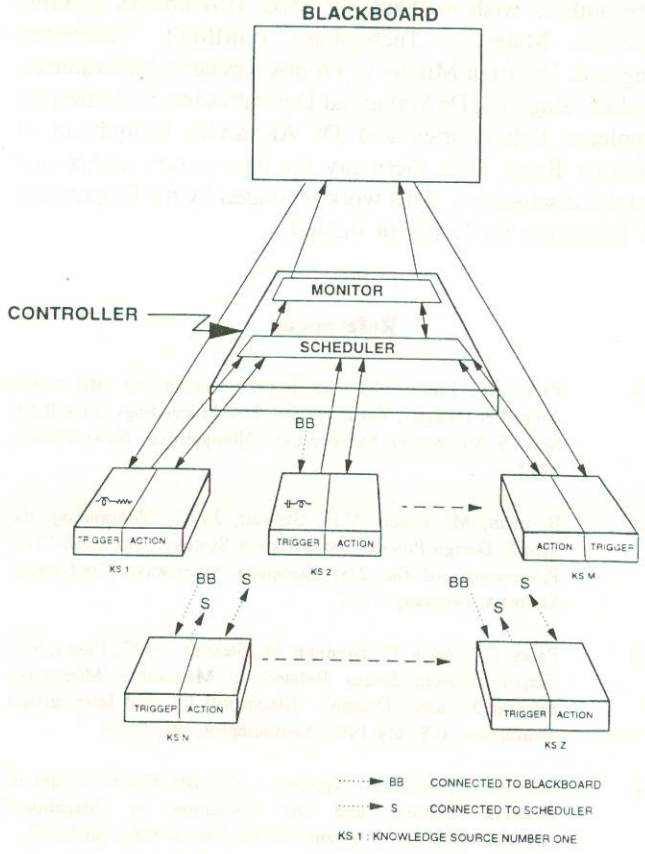


Figure 4. Blackboard architecture used to control component connectivity, routing and placement.

addressed. Experienced circuit designers have been interviewed to gauge their rules of thumb for layout. From experience they were able to show the reasoning for closeness of lines and components, but were unable to justify their reasoning using either statistical process data or EM simulators.

Simulation

As MMIC processes improve, the useful frequency limit will increase. Expert opinion indicates that inter-component coupling will significantly affect circuit performance as component spacing decreases. Simulation has shown the complicated field pattern existing between microstrip lines and passive components as they are moved close to the line violating existing design rules. The decrease in characteristic impedance due to asymmetric line effects has been noted and is being investigated further.

At high frequencies, meander lines are used to provide extra phase length for MMIC matching problems. Simulations have highlighted a problem in the current distribution at meander line corners where the evanescent modes generated increase interline coupling.

Problems exist in modelling the evanescent modes which occur at mitred right angle bends and the coupling between adjacent lines which cause changes in electrical length. These will be addressed in the future combining the best of circuit and electromagnetic simulators (Explorer™)

The Layout Process

GALA is applied to the schematic circuit netlist following the generation of standard and custom cells, including non ideal foundry parasitics, by GALEDA. The position, orientation and component connectivity are compiled to an ASCII file and this information is transferred to a commercially available polygon editor Wavemaker™ or Cadence Analogue Artist™ which then produces a GDSII file for mask preparation.

Validation

A mask has been designed to test the design rules generated from multiple electromagnetic simulation runs. The initial measurements will be made on coplanar waveguide circuits fabricated on 500μm thick GaAs process trial wafers with a 3μm aluminium metallisation. A further set of microstrip coupled lines are being fabricated using the F20 GMMT process under the Eurochip programme. The coupling effect between microstip lines and spiral inductors is currently being simulated and will be measured experimentally when test structures are returned from the GMMT foundry. The spiral inductor under consideration is shown in figure 5.

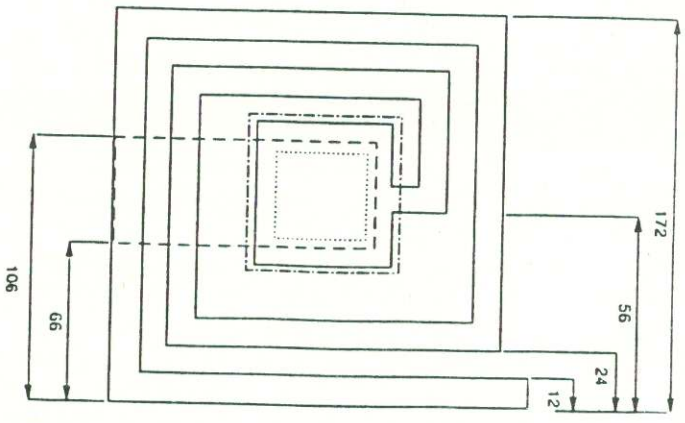
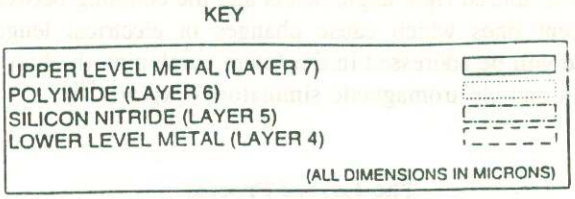


Figure 5. Plan view of GaAs planar MMIC inductor designed for the GMMT F20 Process used for EM analysis of self resonant and coupling effects

Table 1. Design specification for the spiral inductor of figure 5.



	DEPTH	DIELECTRIC CONSTANT
UPPER LEVEL METAL (LAYER 7)	3.20	-
POLYIMIDE	135.00	3.4 +/- 0.2
SILICON NITRIDE	12.00	7.2 +/- 0.3
LOWER LEVEL METAL (LAYER 4)	0.51	-

Conclusions

The GALA layout tool has been described and the software techniques used to develop and control the multiple knowledge sources have been discussed. It is proving effective in locating the ideal position, orientation and geometry of standard cells created from the prime schematic. Intercomponent coupling is being addressed and has indicated a number of interesting effects which are currently being examined in more detail.

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