Novel topologies for MMIC four-quadrant multipliers for T/R wideband systems

Stefano D'Agostino, Piero Marietti, Nunzio Renzella, Alessandro Trifiletti

Dipartimento di Ingegneria Elettronica, Università degli Studi di Roma "La Sapienza",
Via Eudossiana 18, 00184 Roma, Italy

Abstract

In this paper we present a new topology of a nonlinear core for 4-quadrant analog multiplier suitable for high-speed operation that is insensitive to input common-mode signals and can be implemented by MMIC GaAs process.

Introduction

Analog multipliers are essential elements in high-speed data processing and communication links as they can act as frequency shifters, modulators and phase detectors [1]. The multipliers we have examined are based on the quadratic law between gate-source voltage and drain current in MOS devices. This characteristic still holds in D-mode MESFET and HEMT with gate-length smaller than 1 μm. It should be noted that frequency performance of multiplier is limited both by parasitic capacitances of active devices and by differences in lengths of signal paths from the module inputs to nonlinear elements. These mismatches cause phase errors which introduce frequency dependent errors. Advanced MMIC processes make available small devices and allow to obtain compact layouts to reduce such mismatch. The block scheme of the multiplier that will be considered is shown in Fig. 1.

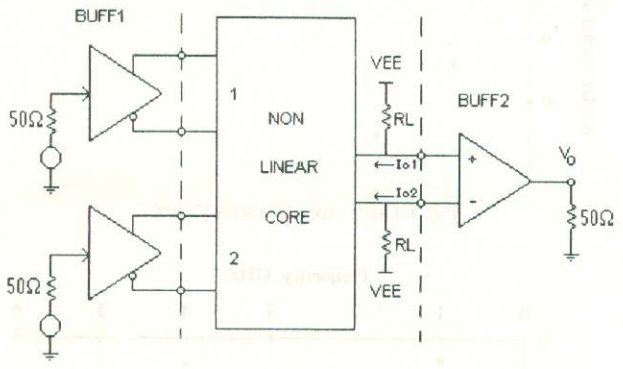

Fig. 1. Block scheme of the multiplier.

The input stage BUFF1 is used to convert a single-ended input signal in a purely differential one and to supply bias level to nonlinear core. The nonlinear core has to be driven nominally by purely differential voltages and its output must be read by a differential to single-ended buffer to eliminate spurious terms. Output buffer BUFF2 has to eliminate all common-mode terms and drives a 50Ω load.

In microwave frequency range it is not trivial to obtain single-ended to differential buffer [2], so we have focused our analysis on the problems of interfacing buffer stages to nonlinear core and of stating the requirements of the buffer stages.

We have performed our simulations using as active devices MESFETs with 0.5 μm gate-length from F20 GEC-Marconi GaAs process. These devices are characterised by a Curtice-Cubic model [3] whose parameters are available in the foundry manual [4].

Priciple of operation of nonlinear core

The nonlinear core is based on a simple structure which obtains the product of the input signals as the difference of two squared linear combinations of them

$$V_o = (V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2. \quad (1)$$

Each term of the difference can be obtained using the inherent square law of drain current for MESFET operating in the saturation region:

$$I_{DS} = \beta(V_{GS} - V_T)^2. \quad (2)$$

Applying two signals to gate and source we obtain a drain current proportional to the square of their difference

$$I_{DS} = \beta(V_1 - V_2 - V_T)^2. \quad (3)$$

To eliminate all spurious terms from (3), it is necessary to use two cells as the one is shown in Fig. 2.

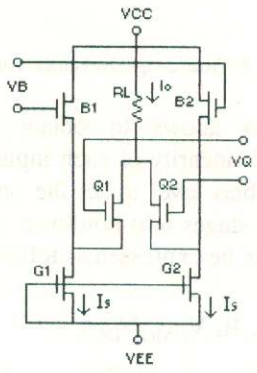

Fig. 2. Squaring cell.

With the purpose of clarifying the influence of common-mode signals in the operation of each cell we set:

$$V^1_{GSQ} = V_{DMQ} + V_{CMQ} - \left(V_{DMB} + V_{CMB} - V_{GSB}\right) \quad (4)$$

$$V^2_{GSQ} = -V_{DMQ} + V_{CMQ} - \left(-V_{DMB} + V_{CMB} - V_{GSB}\right) \quad (5)$$

where DM indicates differential-mode and CM common-mode, Q stands for squarer and B for buffer. Under the assumption of high scaling ratio of the couple buffer-squarer ($\beta_B >> \beta_Q$) and of negligible output conductance of the MESFETs it is possible to assume a constant voltage drop V_{GSB} on the source follower also in presence of signals. Using the (2), (4), (5) we can evaluate the output current of a single cell:

$$\frac{2I_{OUT}}{\beta_Q} = V^2_{DMQ} + V^2_{DMB} - 2V_{DMQ}V_{DMB} + V^2_{CMQ} + V^2_{CMB} + V'^2_{GS} + 2V_{CMQ}V'_{GS} + -2V_{CMQ}V_{CMB} - 2V_{CMB}V'_{GS} \quad (6)$$

this equation will be used to compute the final output of the multiplier. To eliminate spurious terms in output signal due to the squares of input voltages and due to the cross-products of threshold voltages it is possible to use the differential topology [5] shown in Fig. 3 made by two cells each one evaluating a squared term of the difference (1).

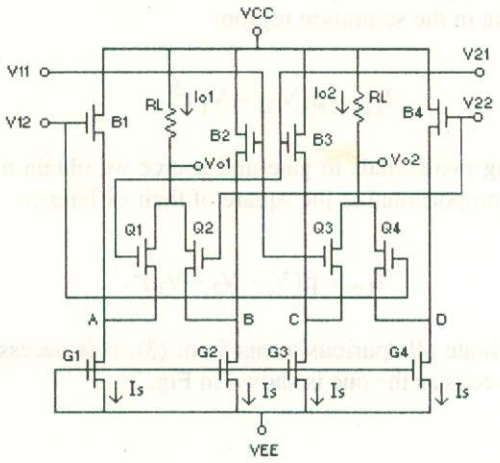

Fig. 3. Cross-coupled nonlinear core.

This configuration allows to obtain equal frequency response and equal linearity of each input and permits the usage of a single bias level to set the operating points of squarer and buffer stages into nonlinear core. Final output of the multiplier can be expressed as follows.

$$V_O = 2\beta_Q R_L V_{DMQ} V_{DMB} + +2\beta_Q R_L \left(V_{GSB} - V_T\right)\left(V_{CMB} - V_{CMQ}\right) \quad (7)$$

The output signal is affected by error terms due to the common-mode components of input signals. It should be noted that in our analysis we have assumed a unity transfer function of buffer stages. In reality we have an unsymmetrical processing of the signals inside the nonlinear core which causes spurious terms as will be explained in the following section.

A. Simulations

To check the performances of the cross-coupled configuration we have performed computer simulation with lumped element circuits under the conditions listed in Tab. 1.

Tab. 1. Simulation set-up.

$I_{BIAS\_Q} = 4mA$	$F1 = 1GHz$
$I_{BIAS\_B} = 16mA$	$F2 = 4GHz$
$W_B = 4W_Q$	$R_L = 50\Omega$

Where W_B and W_Q are respectively the gate-width chosen for buffer stages and squarer stages. We apply two sinusoidal signals of 1 and 4 GHz, with an amplitude of Vdm = 100 mV, with two different common-mode levels. The results are presented in Fig. 4 which is relative to a purely differential input signal and in Fig. 5 with a ratio Vdm/Vcm = 100.

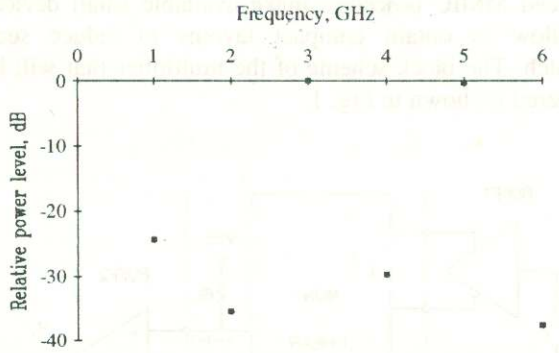

Fig. 4. Output spectrum with Vcm=0.

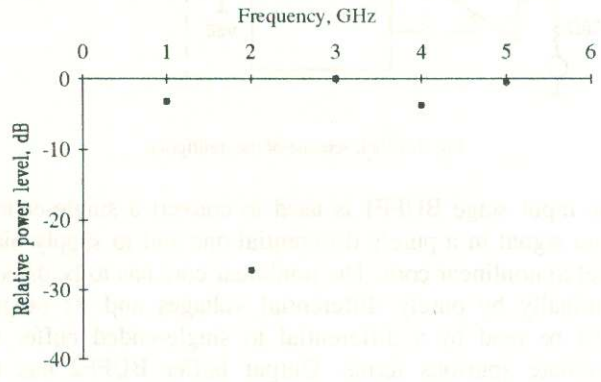

Fig. 5. Output spectrum with Vcm=0.01Vdm.

Even small level of common-mode signal causes a great error in the cross-coupled configuration and this can make difficult to implement such a topology in the microwave frequency range.

Our proposal

To reduce the influence of common-mode input signals we propose a different way to eliminate spurious terms in the output current of a single cell. As shown in Fig. 6 we connect the squaring cells without the crossings.

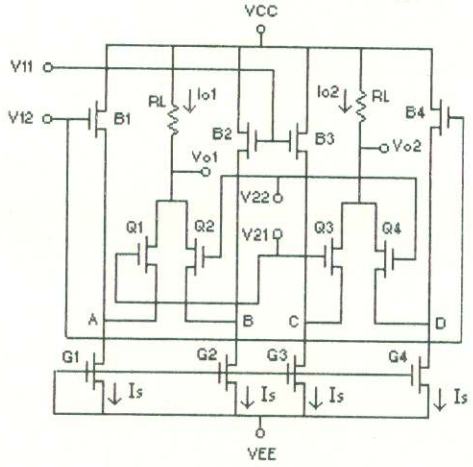

Fig. 6. Straight-coupled nonlinear core.

Under the same assumptions we have used to get (7), the output signal is given now by:

$$V_O = 2\beta_Q R_L V_{DMQ} V_{DMQ} \qquad (8)$$

with a full suppression of common-mode spurious terms. The following differences of this configuration with respect to the previous one, must pointed out:

A. Frequency response

This scheme permits to separate the slow input (buffer) from the fast one (squarer) improving overall frequency response.

B. Dynamic range

In this configuration without crossings the two inputs have different dynamic ranges, so it is possible to choose the input with the greater dynamic range to get the greater input signal, increasing the output voltage swing.

C. Reduced dynamical errors.

This topology eliminate some errors which are present in the cross-coupled one. In fact the squaring MESFETs of each cell are driven by the same signals. In Fig. 3 we can see that input signal v11-v12 appear directly on the gates of the right cell, while it is filtered by B1, B2 prior to reach the sources A, B of the left cell and similarly for the other input. Assuming purely differential input signals V_1, V_2 it is possible to consider the influence of the filtering action of the buffer stage considering the following error terms:

$$e_{cc}(t) = V_1^2 - (V_1 * h_B)^2 + V_2^2 - (V_2 * h_B)^2 \neq 0 \qquad (9)$$

$$e_{sc}(t) = V_1^2 - (V_2 * h_B)^2 - V_1^2 + (V_2 * h_B)^2 = 0 \qquad (10)$$

in the cross-coupled configuration error terms e_{cc} cannot be completely cancelled due to the low-pass characteristic h_B of buffer stage which breaks the symmetry.
We have performed computer simulations of this topology in the same input conditions of Tab. 1. The results are presented in Fig. 7 without common-mode signals and in Fig. 8 in the truly severe condition of Vcm = Vdm.

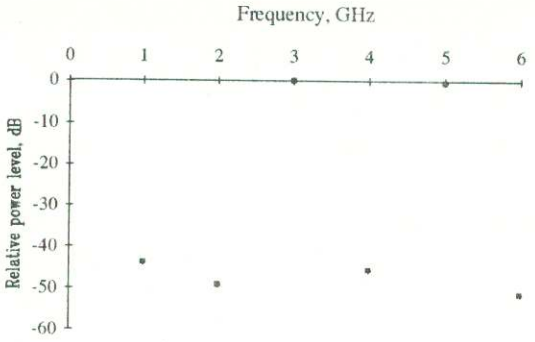

Fig. 7. Output spectrum with Vcm=0.

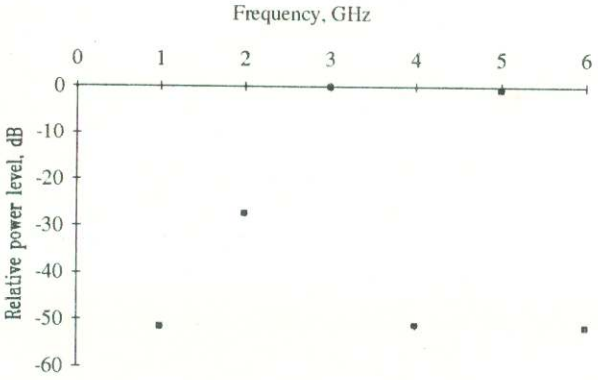

Fig. 8. Output spectrum with Vcm = Vdm.

The results of simulations shows an improved response in absence of common-mode components, and a great insensitivity to common-mode inputs. This configuration appears to be more robust and versatile than cross-coupled one and, with respect to the problems of input interfacing, it can be implemented with a few problems. Even if the simulations have been performed on lumped elements circuits the results appear to be promising. The usage of a MMIC design process with fully scalable and compact devices it is advisable for high speed application.

Conclusion

In this paper we have presented a nonlinear core which is almost insensitive to common-mode input signals and which can be implemented with standard MMIC GaAs process.

References

[1] S. Betti, F. Curti, G. De Marchis, E: Iannone, A. Trifiletti, "Stokes-parameter detection experimental results for polarization modulation coherent systems with low bit-rate-to-linewidth ratio," *Microwave and Opt. Tech. Lett.*, Vol. 6, No. 9, pp. 525-527, July 1993.

[2] C. Toumazou, D. G. Haigh, "Level-shifting differential to single-ended buffer circuits for GaAs MESFET implementation," *El. Lett.*, Vol. 23, No. 20, pp. 1053-1055, 24 Sep. 1987.

[3] W. R. Curtice, M. Ettemberg, " A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, Vol. MTT-33, No. 12, pp. 1383-1394, Dec. 1985.

[4] GEC-Marconi, GaAs IC Foundry Design Guide for F20 and F14 processes.

[5] H. -J. Song, C. -K. Kim," An MOS four-quadrant analog multiplier using two-input squaring circuits with source followers," *IEEE Jour. of Solid State Cir.*, Vol. 25, No. 3, pp. 841-848, June 1990.