On the Bias Point Selection for Improved Performance in Low Intermodulation Distortion Amplifiers

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Abstract

Conventional design techniques for low in-band intermodulation distortion GaAs MESFET amplifiers, generally indicate a bias-point equal or close to Idss/2 [1,2]. This quiescent point choice results from the will to maximise output current swing without severe distortion, which by no means necessarily implies a minimisation of small-signal intermodulation distortion.

The aim of this paper is to review this two types of distortion, and to give precise rules for bias point selection in the design of low IMD amplifiers.

I. Introduction

There is a broad range of applications for highly linear RF amplifiers, that spread from cable (or recently optical-fibre) TV distribution (CATV), to the incoming mobile-radio services. Also, many of the existing telecommunications systems are based in networks that rely on SCM, sub-carrier multiplex transport, and for which large amounts of work have been done on the subject of channel linearisation. All these systems are asked to handle very high dynamic range signals, i. e., they must be capable of treating its inputs without adding to much noise, or induced nonlinear distortion.

Among the last class of signal perturbation, stands the in-band intermodulation distortion, IMD, because of the known faced difficulty to eliminate it by simple linear filtering. In a Power Series, or Volterra Series context, this particular type of distortion can be attributed, to the system's odd nonlinearities, i. e., to the 3rd, 5th, ..., degree terms of the Taylor Series or Volterra Series nonlinear operator's model expansion [2]. This is the main reason why there has been an increasing interest to study and accurately model those nonlinear properties of the active devices, like MESFETs HEMTs or HBTs, normally used in system implementation.

The present paper is dedicated to the GaAs MESFET. It is primarily intended to give a contribution to the understanding of 3rd order IMD dependence on gate bias, and thus to provide precise rules on the low IMD amplifier's quiescent point selection.

II. MESFET IMD control by bias point selection

In a graph of output I/V characteristics of a GaAs FET, i.e. Ids *versus* Vds for various Vgs (see Fig. 1), four strong nonlinearities can be identified.

Two can be directly observed from those I/V plots, as their knees. The first one appears for low Vds voltages (V_k typically 1 to 1.5V), and has its origin in the transition from the FET's linear to saturation regions. The second stands for much higher Vds voltages (V_{BR}), as it results from gate-channel union breakdown.

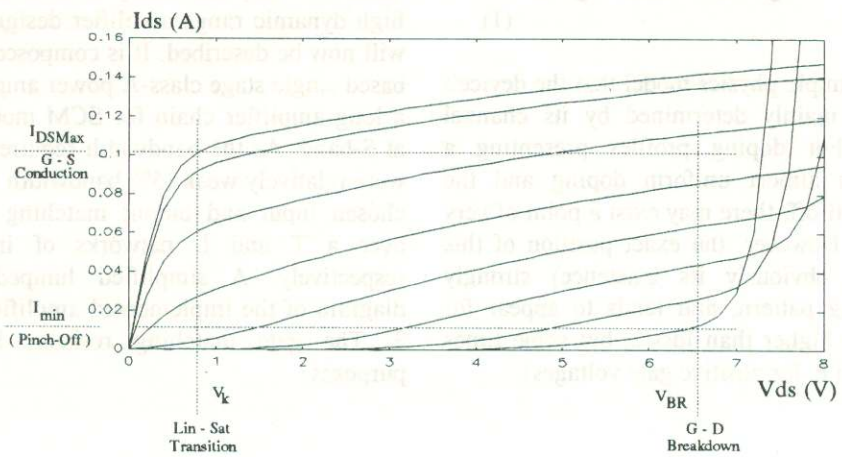

Fig. 1 - Typical MESFET output I/V curves.

The other two are related to the input network, i.e., to the dependence of Ids on Vgs. On the output I/V plots, they manifest themselves as sudden changes on the separation of the curves, and correspond to drain current pinch-off (Ids≈0), and maximum opening of the device's channel (Ids=I_{DSMAX}), respectively.

Those four strong nonlinearities define a rectangle on the phase-plane of (Vds,Ids), inside which the device is approximately linear. This means that if the signal excursion is not maintained inside those borders, its shape will be clearly modified, thus showing a severe distortion. However, it also means that even inside that zone the FET's I/V characteristics are not absolutely linear, but still present a residual curvature or mild nonlinearity. Two obvious conclusions arise from these facts. First, for low distortion applications the device should be biased comfortably inside that rectangle. And second, for maximised output signal excursion (or maximum output linear power [3]) the best quiescent point should be close to the figure's geometric middle point, i.e., $V_{DSQ}=(V_k+V_{BR})/2$ and $I_{DSQ}=I_{DSMAX}/2$. Nevertheless, this procedure does not guarantee an optimum IMD performance. In fact, for many high dynamic range applications requiring carrier to IMD ratios (C/I), some times greater than 40 or 50dBc, where the device is driven with signal levels reasonably less than its available maximum (class-A operation), the IMD performance can not be determined by those strong nonlinearities, since the signal excursions do not reach them, but by the referred residual or mild nonlinearities. For this C/I levels, it can be proved that IMD can be completely described as a 3rd order effect (its power rises with a slope of 3dB per 1dB of input power increase). Therefore, the optimum bias point is the one that minimises the 3rd degree coefficients of the Taylor Series representing the nonlinear elements' (Ids(V_{gs},V_{ds}) and Cgs(V_{gs})) dependence on the control voltages [4]. Expression (1) is such a bi-dimensional Taylor Series expansion for Ids(V_{gs},V_{ds}). For Cgs(V_{gs}) or Qg(V_{gs}), a similar one-dimensional expansion could be presented.

$$\begin{aligned} Ids(V_{gs},V_{ds}) = {} & I_{DS} + Gm.vgs + Gds.vds + \\ & + Gm2.vgs^2 + Gmd.vgs.vds + Gd2.vds^2 + \\ & + Gm3.vgs^3 + Gm2d.vgs^2.vds + Gmd2.vgs.vds^2 + \\ & + Gd3.vds^3 \end{aligned} \qquad (1)$$

It can be shown by a simple physics model that the device's IMD performance is mainly determined by its channel doping profile [5]. For doping profiles presenting a transition between an almost uniform doping and the channel to substrate roll-off, there may exist a point of very good 3rd order IMD. However, the exact position of this optimum point (and obviously its existence) strongly depends on the doping pattern, and tends to appear for drain currents slightly higher than Idss/2, but some times even higher than Idss (i.e. for positive gate voltages).

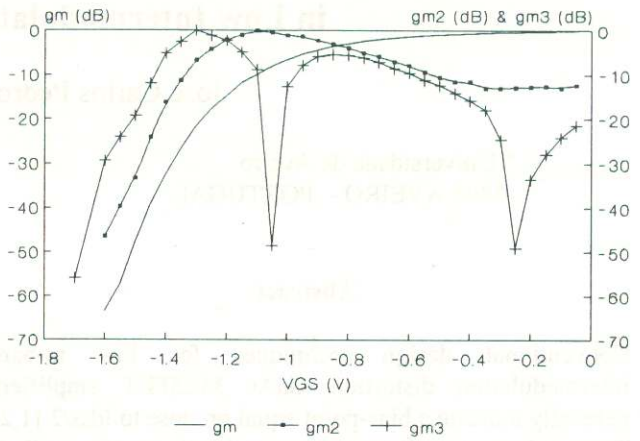

Fig. 2 - Normalised input distortion coefficients *versus* gate-source bias.

Fig. 2 presents values of Gm, Gm2 and Gm3 normalized to their maxima (measured in a general purpose MESFET with the method described in [4]). These figures are proportional to the most important contributions of fundamental, 2nd and 3rd order IMD output powers, respectively, when the device is drive by an unity voltage source. It can be concluded from this graph that, contrary to the 1st and 2nd order powers, the 3rd order component does in fact present two nulls, one for very low Vgs values, near the FET's pinch-off, and another near Vgs 0V. The first is almost useless for IMD amplifier applications because the associated low transconductance, and hence, power gain available from that region. On the other hand, the second null is not marked by this drawback, as it appears in the zone of almost "saturated" transconductance. It can be shown that this null corresponds to the IMD optimum bias point referred above from physics considerations [6].

III. An experimental example

In order to illustrate the concepts above explained, and to show how they can really be used on RF and microwave high dynamic range amplifier design, a practical example will now be described. It is composed by a GaAs MESFET based single stage class-A power amplifier, intended to end a long amplifier chain for SCM mobile-radio applications at S-band. As the bandwidth requirements, for this design were relatively weak (5% bandwidth for a +1dB ripple) the chosen input and output matching networks were build over a T and L networks of inductive components, respectively. A simplified lumped element schematic diagram of the implemented amplifier can be seen in Fig. 3. The gate matching resistor, Rg, has stabilisation purposes.

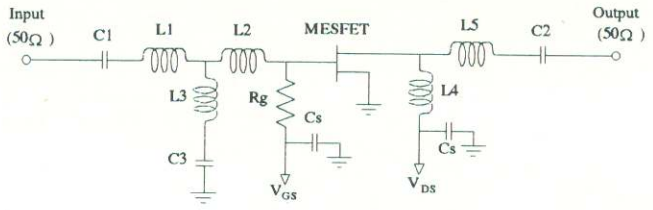

Fig. 2 - Simplified schematic diagram of the implemented prototype.

The laboratory IMD performance evaluation of this design was made following a conventional two-tone test. The necessary two signals were derive from the combination of highly pure sources, with equal output powers. They were tuned to met the amplifier's centre frequency - 2GHz -, and were separated by 10MHz..

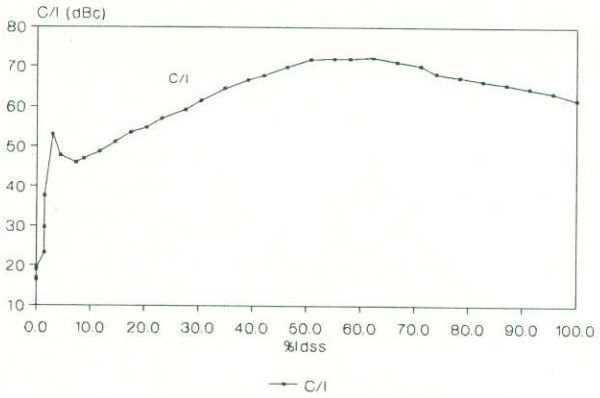

Fig. 4 - C/I performance vs current bias.

Fig. 4 represents carrier-to-intermodulation ratios, C/I, *versus* quiescent current, % Idss bias. In the useful range of I_{DS} values, i. e., from about 20% Idss to 100% Idss, this device presents a C/I variation of near 15dB, reaching a 72dBc maximum (0dBm output power) for an optimum I_{DS}≈60% Idss. Although in this case there exists a fairly broad zone of biases where C/I performance is quite good, it has been previously observed that sharper patterns are also possible, depending on the device and operating frequency. In fact, frequency determines the magnitude of the Cgs(Vgs) IMD contribution, and also the relative phase of IMD components due to the various terms of (1) depending on vgs and vds. Thus, it should be expected that for very high frequencies the phasorial sum of all distortion contributions will hardly be a strong null, like the one of Fig. 2, even if all 3rd order coefficients of (1) and Cgs(Vgs) present points of zero.

On the other hand, Fig. 5 represents measured output fundamental IMD power *versus* input power when the active device is biased in this optimum IMD point. The extrapolated 3rd order intercept point, IP3, is 36dBm while the 1dB compression point is near 12dBm. As the amplifier's input DC power is only 120mW, it presents a linearity figure of merit $IP3/P_{DC}$ of 33, which is believed to be state-of-the-art for an amplifier made with a general purpose MESFET [7].

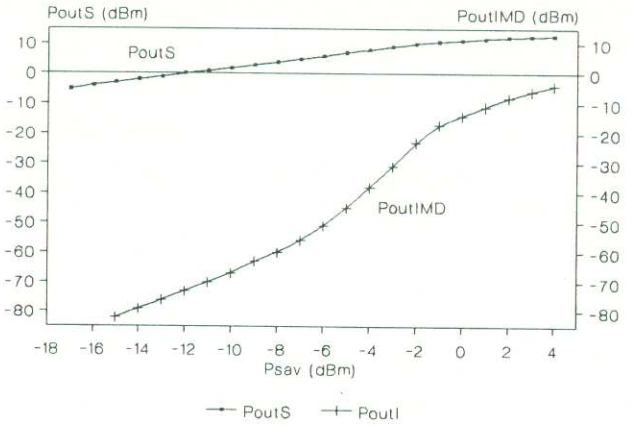

Fig. 5 - Fundamental and IMD output power *versus* input signal power.

IV. Conclusions

The above results indicate that for best IMD performance the design procedure should begin by a careful active device choice (channel doping profile), and than pass by a dedicated bias point selection. This can be done on an *a posteriori* basis, i. e., by an experimental optimum bias search after the design has been implemented, or, for reduced trial and error iterations and better final results, on a *a-priori* basis, which should be supported by dedicated nonlinear device characterisation [4].

Acknowledgement

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