ANALYTICAL MODEL of GaAs BMFET STRUCTURES*

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Abstract A model of the d.c. operation of the GaAs Bipolar Mode Field Effect Transistor (BMFET) is presented. The model in based on a approximate, closed-form solution of the fundamental transport equations, and includes some two-dimensional effects that were not included in previously developed models of silicon BMFET structures. A comparison with the characteristics of a experimental device shows that the incorporation of the 2D effects allows an accurate modeling of the GaAs device.

Introduction

The bipolar mode operation of JFET structures has represented in the last decade a key for the development a new family of bipolar silicon devices, such as the BMFET [1] or BSIT, that have demonstrated a superior performance, with respect to the BJT, in the fields of power amplification and switching.

Recently, BMFET structures have been also implemented in GaAs [2], and demonstrated the potential of this class of bipolar devices to overcome the limitations of homojunction GaAs BJT's by means of a simple technological process. The realized devices have shown an excellent frequency behavior and radiation hardness, as required for telecommunication purposes [3], as well as the ability to operate at temperatures substantially higher than the corresponding Silicon devices [3,4].

Basically the BMFET consists of p^+ (gate), n^+ (source) interdigitated regions, realized on the top of a $n - n^+$ (drain) wafer. In bipolar operation, the Gate is forward biased with respect to the source and induces a electron - hole plasma within the epilayer. The mechanism of current amplification is similar to that of a BJT under base pushout regime, but the device structure gives the designer a additional degree of freedom with respect to a classical BJT, due to the absence of a base layer underneath the source.

A proper bipolar operation of the BMFET requires that the thickness of the epilayer be smaller than the carrier diffusion length. This condition is easily achieved in Silicon where diffusion length values as large as $200\mu m$ are easily found in low-doped epilayers, thus eliminating any constraint in the thickness of this layer also for high-voltage devices. On the contrary, the small lifetime value in GaAs sets a severe limit in the design of GaAs BMFET's, the epilayer thickness being limited to a few μm if a reasonable current gain is to be achieved. In addition, because of the reduced thickness of the n-type layer of GaAs devices, the debiasing effect induced by the transverse flow of the drain current underneath the gate causes the active area of the device to be less than the geometrical device area and to depend on transport parameters and bias conditions. This effect was never included in previous analysis of BMFET devices.

In this paper the first model of GaAs BMFET structures is presented, and compared with experimental results. After deriving an original expression for the active area of the device, as a function of bias condition, the gate and drain current components are evaluated by accounting for the effects of carrier recombination and of electric field distribution on the carrier transport.

This approach allows to derive closed-form solutions for the output I-V characteristics, saturation voltage and current gain, which are shown to agree with the experimental results reported in [2]. The analysis carried out in this paper shows that:

- the active area is generally smaller than the geometrical area of the GaAs device, and this circumstance must be carefully taken into account in the device design.
- unlike the silicon BMFET's, the current gain is dominated by the carrier lifetime of the n-type region over a wide range of injection regimes.

Model

The elementary cell of a BMFET and its current components are sketched in Fig.1. Bipolar operation requires that the Gate-Source diode is forward biased, and that positive voltage is applied to the drain. Minority carrier injected from the gate are confined within a distance X_1 from the top surface, and build-up a conductivity modulation regime, with a significant majority carrier gradient along the vertical axis, that is responsible for

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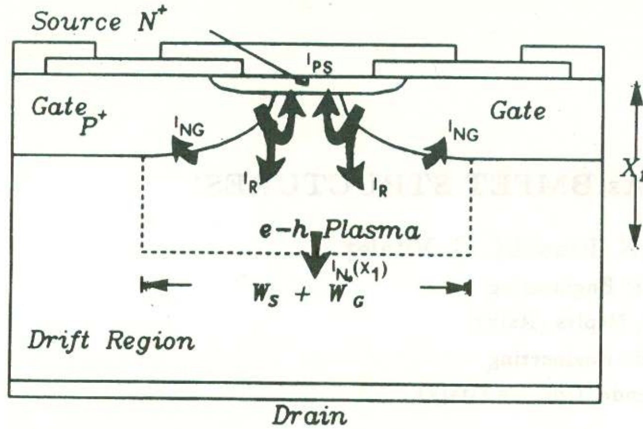

Fig.1 - The elementary cell of BMFET and its current components.

the drain current. Current amplification is due to the control of majority carrier injection from the source, at expenses of a relatively low current injected by the diode.

The analytical model of the BMFET is developed by splitting the epilayer into two subregions, bounded at the abscissa X_1 and characterized by different conduction mechanisms. These are: a) the electron-hole plasma region, where the carrier diffusion mechanism dominates and the charge neutrality condition holds up. b) the drift region, where the minority carriers density is quite negligible and where the drain voltage is localized.

At low drain voltages, the boundary X_1 reaches the epilayer-substrate interface. This is the saturation region of device: the drift region disappears and plasma fills all the epilayer.

If the epilayer thickness is comparable to the cross section of the elementary cell, a significant majority carrier current flows horizontally underneath the gate causing a partial debiasing of the junction. This phenomenon is depicted in Fig.2 with the help of the electron current vectors, calculated by 2D simulation. Gate debiasing causes the active area of the device to be less than its geometrical value, and this has several consequences on the static and dynamic performance of the BMFET. In GaAs devices this situations occurs sistematically as the thickness of the epilayer is limited to a few μm.

Consideration of the lateral current flow allows to determine the active area of the device as a function of bias condition.

Gate crowding effect

The gate crowding phenomenon is due to the flow, parallel to the Gate junction, of the electrons which reach the drain region underneath the Gate region (see Fig.2). This transverse flow causes the applied voltage across the Gate junction to vary, and the Drain current density to be confined near the Gate edge. This effect is similar to the "emitter crowding" phenomenon occurring in BJT' s, and has not been reported yet for BMFET structures. However, while in BJT' s the debiasing mechanism is caused by the transverse flow of a relatively small Base (input) current, in BMFET structures it is associated with the sidewall component of a large Drain (output) current. Therefore, the crowding effect is expected to be more severe in BMFET' s. Moreover, in BMFET structures the current crowding is a sensitive function of the output voltage, due to the Drain voltage-dependence of the plasma region thickness X_1. In fact, as the Drain voltage increases, the plasma region thickness X_1 decreases, causing an increase of the ohmic drop.

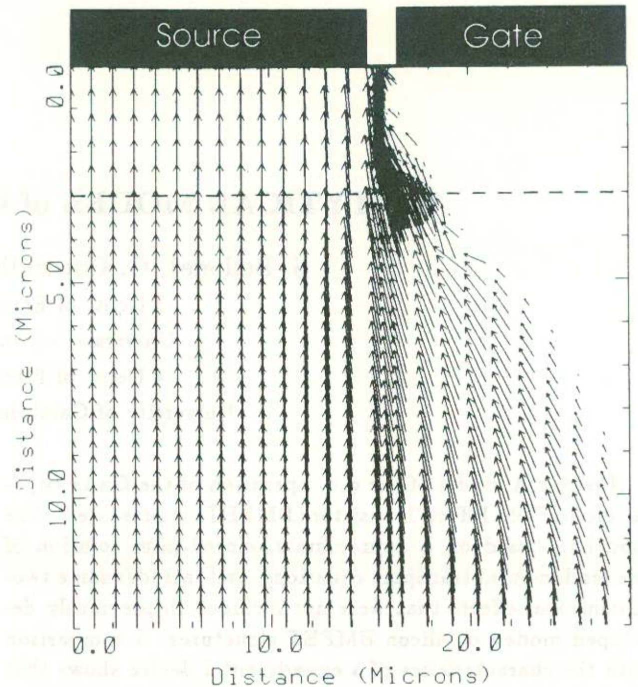

Fig.2 - Two dimensional plot of electron current density, showing the gate debiasing effect.

We have developed a simple analytical model for this debiasing effect which, unlike the low injection level analysis proposed for BJT' s [5], takes into account the conductivity modulation of the epilayer. The main result is that the Drain current density decreases from the Gate edge towards the center following an exponential law, whose characteristic length y_c is given by

$$y_c = X_1 \sqrt{\frac{1}{2}\frac{b+1}{b}} \qquad (1)$$

b being the mobility ratio μ_n/μ_p. As a consequence, the "effective Gate width" W_G^* where carrier injection actually occurs, is less than the metallurgic value W_G, and can be expressed as

$$W_G^* = 2y_c \tanh \frac{W_G}{2y_c} \qquad (2)$$

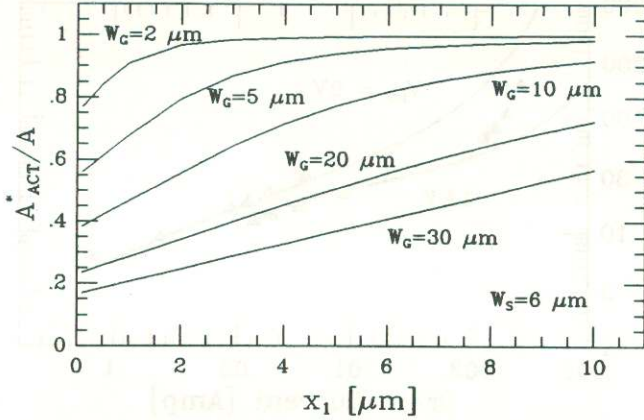

Fig.3 - Ratio of effective to metallurgical area as a function of the thickness of plasma region.

for interdigitated structures. Notice that y_c and W_G^* depend on the plasma region thickness X_1, and hence on the Drain voltage. From (2) it can be seen that as X_1 increases, W_G^* approaches the metallurgic value W_G, while for small values it results $W_G^* \simeq 2y_c$. The active drain area can be easily calculated as $A_{ACT}^* = (W_S + W_G^*)L$, being W_S the distance between the gate diffusions, and the L the device (z-direction) length. Fig. 3 shows the calculated Drain area A_{ACT}^*, normalized to the metallurgic value $A_D = (W_S + W_G)L$, as a function of X_1, for different values of W_G. It is seen that the active region can be considerably reduced by the crowding phenomena. For instance, in the experimental GaAs devices, presented in Section V the epilayer diffusion length is about $3\mu m$. In order to have a reasonable current gain, the epilayer thickness needs to be limited to about is $5\mu m$. From Fig.3, it turns out that the effective area is substantially reduced with respect to its metallurgical value, unless the gate layer is less than $2\mu m$.

Analytical expression of the current components

According to the schematic of Fig. 1, the gate and drain currents under generic operating conditions can be expressed as:

$$I_G = I_{PS} + I_R + I_{NG} + I_p(X_1) \quad (3)$$

$$I_D = I_{ND} - I_p(X_1) \quad (4)$$

where I_R is the recombination current in the electron-hole plasma region, I_{PS}, I_{NG} are the minority carrier current in the source and gate regions, while $I_p(X_1)$ is significant only in the saturation region, namely when X_1 reaches the epilayer-substrate interface.

Except for I_{PS}, calculation of the current components in (3),(4) requires the knowledge of the lateral extension of the electron-hole plasma region, since it establishes the actual epilayer volume where the carrier recombination occurs, the percentage of the injecting area of gate region, and the width of the vertical channel.

Table 1: DEVICE PARAMETERS

	Units	source	gate	epilayer	substrate
Thick.	μm	0.3	0.7	5.0	200.
μ_n	$cm^2/V/s$	-	2293	7122	-
μ_p	$cm^2/V/s$	160	-	376	170
Doping	cm^{-3}	1.3E18	5E18	3.2E13	3E18
τ_n	sec	-	7E-13	7E-9	-
τ_p	sec	1E-9	-	3E-9	1E-9

The two-dimensional behavior of these devices can be described by analizing the operation of two one-dimensional sub-structures, namely the lateral $p^+ - n - n^+$ diode and the vertical $n^+ - n - n^+$ structure, both overlapping on the electron-hole plasma region. By separetely solving the continuity equation into each subregion and by expressing the minority carrier injected in the heavily doped regions in terms of an effective recombination velocity [6], (3) and (4) can be reduced to a fourth-order polynomial which allows to describe the drain current as a function of the abscissa X_1, varying with V_{DS}.

The output voltage is calculated as the sum of the voltage drop across the neutral region of the vertical channel and the voltage of the drift region:

$$V_{DS} = 2V_t ln(\frac{p_g + N_D}{p(X_1) + N_D}) - \int_{X_1}^{X_{EPI}} E(x) \cdot dx \quad (5)$$

where p_g, $p(X_1)$ are the carrier densities at the gate and at the varying boundary, respectively.

Although closed-form solutions of (5) can be derived [1] by using approximate expressions of the electron field-dependent velocity, for this analysis, (5) has been numerically solved by describing v_n as in [7]:

$$v_n = \frac{\mu_n E + v_s \cdot (\frac{E}{E_o})^4}{1 + (\frac{E}{E_o})^4} \quad (6)$$

where $E_o = 4 \cdot 10^3 V/cm$ and $v_s = 1 \cdot 10^7 cm/sec$. With the procedure outlined above for I_D calculation, (3)-(5) allow to completely describe the $I_D - V_{DS}$ curves at a fixed gate current.

Results

The accuracy of this model has been checked by comparisons with the results obtained on experimental BMFET structures. Details on the technology of these devices are reported in [2]

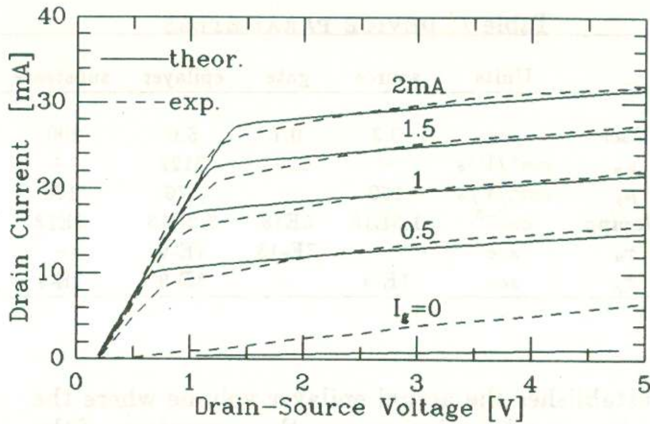

Fig.4 - Output characteristics of a BMFET.

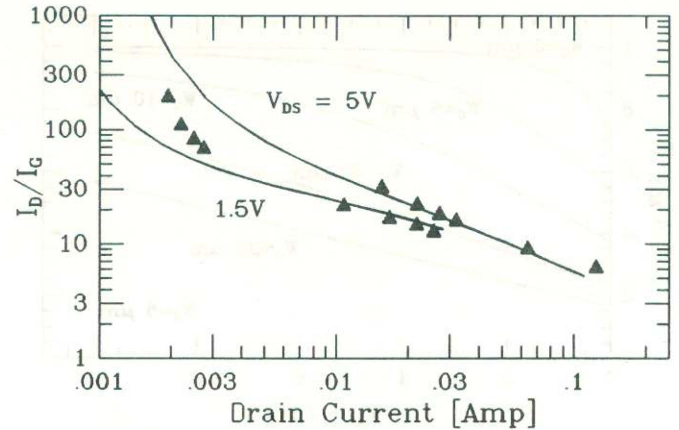

Fig.5 - The d.c. current gain of BMFET.

From the modelling viewpoint, among the various physical parameters of such material the minority carrier lifetime is the most crucial to be set because of its wider spread of literature data and of its stronger sensitivity to the technological steps.

In Fig.4 a set of measured $I_D - V_{DS}$ curves is compared with the theoretical ones obtained by using $n_i = 1.79 \cdot 10^6 cm^{-3}$ [8], the doping dependence of the apparent bandgap narrowing as in [9], carrier lifetimes of the epilayer and of heavily doped regions have been taken from [4] where the analysis of $p-n$ junctions made on the same material was discussed. The parameters used in simulations are reported in Table I. It's interesting to note that the behavior of the device is properly described by the model, both in saturation and in the active region. The effective area, calculated as outlined above, is about 30% of the metallurgical value and this represent a proof of the need to include the gate debiasing effects for a accurate description of the output characteristics of a GaAs BMFET.

Since the present model does not include a detailed description of the transition between bipolar and unipolar (or JFET) operation of the device, some discrepacy with the experiments is detected at very low drain currents, as seen from the output curves as well as from the curves of current gain vs. the drain current of Fig.5.

It is worth noting that the fall-off of current gain, at the highest injections is smaller than that observed in silicon devices due to the relevance of the recombination current within the epilayer, as compared to the other current components in (3).

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