Numerical Study of the Series Resistances in Deep-Submicrometer Recess Gate MESFETs

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Abstract

We report on a new approach to the extraction of the series resistances in recess gate submicrometer MESFETs. The method is based on numerical simulation of the device characteristics using finite element description of the recess shape and realistically treatment of the surface effects. For the first time the contribution of the recess region in the total series resistance is estimated separately. The method is applied to 200 nm gate length MESFETs fabricated recently in the Nanoelectronics research centre at the Glasgow University.

Introduction

The source and drain series resistances are key parameters which strongly influence the performance of modern recessed GaAs MESFETs with deep-submicrometer gate lengths. It is well known that the source resistance strongly affects the device transconductance and noise figures [1]. Both series resistances slow down the device operation.

The precise extraction of the series resistances is extremely important for correctly identifying parameters in the equivalent circuit model and reliably designing MMICs. Although a variety of experimental methods have been proposed to determine these parasitics [2] designers of new devices would like to be able to predict them from the results of a 2D simulation. Few attempts have been made to extract the series resistances from the results generated with device simulation programs. However, they are either restricted to planar geometry [3], or when recess geometry are considered the recess shape is simplified and the surface conditions are poorly modelled [4]. This is unacceptable in devices with gate length comparable to the width of the free recess region.

We report on a new approach for extracting the series resistances in deep-submicrometer recess-gate MESFETs. The work is based on a realistic 2D finite element simulation, using the recently developed Heterojunction 2D Finite element simulator H2F [5]. The shape of the recess and the surface effects leading to a potential pinning and partial surface depletion in the unprotected recess region are properly included in the simulations. We demonstrate that the incorrect treatment of the surface conditions leads to an unacceptable error when estimating the series resistance. For the first time the series resistances associated only with the recess region are separated from the rest part of the device.

Simulation tools and calibration

The extraction of the series resistances is based on the simulation results generated with the program H2F after careful calibration. H2F is a 'classical' steady-state finite element simulator, which solves Poisson's and the current continuity equations in drift-diffusion approximation. Although this approach is unable to describe in fine details the device transport, in many cases it is justified by the need to accurately predict the device parasitics. A great deal of attention has be paid to the proper handling of the surface effects in the simulation. For the Poisson's equation, the simulation domain includes the space above the semiconductor surface providing a proper interaction between the charge on the interface states and the spreading surface potential. A generalised surface trap model includes acceptor and donor like traps with an arbitrary energy position whose occupation depends on the quasi-Fermi level and the surface potential variation. Quadrilateral finite elements have been used for the discretiztion which allows for a precise approximation of the recess shape [6].

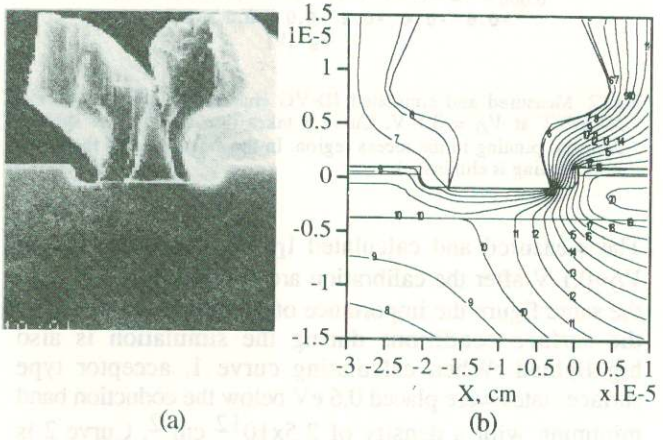

Fig. 1. Finite element simulation of a 200 nm gate length MESFET. (a) SEM picture of the device cross section. (b) Potential distribution at $V_G = 0.4$ V and $V_D = 2.5$ V.

A 200 nm gate length MESFET, recently fabricated in the Nanoelectronics Research Centre at Glasgow University and described elsewhere [7] has been used to study the effect of the recess associated series resistance. The shape

of the recess region obtained by dry etching is illustrated in Fig. 1 (a) on a SEM micrograph of the device cross section. The potential distribution within the device at V_G = 0.4 V and VD = 2.5 V is given in Fig. 1 (b). The shape of the H2F simulation domain closely approximates the real shape of the device.

The rigorous extraction of the series resistances requires fabrication and measurement of devices with different channel lengths [1]. If the contribution of the recess regions needs to be estimated, set of devices with different recess widths has to be fabricated and measured additionally. The overall procedure is time consuming, expensive and unreliable.

In the proposed approach we use fabricated devices with only one channel length. The device characteristics are measured and the device structure precisely investigated. Than the program H2F was calibrated against the device structure and the measured characteristics. Since the extraction of the series resistances proceeds at low drain voltages, only the low field mobility has to be calibrated. The calibration also includes the position and the density of the pining surface states. When the calibration were satisfactory completed the simulation program has been used to generate 'quasi experimental' results for different channel lengths and recess widths from which the overall series resistances and the contribution of the recess region were extracted.

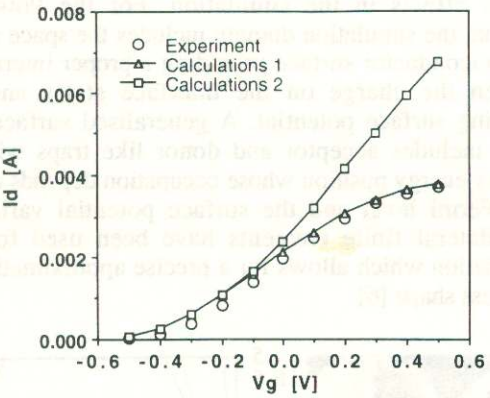

Fig. 2. Measured and simulated ID-VG characteristics of a 200 nm MESFET at V_D = 0.1 V. Curve 1 takes into account the surface potential pinning in the recess region. In the calculation of the curve 2 the pinning is eliminated.

The measured and calculated I_D-V_G characteristics at V_D=0.1 V after the calibration are compared in Fig. 2. In the same figure the importance of the proper treatment of the surface conditions during the simulation is also highlighted. When calculating curve 1, acceptor type surface states were placed 0.6 eV below the coduction band minimum with a density of $2.5x10^{12}$ cm^{-2}. Curve 2 is calculated ignoring the surface charge. The potential distributions with and without surface pinning states, at V_G=-0.1 V is mapped in Fig. 2 (a) and (b) respectively. Fig. 2 (a) clearly indicates how the surface potential pinning depletes the recess region, reducing the current path width to less than a half of width estimated by the unpinned model.

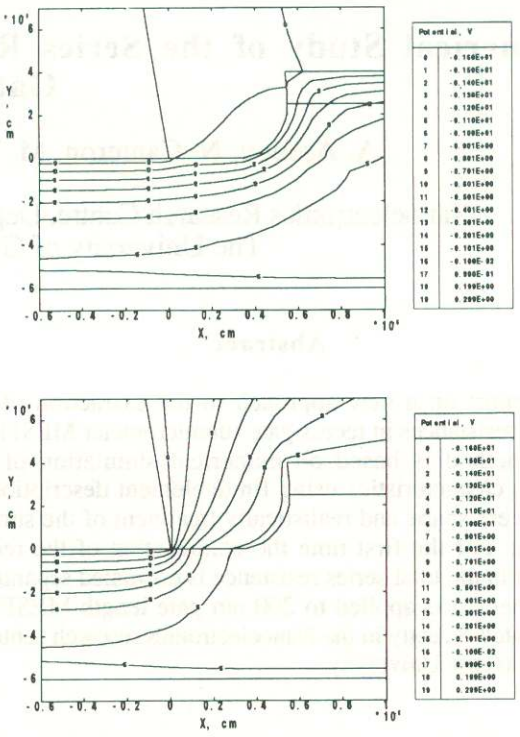

Fig. 3. Effect of the surface potential pinning on the potential distribution in the recess region. (a) Acceptor surface states 0.6 eV bellow E_C with concentration $2.5x10^{12}$ cm^{-2}. (b) No surface charge.

As an addition proof that the estimated position and density of the pinning states is correct for our device in Fig. 4 we compare the calculated and measured I_D-V_G characteristics at high drain voltage V_D=2.5 V. The calculations have been done for different positions of the acceptor surface states and constant surface state density $2.5x10^{12}$ cm^{-2}. The agreement is good again for the states position 0.6 eV bellow the conducting band minimum.

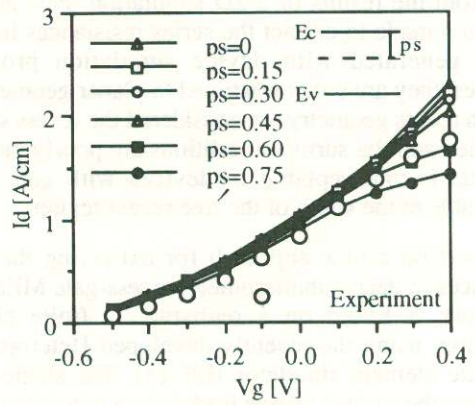

Fig. 4. Simulated and measured I_D-V_G curves at V_D=2.5 V. In the simulations different positions Ps for the surface pinning states were assumed with state density $2.5x10^{12}$ cm^{-2}.

Series resistances model

The series resistances model we are using in this work is illustrated in Fig. 5.

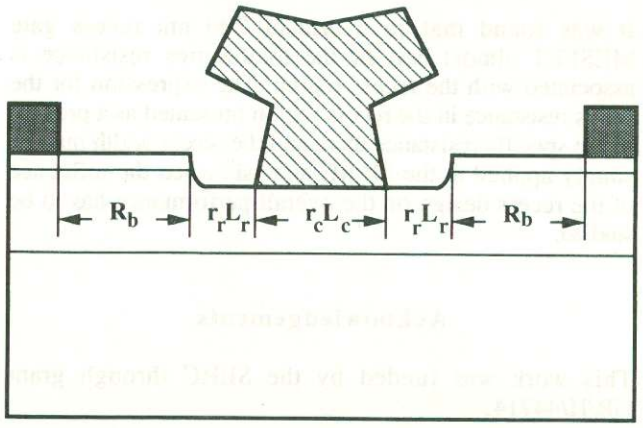

Fig. 5. Series resistances in a recess gate MESFET

The total device resistance $F=V_D/I_D$ at low drain voltage can be divided into three components: the channel resistance $R_C=r_CL_C$; resistances of the recess regions $R_r=r_rL_r$; and resistances of the capped regions R_b, where r_C and r_r are resistances per unit length. Hence

$$F=2R_b+2r_r(L_r+dL_C)+r_C(L_C-dL_C), \qquad (1)$$

where dL_C accounts for the effective channel length modulation due to the applied gate voltage. The expression (1) is valid for a symmetrical MESFET but its extension to a asymmetrical structures is straightforward.

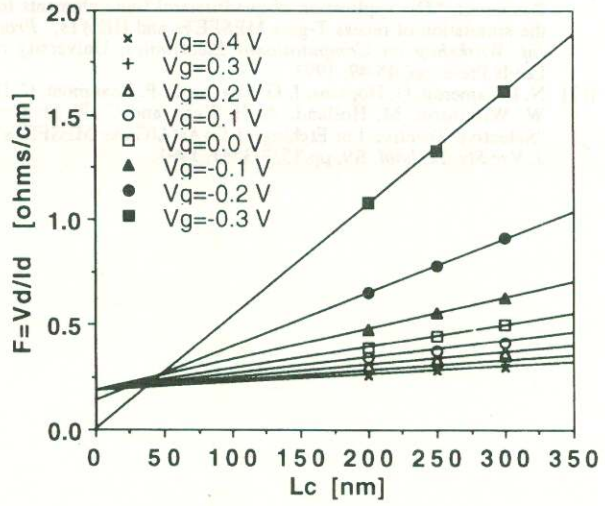

Fig. 6. Dependence of the total device resistance $F=V_D/I_D$ on the channel length.

The linear interpolation of the dependence of F on the channel length L_C (Fig. 6) determines both r_C (the slope) and the series resistances $R_S+R_d=2R_b+2r_r(L_r+dL_C)-r_CdL_C$ (the intercept). The channel length modulation dL corrupts these values resulting in $Rs+Rd$ becoming negative near the threshold voltage. But above the threshold, when r_CdL_C is small, this method works fairly well. The effect of the surface potential pinning on the series resistances is clearly indicated in Fig. 7 where the extracted series resistances, with and without inclusion of the surface effects in the simulation, are plotted as a function of the gate voltage V_G.

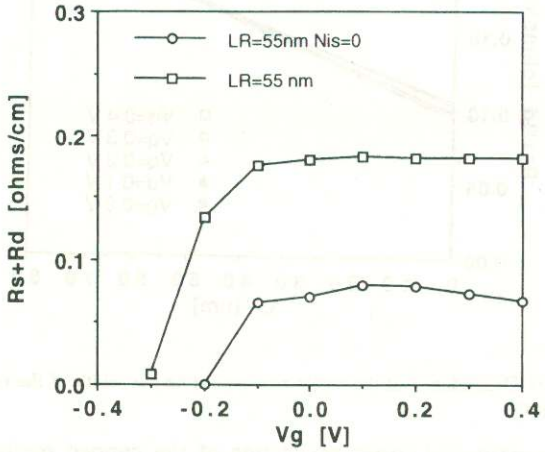

Fig. 7. Series resistances extracted with and without (N_{is}=0) surface effects included in the simulation.

Neglecting the pinning (N_{is}=0) leads to an underestimation of the series resistances to less than the half their true value.

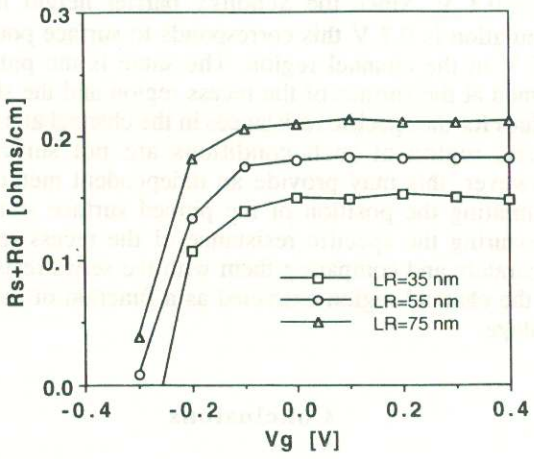

Fig. 8. Dependence of the series resistances on the width of the recess region.

The calculated series resistances for three transistors with different recess length are presented in Fig. 8. As can be expected, above the threshold when $r_c dLc \cong 0$ the dependence of the series resistances on the recess length is linear because $R_S+R_d=2R_b+2r_rL_r$. The plot of the series resistances as a function of the recess width gives the specific resistance of the recess regions r_r (the slope) and the resistances of the capped regions $2R_b$ (the intersect)

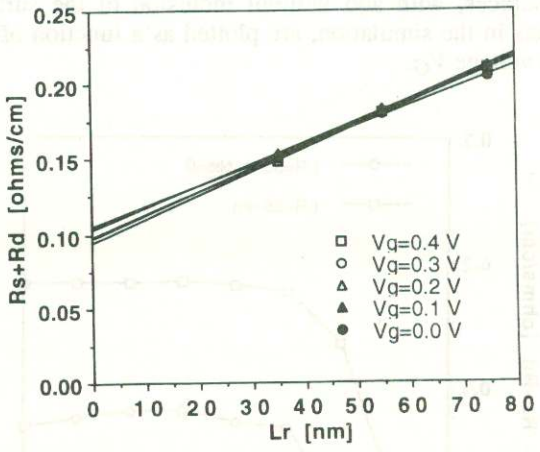

Fig. 9. Dependence of the series resistances on the width of the recess region.

The estimated series resistance of the capped region is approximately R_b=0.05 ohms/cm and the specific resistance of the recess region is r_r=7.5x10^3 ohms/cm^2 which gives for a 55 nm recess length R_r=0.04 ohms/cm. This makes it clear that the contribution of the recess region is almost half of the total series resistance in our device.

It is interesting to note that the channel specific resistance, r_c, is approximately 7.5x10^3 ohms/cm^2 at V_G=-0.1 V. Since the Schottky barrier height in our simulation is 0.7 V this corresponds to surface potential 0.6 V in the channel region. The same is the potential pinned at the surface of the recess region and the similar values for the specific resistances in the channel and in the recess region at such conditions are not surprising. However, this may provide an independent method for estimating the position of the pinned surface states by measuring the specific resistance of the recess regions separately and comparing them with the series resistance of the channel region extracted as a function of the gate voltage.

Conclusions

In this paper we have presented a new approach to the extraction of the series resistances in a short recess-gate MESFETs. The method is based on a single gate length device fabrication and characterisation. Than rigorously calibrated simulation result were used to generate 'quasi-experimental' data for different gate length and different recess widths. Those data are than used to extract the total series resistances in the device and to separate the contribution of the recess region based on a simple series resistances model.

It was found that in a typical 200 nm recess gate MESFET almost half of the total series resistance is associated with the recess region. The expression for the series resistance in the recess region presented as a product of the specific resistance there and the recess width may be simply applied in the MMIC analysis when the influence of the recess design on the overall performance has to be studied.

Acknowledgements

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