A new coherent extraction method of FETS and HEMTS models for MMIC applications

J. Portilla, M. Campovecchio, R. Quéré, J. Obrégon
IRCOM - URA CNRS n° 356 - Faculté des Sciences
123, Avenue Albert-Thomas - 87060 LIMOGES Cédex (France)

Abstract

In this paper, we present a study of broad band FET model parameter extraction problems. A novel modeling method, providing reliable FET small-signal model parameters, is presented and compared with well-known extraction methods. The named extrinsic elements are optimized to yield a broad band coherent model and the optimization approach is based on "simulated annealing" method which overcomes the multi-minimum optimization problems.

Bias dependence of some of the named extrinsic elements are reported and discussed. In particular, physical explanations of the negative resistance values, based on quasi 2D physical simulations , are discussed and the novel extraction method is evaluated by MMIC FETS and HEMTS broad band measurements.

Introduction

Today, the development of nonlinear microwave circuits and in particular of the MMIC technology applications relies on an intensive use of CAD software packages which requires, to be effective, suitable and accurate electrical models of the active component behavior such as MESFETs and HEMTs. A coherent approach for nonlinear modeling of MESFETs necessitates specific measurement techniques, well suited to the real operating conditions (pulsed I-V measurements [1], S-parameters measurements under pulsed bias conditions [2]) and also accurate extraction techniques of model parameters. In particular, the extraction method should ensure the reliability of all the extracted model elements at the same operating and measurement conditions over the frequency band.

Coherent extraction of broad band electrical models

The determination of the FET small-signal equivalent circuit elements from measured S-parameters is commonly realized, at a given bias point, by extraction techniques based either on optimization or the so-called direct extraction method [3]. In this last case, the extrinsic access elements are measured and the intrinsic model elements are then analytically determined from the deembedded Y-parameters.

Nevertheless, it should be pointed out that the different kinds of measurements and methods [3 - 5], involved in the determination of the access elements, provide a set of multiple solutions which directly affects the intrinsic element values. This extraction problem is due to the bias dependence of the named extrinsic elements which are considered as invariant parameters in the usual extraction techniques but are practically affected by the transistor operating conditions. Moreover, once the access elements known, the intrinsic parameters are generally found frequency-dependent, using classical extraction methods (see figure 2b).

Hence, the reliability of the small-signal model, whose parameters must be taken frequency-independent, is affected.

Our method, which is a combination of both analytical and numerical extraction methods, consists in optimizing the extrinsic elements so that a frequency-independent set of intrinsic elements can be analytically derived. This approach leads to a reliable coherent model with respect to the operating conditions over a frequency broad band.

The flow chart of the coherent extraction method proposed is presented in the figure 1. The

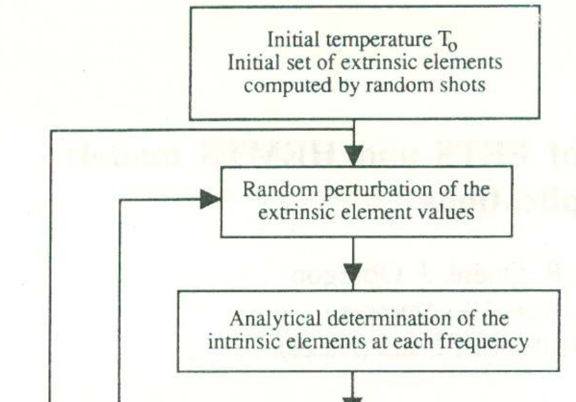

Figure 1 - Flow chart of the coherent extraction method

optimization method is based on a modified "simulated annealing" approach [6, 7]. This technique makes an analogy between the error function to minimize, and the energy of a particle system which evolve towards the thermodynamic equilibrium. During the optimization flow, the solutions associated with an higher error function (energy) may be accepted according to a probability law which depends on the energy state (error) of the system. Hence, the simulated annealing optimization method provides, with a high probability, the global minimum of the error function and overcomes the well-known local minimum problem.

An example of comparison between the usual direct extraction technique and our method is shown figure 2 for a 0.5 x 300 µm MMIC FET fabricated at Thomson foundry. The final set of intrinsic elements derived from our technique is almost frequency-independent and shows a good improvement, compared to the classical direct extraction results as it can be seen on the intrinsic Y-parameters.

Bias dependence of series resistances and physical explanation of their positive or negative values

Under saturated operating conditions, the novel extraction method applied to FETs and HEMTs devices leads to negative values of series resistances. In fact, each access resistance consists of two series elements which are respectively Rd_{ext} and Rd_{int} for the drain resistance Rd (see figure 7). Rd_{ext} is a constant positive resistance due to the ohmic contact while Rd_{int} is an intrinsic bias-dependent resistance which may be positive or negative, depending on the operating conditions. The negative values of drain resistance are quite often encountered in the actual GaAs devices with short gate lengths which lead to a non-stationary dynamic phenomenon [8] and consequently affect the small-signal behaviour of the FETs.

Indeed, the physical origins of this phenomenon are the particular properties of the carrier transport in the GaAs material and the high field electron region presented at the drain side of the active channel under saturated operation.

These explanations are supported by quasi bi-dimensional physical analysis performed with the QUASAR simulator [9] for short gate lengths GaAs FETs. The physical simulations, presented in this paper, have been performed by using an energy transport model which allows to take into account the non-stationary dynamic phenomena. The examples presented figure 3 and 4, related to 0.5 µm and 1 µm gate length FETs, demonstrate for a saturated bias point the existence of a negative resistance region at the drain end of the channel.

It should be noted that the negative values of the intrinsic element Rd_{int} cannot be taken into account in the classical extraction methods since the resistances are measured while the transistor is biased in the ohmic region. As shown in the figures 5 and 6, the physical simulations of the 0.5 µm and 1 µm gate length FETs never present negative region along the channel for an ohmic bias point.

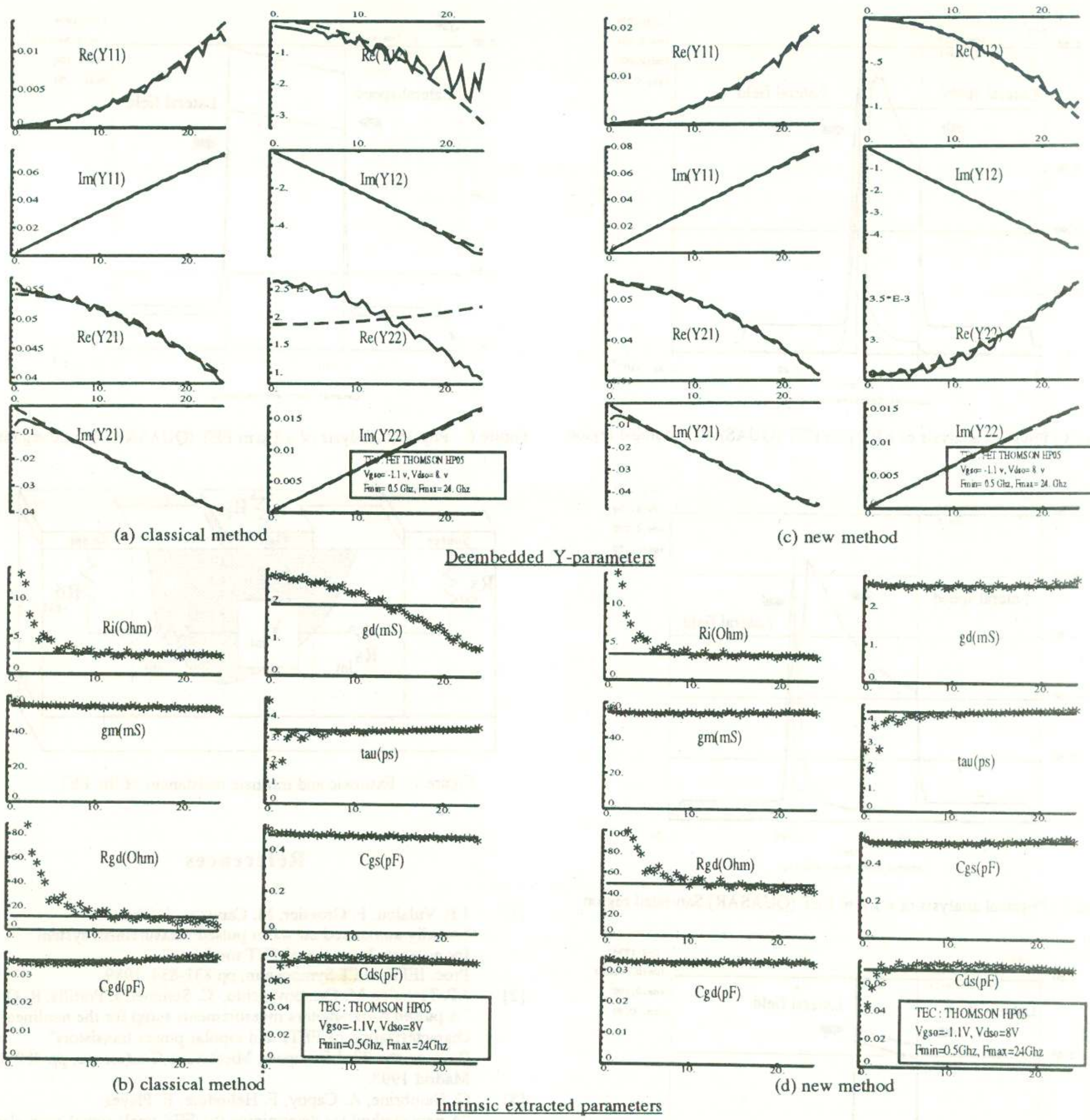

Figure 2 - Comparison between classical extraction (a,b) and new method (c,d) versus frequency

All these results obtained by the new coherent extraction method and confirmed by physical simulations lead us to consider a more realistic model including the intrinsic bias dependent resistances in series with the positive access resistances as it can be seen at the figure 7.

Conclusion

A new coherent extraction method of broadband FET model, which is a combination of both analytical and numerical extraction methods, have been presented and compared to the well-known extraction techniques. The optimization approach is based on a modified "simulated annealing" method and includes the extrinsic access elements in the optimization flow to yield a broadband FET model whose parameters must be frequency-independent and coherent with the operating conditions.

The extraction results, presented in this paper for Thomson MMIC FETs, show good improvements compared to the classical methods. The bias dependence of the series resistance have been investigated and the physical explanation of their positive or negative values encountered

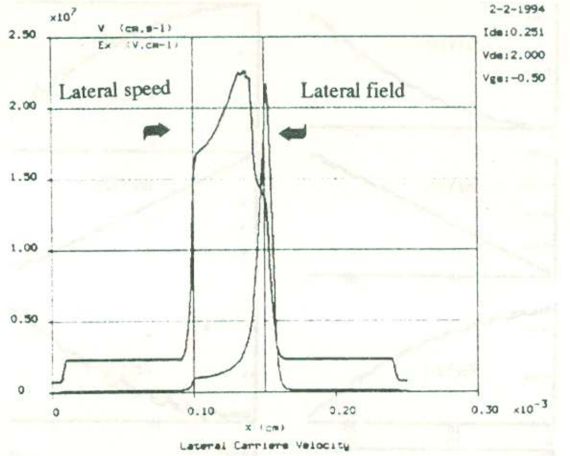

Figure 3 : Physical analysis of a 0.5 μm FET (QUASAR) Saturated region

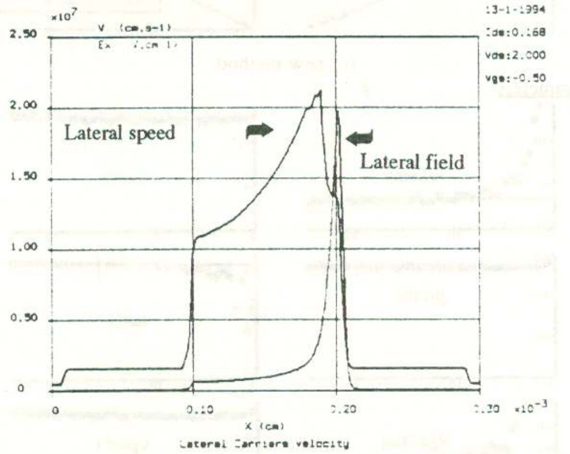

Figure 4 : Physical analysis of a 1 μm FET (QUASAR) Saturated region

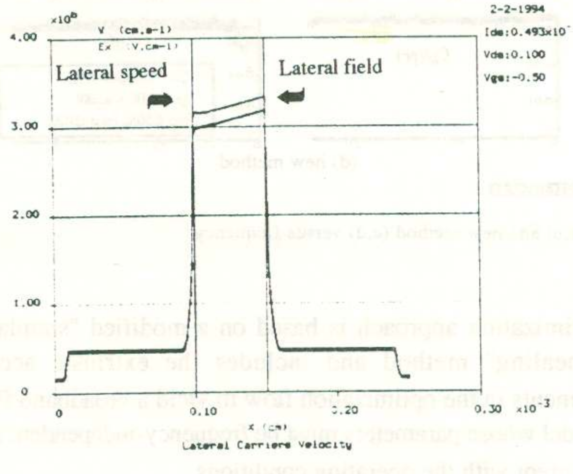

Figure 5 - Physical analysis of a 0.5 μm FET (QUASAR) Ohmic region

in the actual GaAs devices have been supported by quasi bi-dimensional physical analysis under ohmic and saturated device operation.

In conclusion, a more realistic FET model must include the intrinsic bias dependent resistances in series with the positive access resistances.

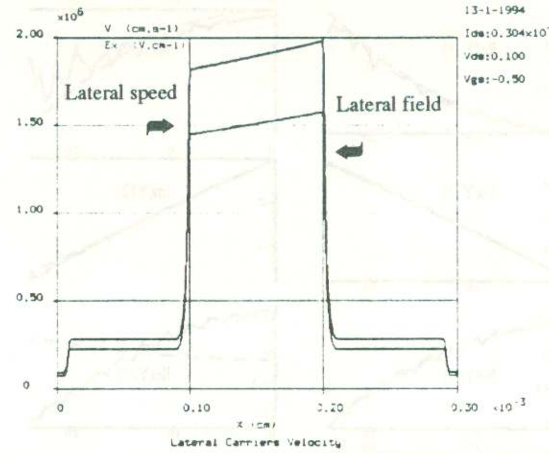

Figure 6 - Physical analysis of a 1 μm FET (QUASAR) Ohmic region

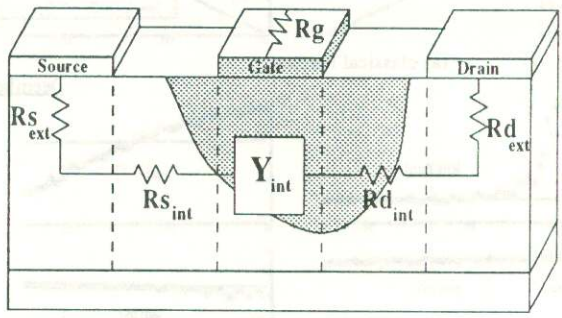

Figure 7 - Extrinsic and intrinsic resistances of the FET

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