A Large-Signal Model for GaAs MESFET's and HEMT's Valid at Multiple DC Bias-Points

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Abstract

In this paper we present a general-purpose GaAs FET non-linear circuit model, for universal use (DC, small-signal and large-signal) which is valid at multiple DC operating points. Novel features of the model include: (i) a direct and reliable multi-bias point parameter extraction methodology (no optimisation required), based solely on CW S-parameter measurements, with an improved approach to the extraction of the parasitic resistances; (ii) more accurate models for the main non-linearities, with special attention paid to the gate capacitances, the intrinsic resistance and high-frequency dispersion in the drain circuit. The validity of the model is demonstrated through extensive power-sweep tests, carried out at different DC bias-points and different frequencies.

Introduction

Design tools for large-signal applications of GaAs MESFETs and HEMTs, ideally require a single CAD model which can provide accurate descriptions of non-linear DC and AC behaviour over a wide range of bias points. Furthermore, a direct and reliable methodology for the extraction of extrinsic and intrinsic elements of the equivalent circuit, as well as accurate modelling formulas for the main non-linearities, are of critical importance. In this work we will outline such a general-purpose FET model together with its associated parameter-extraction methodology, introducing some new ideas, particularly in relation to parasitic element identification and non-linear modelling. Validation of the model, for an "on-wafer" *0.5μm* GaAs MESFET (Plessey-F20), using power sweeps in a *50Ω* amplifier environment is demonstrated at several DC bias-points and at different frequencies.

Parameter extraction

The parameter extraction procedure, which follows, at least in principle, similar methods presented in literature [1][2][3], is based solely on small-signal CW S-parameter measurements, performed at various bias points, and it has three main parts. Firstly, S-parameters measured at *Vds=0V*, *Vgs=0V* ("unbiased FET"), and at *Vds=0V*, *Vgs<Vp* ("pinched-off FET"), are used to determine all the parasitic elements. Secondly, having obtained the parasitics, their effect is de-embedded from the original measurement data, by means of a simple matrix transformation sequence (S-Y-Z-Y), leading finally to the Y-parameter matrix of the intrinsic device. Finally, these parameters are used to determine the intrinsic elements of the equivalent circuit, following a similar methodology to that introduced by Dambrine et al. [1] and completed later by Berroth and Bosch [2].

A. Extraction of parasitic elements

The possibility of extracting all parasitic elements from the "unbiased" and "pinched-off FET" S-parameter measurements brings substantial benefits, particularly in relation to parasitic resistance extraction [3], in that the so-called "hot-FET" measurements are avoided and consequently the number of measurement points needed is reduced. Also, it allows the observation of the frequency dependence of these resistances and overall, simplifies whole procedure. Recently, such a methodology has been proposed [3], showing very good results. Yet, some difficulties still arise when extracting the parasitic resistances, and in this section we will try to introduce an improved method that is found able to overcome some of these difficulties. The first step, before proceeding to the extraction of parasitic resistances, is to extract the pad capacitances and the fringing capacitance using the Y-parameters of the "pinched-off FET" [1]. The actual values should be computed by averaging over the lower side of the frequency band, where the influence of the inductors is insignificant. This method is straightforward and gives very accurate results as shown in *Fig.1.*

If one considers that *Rg*, *Rs* and *Rd* are not changing between the two bias points, Z-parameters for the "unbiased" (index "*u*") and "pinched-off FET" (index "*p*") can be written as [1]:

$$Z_{11u}=Rg+\alpha Rch+Rs+j(\omega(Lg+Ls)-1/\omega Cg) \quad (1)$$

$$Z_{12u}=Rs+0.5Rch+j\omega Ls \quad (2)$$

$$Z_{22u}=Rs+Rch+Rd+j\omega(Ls+Ld) \quad (3)$$

$$Real\{Z_{11p}\}=Rg+Rs \quad (4)$$

$$Real\{Z_{12p}\}=Rs \quad (5)$$

There are a few difficulties in relation to the extraction of parasitic resistances as presented in [3]. Firstly, the implicit assumption that *Rs* and *Rd* are not changing between the "unbiased" and "pinched-off" states is not as evident as it is for *Rg*. This is because the gate resistance is associated with the gate metalisation and contact, and is expected to

show only a small bias-dependence, while *Rs* and *Rd* are dependent on the shape of the depleted region within the active channel, which in our case varies between two extreme states. Secondly, a value for Rs determined from (5) will be slightly dependent on how strongly the channel is pinched-off. As a result, these values can be inaccurate or sometimes even hard to extract. Thirdly, in [3] the coefficient α is set to *0.5*, making possible the extraction of *Rg* from (1) and (2). This differs from the results described in [1], where, based on some physical considerations, a value around *0.3* has been proposed. In fact, our simulations for the devices tested here, showed that a value around *0.3* leads to more realistic values.

In order to overcome some of these difficulties, our approach in extracting the parasitic resistances, begins with the extraction of *Rg* from the "pinched-off" data, by simply subtracting (5) from (4). In this way, the actual value of *Rs* in (4) and (5) becomes irrelevant. Now with *Rg* determined and with α set to 0.3, the extraction of *Rs* and *Rd* from (1), (2) and (3) is straight-forward. One last detail regards the computation of the actual values of these resistances. Based on our results, we recommend that when averaging, to avoid the extreme ends of the frequency band, where the reactive elements in the circuit (*Cg* at the lower end and parasitic inductances at the higher end) may introduce significant errors.

For the determination of the parasitic inductances, the methodology described in [1][3] works very well. A simple graphical method can be alternatively used to determine *Lg* and *Cg*. The above outlined procedure has been applied to three different "on-wafer" *0.5μm* GaAs MESFETs, and the results are also shown in *Fig.1.*

B. Extraction of intrinsic elements

After de-embedding the effect of parasitic elements from the original S-data by means of a simple matrix transformations sequence, an automated routine enables the computation of all intrinsic elements in the equivalent circuit, following a method similar with that presented in [1][2]. Again, special care is taken when averaging these values over the frequency band of interest. For the three devices under test here, the results were very similar and consistent and the curves remarkably smooth. An example for one of the devices considered is shown in *Fig.2a, b, c, d, e, f* and *g* (*Vgs* is varied between *-1.8V* and *+0.4V* in steps of *0.2V*; the pinch-off voltage was around *-1.8V*). Small-signal AC tests using linear models based on these results show excellent fit with the measurements, but they are not presented here for lack of space. The input file contained in this case the S-parameter data for 276 different bias-points, each measured at 52 frequency points (between *0.5 GHz* and *26 GHz*) . The computation time of all parameters, including the creation of all output files for the graphs shown was around 12 seconds, on a 486 PC. Presently this parameter extraction procedure is almost completely automated and recently has been tested on power MESFETs and P-HEMTs with equally good results.

Large-signal modelling

There is no doubt that having all the circuit elements extracted accurately, greatly simplifies the task of large-signal modelling. Looking at these parameters, a first remark is that elements like *Cds* and τ can be kept as constants without causing significant errors. On the other hand, keeping *Ri* as a constant appears no longer acceptable. Therefore, here we propose a novel non-linear model for *Ri* which proved to reproduce very well the kind of behaviour seen in *Fig.3f*:

$$R_i = R_{i0} + K_g \cdot \left[1 - \tanh a_1 \cdot (V_{GS} - V_{T0})\right] + K_d \cdot \left[1 - \tanh a_2 \cdot (V_{DS} - V_{DS0})\right] \quad (6)$$

where V_{T0} is the pinch-off voltage, V_{DS0} is the drain voltage where the velocity saturation occurs and R_{i0}, K_g, K_d, a_1 and a_2 are model parameters.

The gate-to-source and gate-to-drain capacitances are also strong non-linear elements. Recently [5], a new model and a new modelling technique have been proposed for these capacitances and it has been applied here successfully. When *Vds=0V*, the two capacitances are described by:

$$C_{gs,d} = \frac{C_1}{\left(1 - \frac{V_{gs,d}}{V_{bi}}\right)^m} + C_2 \cdot \left[1 + \tanh a \cdot (V_{gs,d} - V_{T0})\right] \quad (7)$$

where V_{bi} is the built-in potential of the Schottky contact at the gate and C_1, C_2, m and a are model parameters. In *Fig.3.* the total gate capacitance extracted from experimental data at *Vds=0* is compared with this model and as it can be seen the fit is excellent.

Finally, the most important non-linearity for GaAs FET structures, resides in the output drain circuit. The DC model that we propose here for the drain current is:

$$I_{ds} = \beta \cdot V_{eff}^{\lambda} \cdot \tanh \alpha \cdot V_{ds}$$
$$V_{eff} = 0.5 \cdot \left[V_{gs} - V_T + \left[(V_{gs} - V_T)^2 + \delta^2\right]\right] \quad (8)$$
$$V_T = V_{T0} - \gamma \cdot V_{ds}$$

where α, β, γ, δ, λ and μ are model parameters. The introduction of *Veff* assures a smooth transition of the drain current to zero when *Vgs* approaches the pinch-off voltage. Also it has the ability to reproduce the negative slope in the saturation region, caused by the increased temperature in the active channel, when *Vgs* increases to positive values. The comparison with the measured DC characteristic for our DUT is shown in *Fig.4.* This new formula has been applied as well recently, with very good results, to other FET structures, such as medium and high-power MESFETs and P-HEMTs.

It is well-known that second-order effects such as electron traps at the channel-substrate interface are responsible for

the dispersion of output conductance and transconductance at higher frequencies. Having available accurate DC and AC data for these parameters, makes it easier and more effective to account for and to model the differences between the two, using a similar approach as in [4]. However, for the present DUTs there was very little dispersion observed between DC and AC data, particularly for the transconductance, and a simple series R-C circuit (R=300Ω) between drain and source proved to be sufficient.

The above model have been successfully implemented in the MDS Simulator (Hewlett-Packard), using a multi-port SDD element (Symbolically-Defined Device) for the intrinsic section making it very flexible and efficient for performing various DC, small-signal and large-signal tests.

Validation of the model

Apart from the DC (see *Fig.4.*) and small-signal AC tests, extensive large-signal tests have been carried out, in order to prove the validity of the overall modelling methodology. These tests consisted in power-sweeps in a *50Ω* amplifier environment performed at several DC bias-points and for two different frequencies. In *Fig.5a* and *b* the results (up to the 4th harmonic) of two such measurements are compared with the simulations performed using the new model implemented in the MDS Simulator. The frequency of the input signal was *f = 4 GHz*. *Fig.5a* shows the results for *Vgs=-1.0V* and *Vds=4.0V* (*Ids=30.2 mA*), while in *Fig.5b* the bias point was *Vgs=-1.8V* and *Vds=0.5V* (simulations are represented by thicker continuous lines). Results for other bias-points and for *f=8 GHz*, gave similar good results but are not included here for lack of space.

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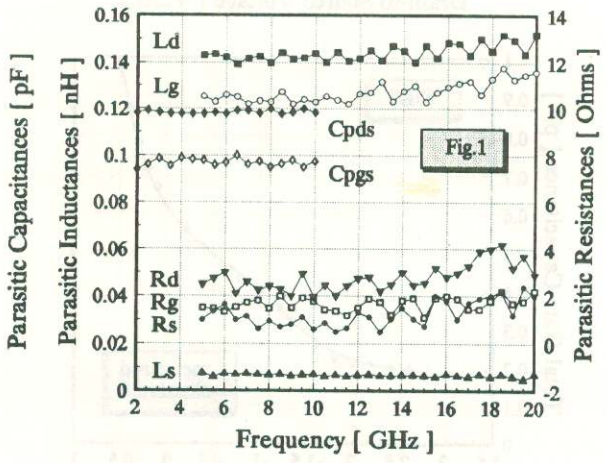
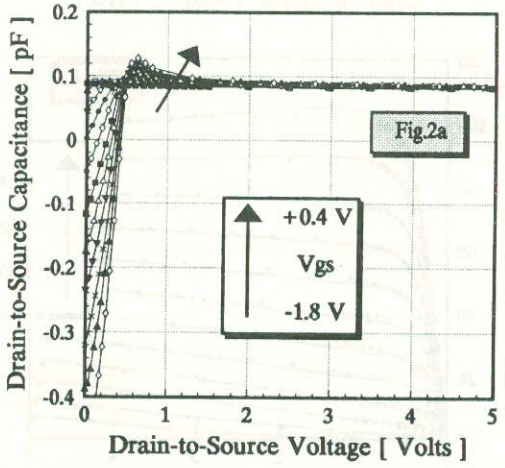
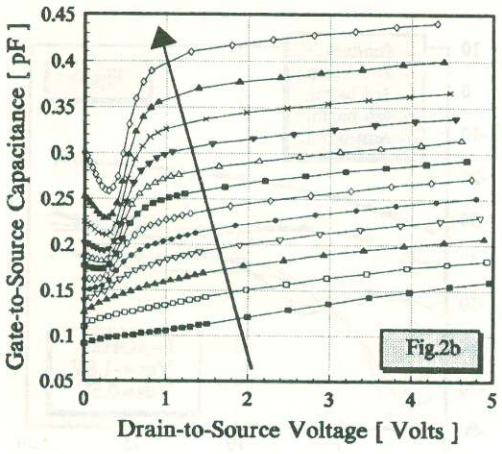
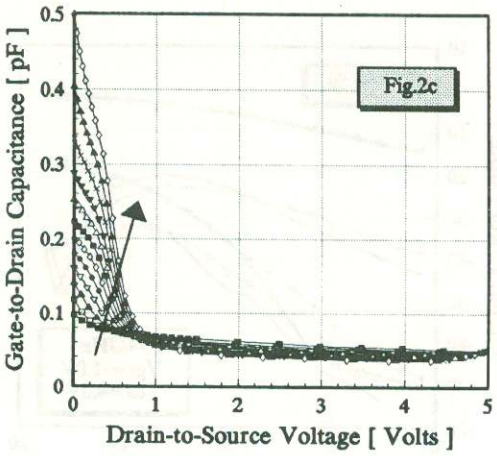








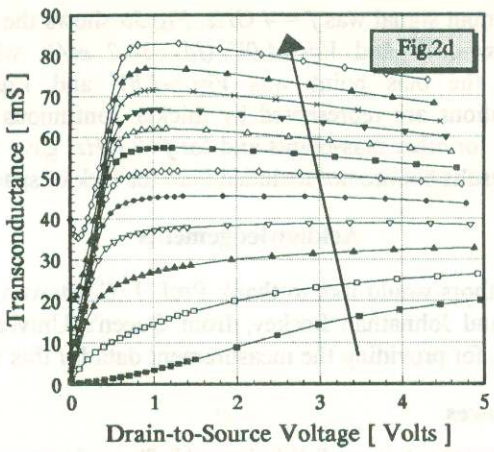


Fig.2d
Transconductance [mS]
Drain-to-Source Voltage [Volts]

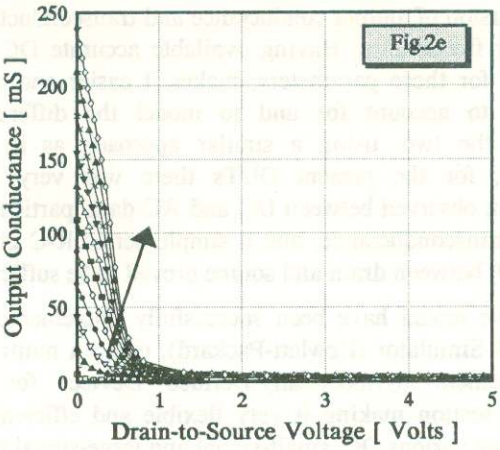


Fig.2e
Output Conductance [mS]
Drain-to-Source Voltage [Volts]

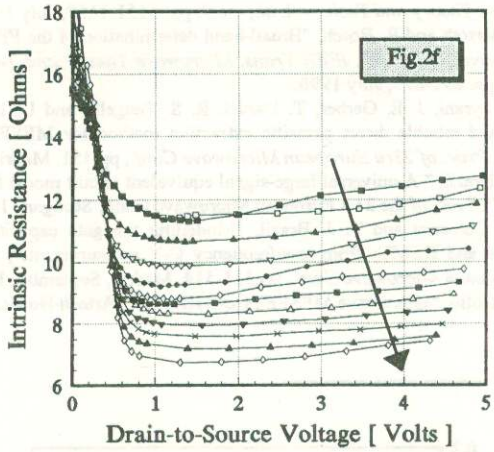


Fig.2f
Intrinsic Resistance [Ohms]
Drain-to-Source Voltage [Volts]

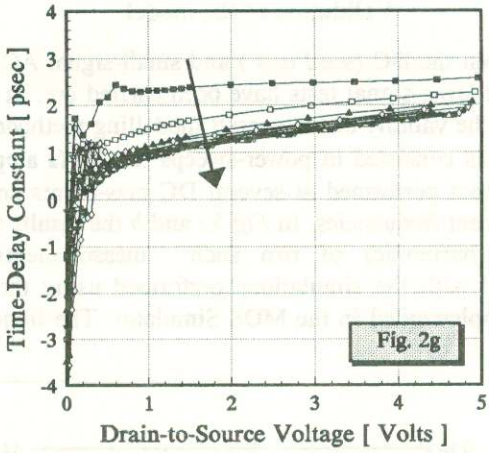


Fig. 2g
Time-Delay Constant [psec]
Drain-to-Source Voltage [Volts]

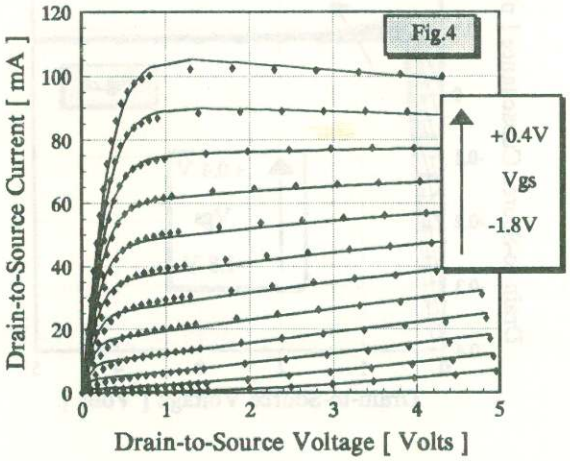


Fig.4
+0.4V
Vgs
-1.8V
Drain-to-Source Current [mA]
Drain-to-Source Voltage [Volts]

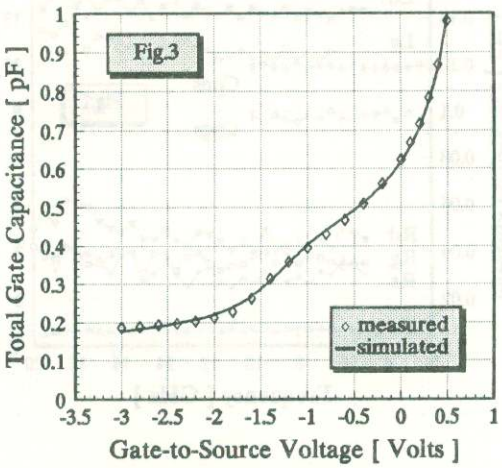


Fig.3
measured
simulated
Total Gate Capacitance [pF]
Gate-to-Source Voltage [Volts]

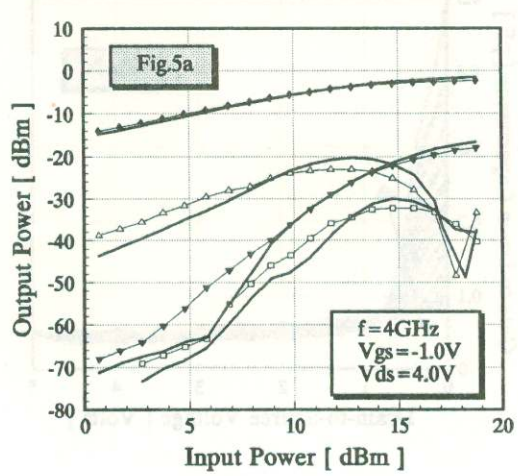
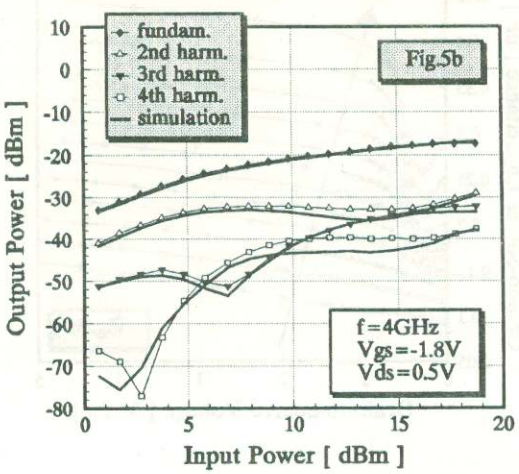


Fig.5a
f=4GHz
Vgs=-1.0V
Vds=4.0V
Output Power [dBm]
Input Power [dBm]


fundam.
2nd harm.
3rd harm.
4th harm.
simulation
Fig.5b
f=4GHz
Vgs=-1.8V
Vds=0.5V
Output Power [dBm]
Input Power [dBm]