Thermal modelling of microwave devices for the electrothermal analysis of nonlinear microwave circuits

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Abstract

The paper discusses a general approach to the electrothermal simulation of nonlinear FET circuits. The thermal resistance of each active device is first computed by a numerical method based on physical and layout information, and is then used to derive a temperature-dependent nonlinear model starting from measured DC and small-signal information. The combined thermal and electrical simulation is then carried out by an extended harmonic-balance technique.

Introduction

The inclusion of thermal aspects in CAD procedures for microwave devices and circuits represents one of the most significant development trends of modern computer-aided simulation techniques. Although a considerable effort is being devoted to this topic both in the industrial and in the academic environment (e.g., [1]), general-purpose electrothermal CAD procedures suitable for the needs of R&D microwave engineering practices have not yet been reported. This paper is devoted to the illustration of a self-contained approach to the electrothermal analysis of nonlinear microwave circuits containing active devices described by temperature-dependent state equations. The proposed solution is a typical CAD one, i.e., is aimed at reaching the best compromise with accuracy while respecting the constraint that the whole process be operable in a fast interactive way on ordinary workstations. For this purpose the CAD procedure has been subdivided into three independent segments, that is, i), the 3-D thermal analysis of microwave semiconductor devices by an electromagnetic analogy, ii), the device thermal modelling based on parameter extraction from temperature-dependent measured information, and iii), the extension of the harmonic-balance technique for nonlinear circuit analysis to include the determination of the (possibly time-dependent) peak temperatures in the active devices.

The basic assumption is that for the sake of circuit simulation it is sufficient to represent each active device by a thermal resistance and a thermal capacitance. This is acceptable in most practical cases, since the circuit designer is usually mainly interested in the peak temperature reached inside each device during the circuit operation, and in the effects of this temperature on circuit performance. The existence of thermal couplings can be accounted for by representing a set of devices by means of a thermal conductance matrix and a thermal capacitance matrix. The device thermal analysis is carried out by the integral equation method in analogy with microstrip problems, and is fast enough to allow the chip three-dimensional geometry and full layout to be directly taken into account even for complex multiple-finger configurations. The results of this analysis are the device thermal parameters as well as a 3-D map of the temperature distribution inside the chip. Both are in good agreement with experimental data obtained by infrared scanning techniques. The device thermal parameters are then used as inputs to the parameter extraction process for the identification of a temperature-dependent device model, and to the subsequent electrothermal nonlinear analysis. The need for solving the coupled heat flow and charge transport equations in the semiconductor is avoided by resorting to empirical modelling. The required input information consists of DC drain characteristics measured with the device in thermal equilibrium and at room temperature (pulsed DC), and of bias- and temperature-dependent scattering parameters.

Device thermal analysis

The 3-D thermal analysis is based on the assumption that all heat transport mechanisms except conduction in the semiconductor are negligible, so that the side walls of the chip can be treated as adiabatic. The device is described by the linear dimensions of the chip (which is assumed to be of rectangular shape), and the layout of its electrode pattern. The layout is arbitrary, with the only restriction that it must be possible to subdivide it into rectangular segments with the sides parallel to the coordinate axes. The segments are assumed to be isothermal. The subdivision can be refined to any required degree in order to account for the nonuniformity of the electrode temperatures. The device backplane is assumed to be held at a known uniform temperature.

The Fourier equation describing the heat flow reduces to the Laplace equation under stationary conditions. Thus the temperature distribution inside the chip is similar to the potential distribution for an equivalent microstrip problem having the same geometry, with the chip walls replaced by ideal magnetic walls. The problem is solved by the integral equation method. A high-accuracy universal two-dimensional look-up table for the Green's function is first developed and stored in the computer memory. This table is then used to efficiently convert the boundary-value problem into a linear algebraic problem from which the thermal conductance matrix of the set of segments is generated. The

segment temperatures and the thermal resistance are then found by solving a DC circuit problem. Three kinds of boundary conditions are allowed, that is, i), thermally active segments (heat sources) for which a known power dissipation is specified, ii), segments of unknown (floating) temperatures, and, iii), segments connected to ground by a priori known lumped thermal resistances. The latter are introduced to approximately account for the effects of via-hole grounding. For a MESFET the heat sources are physically identified with the gate fingers. The Green function data base then provides the temperature distribution inside the chip, from which the device thermal capacitance is derived. The nonlinear thermal effects arising from the temperature dependence of the thermal conductance are accounted for by the Kirchhoff transform [2]. The self consistency of the heat sources is automatically ensured by the solution of the electrostatic problem.

Fig. 1 shows the computer-generated temperature distribution at the air-semiconductor interface for a 20-gate FET geometry. For a medium-power FET manufactured by Alenia the analysis was able to predict the temperature distribution in the electrode region within ±3°C of the actual temperature measured by an infrared scanning technique. In particular, the simulated heat sinking effects of the source grounding pads, and, to a lesser extent, of the gate and drain bonding pads, which are evident in fig. 1, are closely confirmed by measurements.

Device modelling

The thermal resistance computed in the way discussed above is used to derive a nonlinear temperature-dependent empirical model for the microwave FET. The input information consists of the drain characteristics measured with the FET at thermal equilibrium with the ambient and in pulsed-DC conditions, i.e., with the device held at room temperature. The two sets of experimental curves obtained in this way for a 1 mm device are shown in fig. 2. The nonlinear drain current source is described by the empirical model [3]

$$i_D(V_G, V_D, T) = I_{DSS}\left(\frac{T_R}{T}\right)^{\eta}\left[1 - \frac{V_G}{V_p(T) + \gamma(T)V_D}\right]^{[\alpha(T)+\beta(T)V_G]}(1 + \lambda V_D)\tanh\left(\frac{\delta V_D}{1 - \varepsilon V_G}\right) \quad (1)$$

where I_{DSS}, η, λ, δ, ε, are model parameters and V_G, V_D are the intrinsic gate and drain voltages. T is the device absolute temperature and T_R is the known room temperature. All the temperature-dependent parameters in (1) are described by linear models of the form

$$A(T) = A' + A''(T - T_R) \quad (2)$$

where A stands for V_p, γ, α or β. Initially η and the A"s are set to 0, and the remaining model parameters are identified at room temperature by fitting the isothermal drain characteristics. At each bias point the device operating temperature is then found by solving a nonlinear equation of the form $T = \theta(T)\, P_d$, where $\theta(T)$ is the temperature-dependent thermal resistance [2] and P_d is the dissipated (measured) DC power. The whole set of parameters is then adjusted by fitting the computed non-isothermal drain characteristics to the measured ones. Fig. 2 shows that the model defined by (1), (2) can provide an excellent fit to the measured characteristics both in isothermal and in thermal equilibrium conditions. The same model is used in fig. 3 to reproduce a set of measured isothermal drain characteristics of a 300 µm device. In this case the device temperature is kept constant to the indicated value by changing the temperature of the heat sink. Once again the model provides an excellent fit to the measurements.

Reactive effects in the nonlinear device are described by a charge-based two-port capacitance model. A simple linear dependence of the stored charges is assumed according to available measured information [4]. The model coefficients are obtained from the scattering matrices measured at several bias points in thermal equilibrium conditions, taking into account the computed device temperature at each bias level.

Electrothermal circuit simulation

The electrothermal analysis is carried out by an extension of the well-known harmonic-balance (HB) technique [1]. Each temperature-dependent nonlinear device is described by a set of parametric equations including the device peak temperature among the state variables. In steady-state multitone operation, both the device temperatures and the electrical signals are represented by multidimensional truncated Fourier expansions. Since the thermal time constants of real devices are much longer than the RF period, only low-frequency components are usually sufficient for an adequate description of the temperature waveforms. Thus the temperature spectrum is defined as the baseband part of the signal spectrum. The state-variable harmonics represent the problem unknowns. Since the device equations are temperature-dependent, and in turn the device temperatures depend on the voltages and currents at the device ports through the internally dissipated powers, all these unknowns are coupled and must be determined by the numerical solution of a unique nonlinear system.

This solving system is an extension of the usual harmonic-balance system. The latter still has to be satisfied, but is now coupled with a set of thermal harmonic-balance equations which are derived from the thermal balance of the active devices. These thermal equations are formulated in the frequency domain by imposing the conditions that the harmonics of the time-dependent balance of heat flow vanish for each device. The solution simultaneously provides the electrical regime of the nonlinear circuit and the time-dependent peak temperatures in the nonlinear devices. Both single-tone and multitone excitations can be dealt with, so that the electrothermal analysis can be performed both in CW and in pulsed-RF conditions. The thermal nonlinearity of real devices can be taken into account in the simulation [5].

References

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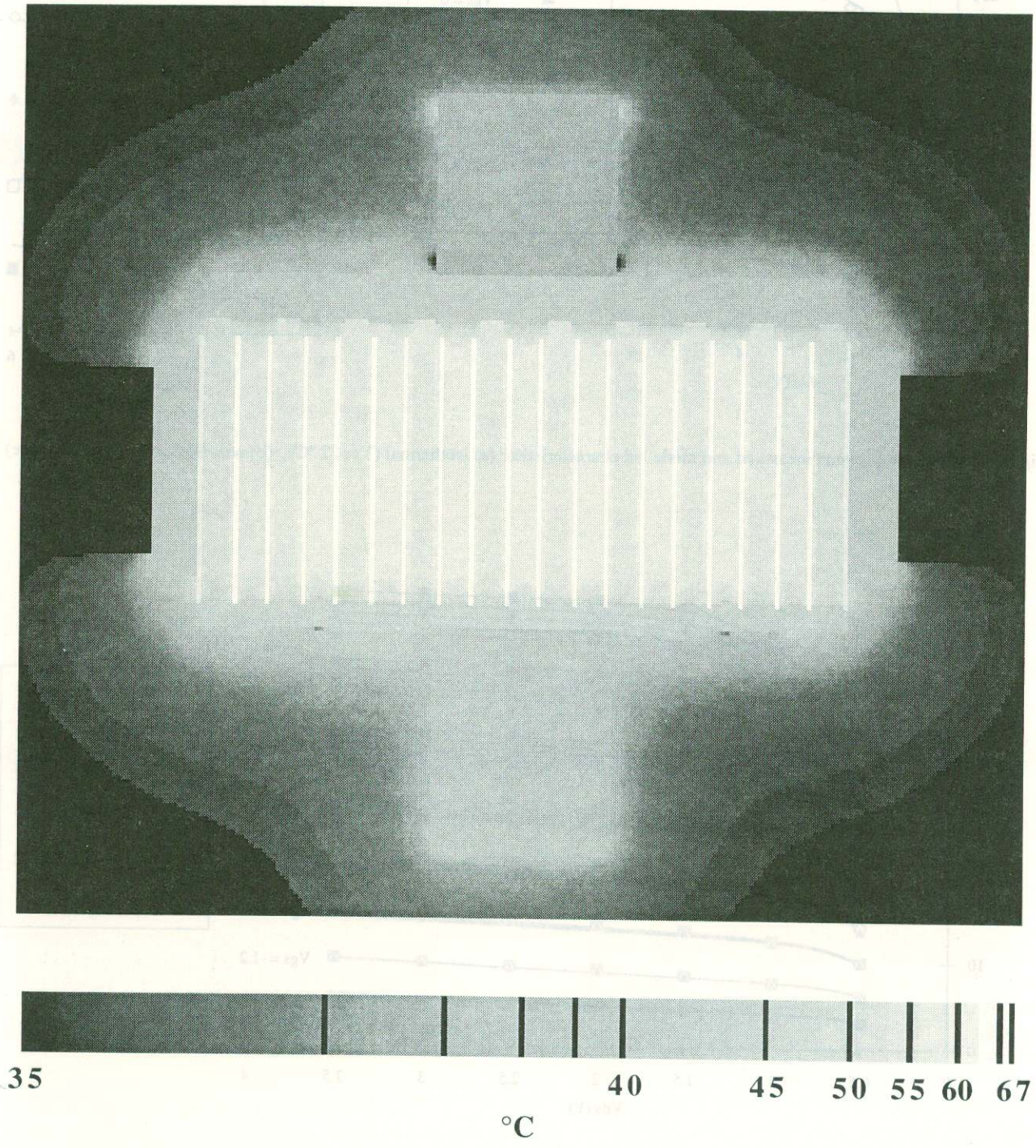

Fig. 1 - Computer-generated temperature distribution for a 20-gate FET geometry.

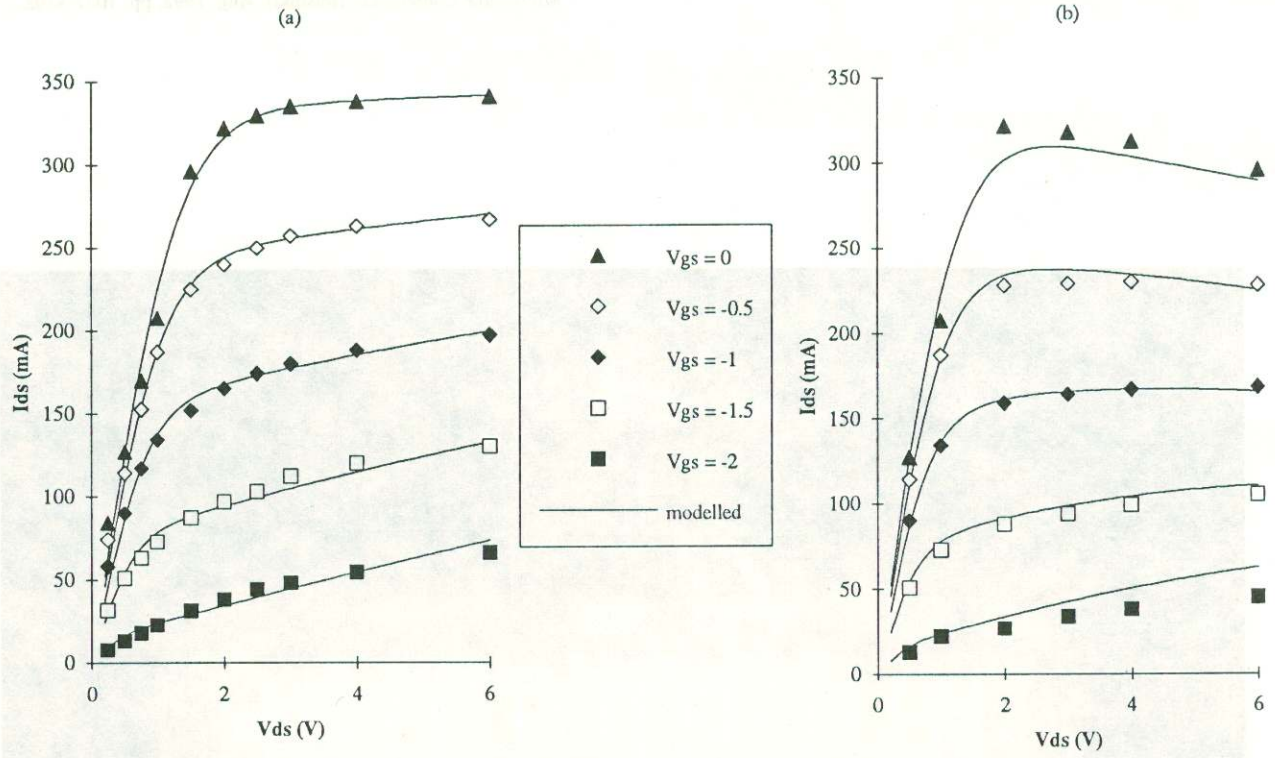

Fig. 2 - Comparison between measured and modelled characteristics: (a) isothermal (T = 27 °C), (b) non-isothermal. (1mm device)

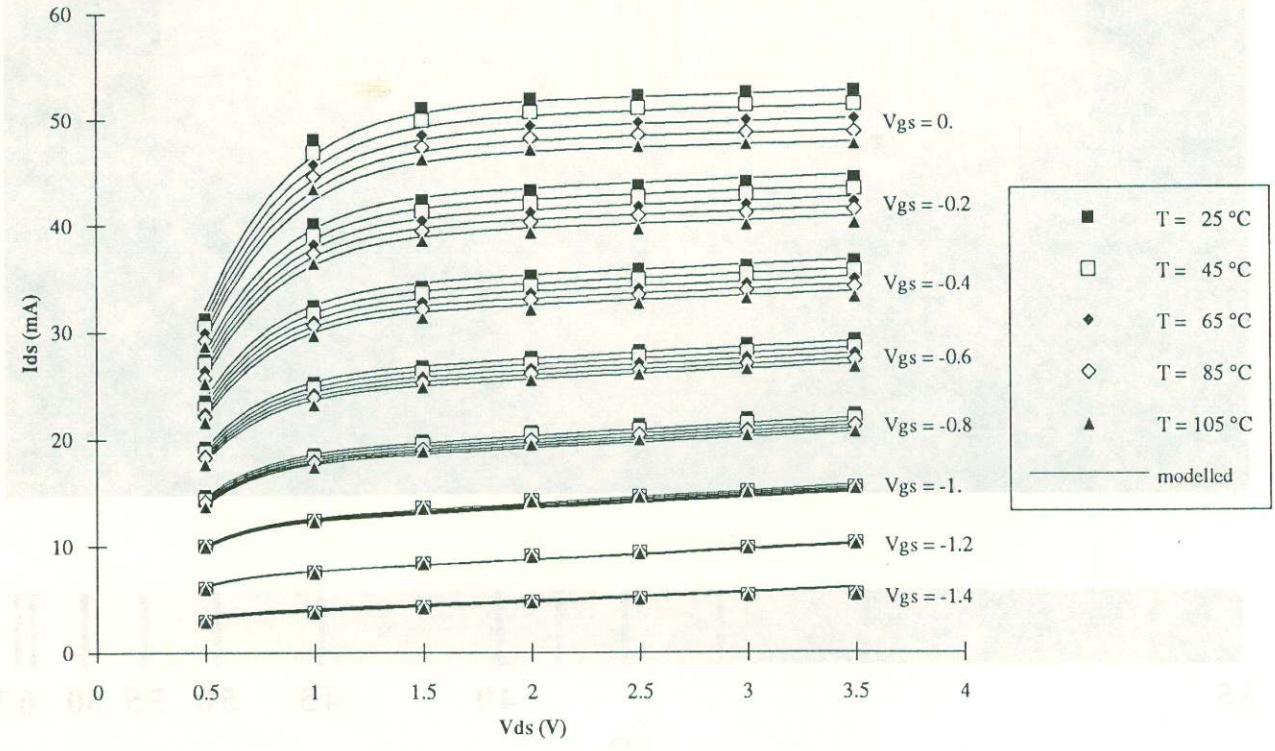

Fig. 3 - Comparison between measured and modelled isothermal characteristics at different chip temperatures. (0.3mm device)