ADJUSTABLE BANDWIDTH GAAS MONOLITHIC TRANSIMPEDANCE AMPLIFIER WITH AGC FOR O/E RECEIVERS UP TO 2.5 GBIT/S

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ABSTRACT

A monolithic transimpedance amplifier with adjustable bandwidth for optical links in the range 155 MBit/s to 2.5 GBit/s is presented. The circuit has been designed and fabricated utilizing commercially available 0.5μm gate length GaAs MESFET process. The gain of the circuit is 85 dBΩ at 1.75 GHz bandwidth, and the Gain*Bandwidth product is near constant for other settings in the mentioned range. Besides, the amplifier includes a 45 dB AGC section, and its output is ECL compatible.

Keywords: Transimpedance Amplifiers, Optical Receivers, Optical Communications

1. INTRODUCTION

The development of new broadband ISDN services will require in the next future to have the capability to update the access network by substituting the present copper pairs technology by optic fiber. The main obstacle for optic fiber diffusion in the external plant is the high cost of the electronics involved. The performance of this equipment defines the maximum length of the passive networks, or the separation between repeaters in the case of active links.

A direct way of decreasing the cost of the electronics involved is to reduce the number of circuits necessary to achieve the required functionality, allowing also a significant size reduction of the receiver. At the same time, an important reduction of the influence of parasitics and long signal paths present in hybrid multicircuit boards and discrete element hybrid solutions is obtained. Future developments will be constrained in same line as these effects are specially pernicious when working at high bit-rates.

Several efforts have been driven recently in order to increase the level of integration of optical receivers (Refs. 1-2), in this paper we present a circuit that implements all the analog functions required to convert to logic levels the current generated in a photodiode.

2. CIRCUIT DESIGN

The circuit has been custom designed and fabricated using a commercial 0.5μm gate length GaAs MESFET process. The circuit is composed of three main sections: a transimpedance preamplifier, a controllable gain section to implement an AGC, and a 50Ω ECL compatible output buffer.

Circuit functionality was specified to allow it to be used in both direct detection and coherent systems. As a result of that, the amplifier developed is suitable to be applied to direct detection systems up to 2.5 GBit/s and also to coherent systems at 622 MBit/s. The controllable gain section allows to prevent from signal limitation when the circuit is used to build coherent receivers, and extends dynamic margin when employed in direct detection systems.

A block diagram of the circuit is presented in figure 1, where dot outlined blocks are external loops not included on-chip as both of them are low frequency feedbacks. DC feedback loop is only necessary when tight DC output voltage control is required, and AGC feedback loop must be used when focusing on wide dynamic margin applications.

DC coupling has been used along the circuit. Because wide supplies voltages margins were desired, self-biasing techniques have been applied to each one of the sections of the circuit. These mechanisms have been optimized as much as possible without compromising RF performance by DC simulation of the whole circuit. As a result of that, the circuit admits V_{DD} voltages in the range varying from 4.5V to 6.0V, and V_{SS} between -3.5V and -5.0V. Power consumption of the circuit is contributed by the preamplifier stage, the controllable gain stage and the output buffer in 0.92W, 0.95W and 0.33W respectively, giving a global consumption of about 2.2W.

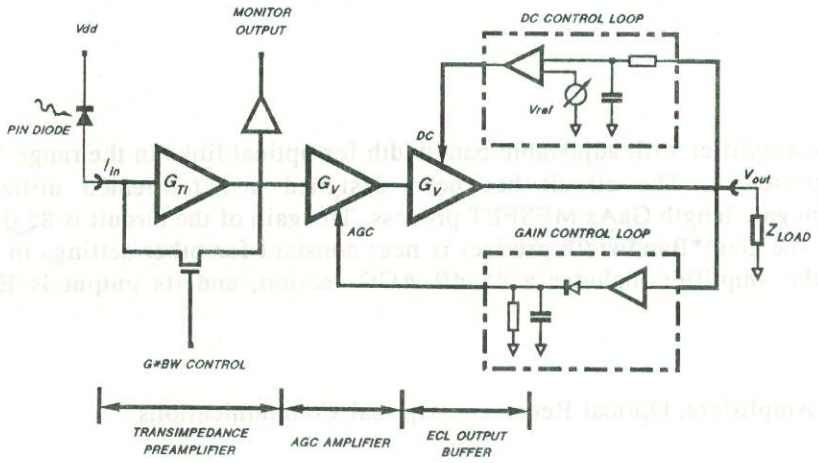

Figure 1: *Block schematic of the circuit.*

Actual chip size is 3.9 mm by 3.1 mm. Decoupling capacitors and protection mechanisms of control inputs have been on-chip included. Independent supply pads have been used in the first version of the circuit to allow bond wire parasitics influence reduction and separated external decoupling networks for each one of the sections. The whole circuit has 83 MESFETs of gate widths between 25µm and 400µm. A microphotograph of the die is shown in figure 2.

2.1 Transimpedance preamplifier

A cascode based transimpedance preamplifier topology has been developed achieving a good compromise among noise, bandwidth and gain characteristics, while obtaining at the same time the required bias point stability. The usual feedback resistor R_F has been substituted by a 25µm gate width MESFET working in the linear region. This allows to perform a bandwidth adjustment while maintaining constant the G*BW product. The feedback loop impedance was designed to allow bandwidth settings in the range 120 MHz to 1.9 GHz, with an equivalent resistance of 8.7 KΩ and 1.2 KΩ respectively.

A model was developed to simulate the behavior of the feedback MESFET at different gate control voltages. Parasitic capacitances of this transistor contribute slightly to bandwidth limitation as Miller effect on the first stage has been deliberately decreased but not completely eliminated. In this way, photodiode capacitance does not impose drastical bandwidth reductions, as simulations predicted.

The input equivalent noise current (i_{enc}) has been minimized by simulation considering the noise contributions of all the elements of the circuit, although only first stage has significant effect on noise. Input MESFET size and bias point providing best noise-gain compromise have been determined by software optimization (Ref. 3). This has been done in conjunction with the rest of the parameters corresponding to the other elements comprising the stage.

This section includes two output buffers following the preamplifier. One of them serves to feed the second section of the circuit, and the other provides a monitor output to have external information of received signal level independently of the AGC state.

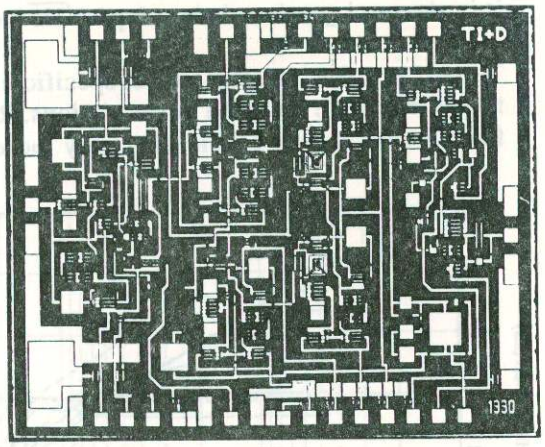

Figure 2: *Microphotograph of the circuit.*

2.2 Controllable gain section

A three stage distributed feedback controllable gain amplifier has been designed to obtain a wide control margin while maintaining a flat band response, and a 3 dB cutoff frequency of about 2 GHz independent to gain control state. Feedback control has been implemented using 100μm gate width MESFETs working as variable resistors within each one of the stages. A control margin in excess of 45 dB was simulated. A mechanism has been designed in order to allow desired gain to be set even by manual control. Typical values of control voltage required to cover the whole margin are between 3.0V and 5.5V.

2.3 Output buffer

The output buffer was designed to provide interfacing compatibility to ECL logic levels, while offering a good output match to 50Ω. This allows to use the circuit in both analog or digital applications. In analog mode, the AGC section will guarantee that the whole circuit behaves as non-limiting. The buffer was specified to have higher bandwidth than previous section, while less importance was given to the achieved gain.

3. CIRCUIT PERFORMANCES

The three sections that compose the circuit have been also implemented separately to allow an individual and more precise characterization. Measurements were performed with on-wafer high frequency test probes.

Results of the measurements realized on adjustable BW transimpedance section for various bandwidth adjustments are presented in figure 3. Bandwidth can be adjusted between 120 MHz and 1.75 GHz in a continuous way, with gain varying in the margin from 78 dBΩ to 57 dBΩ depending on the bandwidth. Expected functionality of the circuit has been achieved, allowing it to be applied to receivers working at different bit rates. This result probes the validity of the model used to characterize feedback MESFET as a variable impedance of low-medium magnitude. Curves corresponding to high gain and narrow bandwidth differ from measurements in a higher degree because the model is not so good to characterize high impedance MESFET state at frequencies over hundreds of megahertzs.

The response of the AGC section is shown in figure 4. A control margin in excess of 45 dB has been achieved. Desired gain can be easily set even manually, as is shown in the figure, where approximate gap between curves is about 3 dB. This section has a 3 dB cutoff frequency higher than 2 GHz in the whole margin of controllability.

The output buffer has a -3 dB cutoff frequency of 2.7 GHz with 7 dB of s_{21} gain. A VSWR of 1.3:1 ±10% up to 2.2 GHz has been obtained, thus pointing out a good match over the whole band of interest. Compression point was measured to be above 5 dBm, independently of the bandwidth and gain settings. The whole circuit has a inferred s_{21} in excess of 55 dB.

Noise measurements for different bandwidth settings were performed, they appear in figure 5. As it is shown, i_{enc} values below 5 pA/$\sqrt{Hz}$ have been achieved for bandwidth settings up to 700 MHz.

To perform O/E measurements, specific carrier and housing were developed. Carrier parasitics and transitions were included in simulations. Results showed a bandwidth degradation of about 150 MHz from previous ones considering only those parasitics due to bonding transitions. Receiver response obtained using a commercial pin photodiode is presented on figure 6, where upper traces correspond to two different bandwidth settings. The response was measured by using the principles of optical mixing applied to coherent systems, where the beat of two lasers feeds the photodiode (Ref. 4).

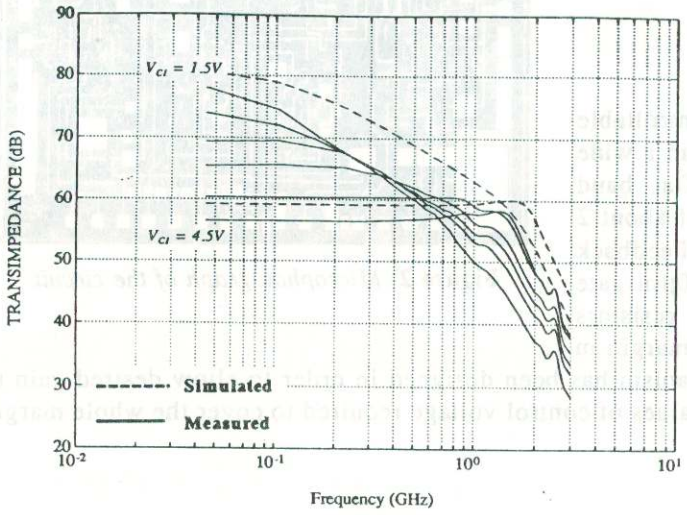

Figure 3: *First section at several BW settings.*

A view of the receiver mounted to characterize the system behavior of the amplifier is on figure 7. Direct detection experiments were performed to characterize the circuit. Sensitivity measurements were realized using a 1.3µm laser source carrying a 2^7-1 pseudo-random NRZ bit-stream at 622 GBit/s. Gain-bandwidth control was set to 500 MHz to measure a sensitivity of -27.1 dBm for BER equal to 10^{-9} without applying any penalty correction. Better result should be obtained improving fiber to PIN coupling, as theory claims for about -30.8 dBm with values of i_{enc} about 4 pA/$\sqrt{Hz}$ in the noise band as corresponds to the bandwidth set. No noise filtering has been applied on these measurements. Maximum optical level of -4.5 dBm was applied to the receiver without producing saturation. Optical dynamic margin in excess of 30 dB has been calculated.

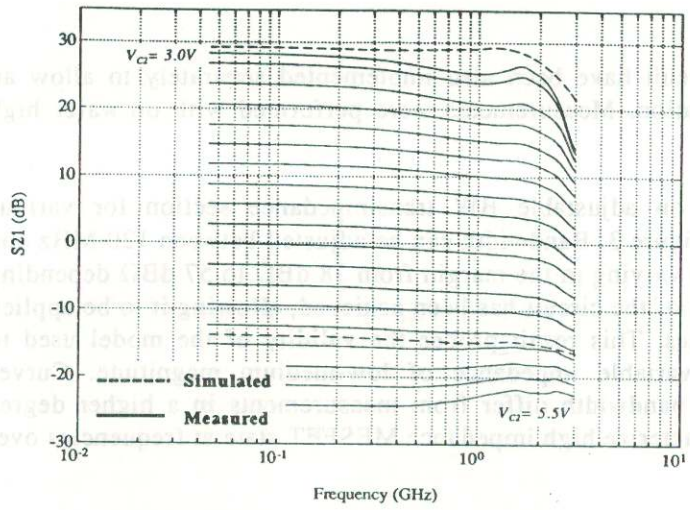

Figure 4: *Controllable gain section response.*

4. THERMAL CONSIDERATIONS

To achieve an uniform thermal dissipation, the transistors have been properly distributed across the chip surface. Three dimensional thermal simulation of the circuit under worst case nominal conditions (maximum supplies voltages) have been performed using in-house developed software. This has been done in order to find the most critical points on the surface of the circuit. Hot spot temperature increment of 25.8°C in the channel of the hotest MESFET has been calculated using an estimator. From this result, and considering the thermal impedances of the die-attach epoxy and package, a worst case maximum hot spot temperature increment over ambient of 53°C has been obtained. This value ensures an appropriate reliability at least up to 60°C ambient temperatures. Circuit performances have been tested to vary less than 5% within a temperature margin between 10°C and 50°C.

5. DESIGN METHODOLOGY

Due to the complexity of the circuit, it has been necessary to improve the existing CAD environment to enable a short and accurate design cycle, suppressing the need to generate an S-par file for every individual type of element and bias point conditions used in simulations.

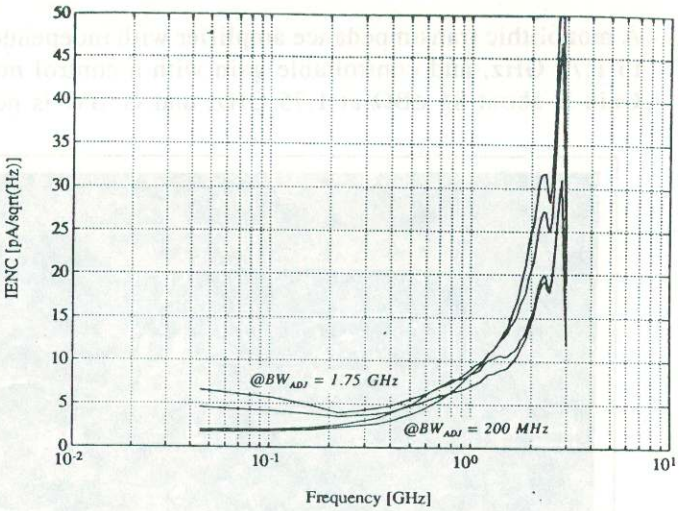

Figure 5: *Input noise measurements (i_{enc}).*

Customizing CAD can provide significant time and effort savings in the design phase of MMICs. The inclusion of user defined models in a commercial simulator by coding electrical dependences, and compiling them joined with the program allows drastical reduction of the time required to describe a circuit, eases modifications, and reduces the whole time necessary to perform simulations. The effort required to add user defined models is widely compensated by the elimination of the necessity of handling a number of s-parameters files (or a large subcircuit description code, that would be required otherwise).

Our design environment has been improved in several ways, by adding parametrizable custom models, schematic symbols, and layout representations to a commercial CAD software. The basis of the system is Academy™ from EEsof™, that includes the well known linear simulator Touchstone™, used to perform RF simulations. Linear models for the element types more frequently used when designing MMICs were created, this includes GaAs MESFET transistors, diodes, passive elements and parasitic transitions. Transistor model includes a complete noise characterization.

A schematic shape for each new added model was also created. This permits to distinguish elements employing user defined models of the ideal ones provided by the original software. Those original elements remain unmodified, and can be also selected when accessing element menus.

Macros were introduced to the software that enable automatic layout of individual passive elements form the dimensional parameters given to the elements at the schematic level. This facility is specially useful when it is necessary to create layouts with many elements of different values.

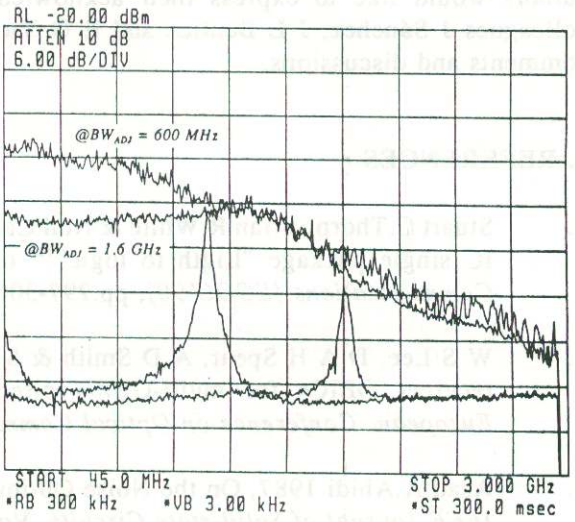

Figure 6: *O/E transfer function at two different bandwidth settings.*

DC simulations of the complete circuit were realized on Pspice™. Some stages were also simulated using Libra™ in order to compare the results obtained with different simulators and models. A custom modified Statz model was used in Pspice™ simulations, while the modified Curtice and Ettenberg model with cubic fit for I_{DS} was employed on Libra™. A good agreement between results obtained from both ways was observed, thus giving confidence to the expected DC behavior.

6. CONCLUSIONS

A monolithic transimpedance amplifier with independent adjustable bandwidth in the range 120 MHz to 1.75 GHz, and controllable gain with a control margin in excess of 40 dB has been developed. Gain is about 85 dBΩ at 1.75 GHz, and G*BW is near constant for other bandwidth settings. The i_{enc} is below 5 pA/$\sqrt{Hz}$ for bandwidth settings up to 700 MHz. The output of the circuit is ECL compatible, and its VSWR is about 1.3:1 over the whole band. Actual chip size 3.9mm by 3.1mm. A number of MESFETs (83) of different gate widths between 25µm and 400µm are properly distributed across the chip surface to allow an uniform thermal dissipation.

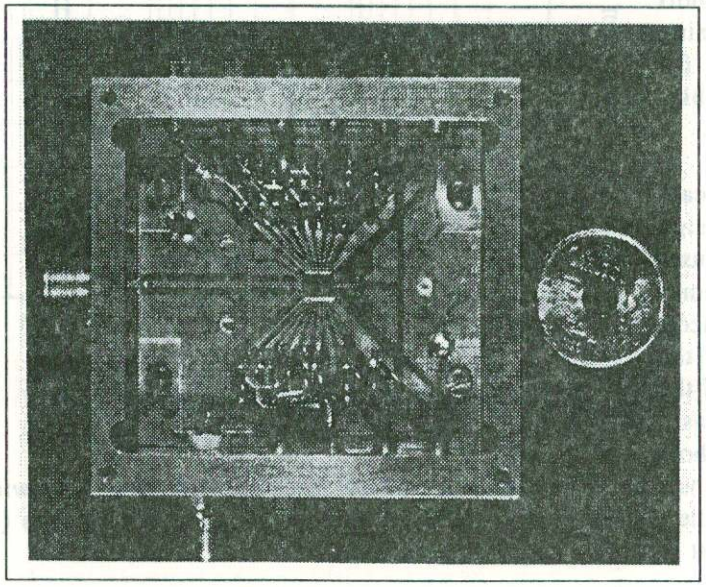

Figure 7: *Developed fixture.*

7. ACKNOWLEDGEMENT

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