A GaAs MONOLITHIC V-BAND RECEIVER FOR SPACE COMMUNICATIONS

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ABSTRACT

A state-of-the-art V-Band millimeter-wave agile receiver subsystem, consisting of an RF module and a phase-locked oscillator (PLO) module, has been designed, fabricated, and tested. All of the active circuits within this subsystem (with the exception of the operational amplifiers in the phase-locked loop) are GaAs MMICs. The RF module includes a 0.1 micron pseudomorphic HEMT-based LNA, a Schottky diode subharmonically pumped mixer and a 7.5 to 30 GHz LO multiplier/amplifier chain designed around a 0.25 x 400 micron power MESFET. The receiver module noise figure is 7.5 dB DSB maximum and the VSWR at the RF input port is less than 2:1. The PLO module includes a linear 7.5 GHz VCO and other commercial MMIC chips which complete the phase-locked loop. In both modules, the MMIC chips have been assembled into light-weight, compact, laser scalable housings, making them attractive for use in space-based communication systems. In addition, the MMIC components have been put through and have passed a full round of radiation testing, including exposure to gamma and x-ray transient dose rates of 3×10^{12} and 5×10^{12} RAD(Si)/sec, respectively, as well as neutron and total dose tests.

Keywords: V-Band Communications Receiver, MMIC Technology, Radiation Hardness

1. INTRODUCTION

State-of-the-art GaAs monolithic technology offers significant advantages in the development of millimeter-wave transceivers. These subsystems need to be compact, light-weight, power efficient, and highly reliable. In some applications, radiation hardness is required as well. GaAs monolithic technology offers superior performance, cost, repeatability and reliability at millimeter-wave frequencies. This paper describes the design, technology development, and test results of a state-of-the-art GaAs monolithic, fast locking receiver for space-based applications.

The low noise characteristics of the subsystem were realized through the use of a monolithic LNA which incorporated pseudomorphic technology and an efficient Schottky-based monolithic mixer. The stable characteristics of the receiver's LO source are derived through the use of phase locking techniques. All of the active circuits in this subsystem are radiation-hard GaAs monolithic chips with the exception of the operational amplifier which utilizes special radiation-hard silicon technology. All components have been tested to various hardness levels.

2. RF MODULE DESCRIPTION

The RF module was developed by Alpha Industries as part of a GAMMA Monolithics[4] team effort under the sponsorship of Martin Marietta Space Systems and the U.S. Air Force. The module uses various GaAs MMIC technologies in performing functions such as low noise amplification, signal mixing, LO signal multiplication, and LO signal amplification. When the 60 GHz development effort began at Alpha, tradeoff studies were conducted to determine a system block diagram. Since minimizing chip count was a major consideration, we chose to utilize our expertise in subharmonic mixers, allowing

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the use of the 30 GHz LO signal produced by the PLO module and the multiplier chain in the RF module. This eliminated the need for a 30/60 GHz multiplier and possibly a 60 GHz amplifier in the receiver without seriously compromising system noise figure performance. Figure 1 shows the final block diagram of the RF Module. The V-Band RF signal is received via a WR-12 waveguide machined into the module wall. An antipodal fin-line circuit, printed on an alumina substrate, is used to transition from the TE_{10} waveguide propagation mode to the quasi-TEM microstrip mode used for the LNA and subharmonic mixer. The C-Band LO source is provided via a coaxial connector, quadrupled in frequency, and amplified to provide sufficient drive to the mixer. Finally, the IF signal is amplified by a low noise, fixed frequency amplifier.

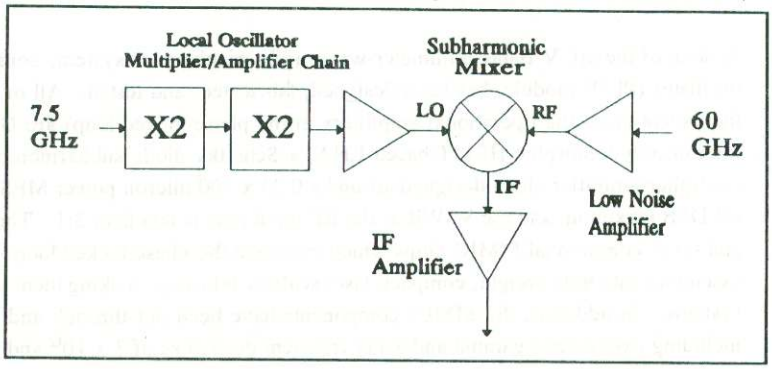

Figure 1
RF Module Block Diagram

2.1 Component Descriptions

In order to reduce noise figure as low as possible, the RF chain starts with a two stage LNA based on 0.1 x 50 micron pseudomorphic HEMT devices. The amplifier, developed by Martin Marietta Laboratories of Baltimore, Maryland as part of the GAMMA Monolithics team effort previously mentioned, exhibited a noise figure of 4 dB with an associated gain of 12 dB at 60 GHz. Following the LNA is a GaAs monolithic X2 subharmonic mixer. The mixer utilizes an antiparallel pair of Schottky diodes embedded in microstrip circuitry. The diodes exhibit a series resistance of 8 ohms and a capacitance of 0.035 pF, allowing efficient frequency conversion at 60 GHz. Noise figure (see figure 2) is typically 7-8 dB across a 10% bandwidth. The mixer, due to the self-biased nature of the subharmonic configuration, requires as little as +6 dBm LO drive. The RF and LO matching networks and the IF filter circuit are realized using microstrip distributed transmission line techniques. The entire circuit including DC blocking functions was fabricated on 4 mil thick GaAs using a high quality, high volume Schottky diode based manufacturing process. IF amplification is achieved using a commercially available low noise GaAs amplifier chip.

The LO Multiplier/Amplifier chain (Ref. 1) was constructed using two X2 multiplier chips and a wide band post amplifier. All three circuits are constructed on 4 mil GaAs using a 0.25μm MESFET based production process. The 7.5/15 GHz multiplier was designed to receive the C-Band LO signal and multiply it to Ku-Band while simultaneously providing flat conversion loss (as low as 7 dB) vs. frequency and input power, good fundamental suppression, and low VSWR. The 15/30 GHz multiplier was likewise designed to further multiply the LO signal to Ka-Band and exhibited a conversion loss as low as 4 dB. This doubler is a balanced design which utilizes Lange couplers matched at the input and output frequencies for power division and power combining, respectively. This ensures high fundamental suppression, since the output coupler combines 180 degrees out of phase at the input frequency. The 30 GHz amplifier is a 2-stage design with a balanced output to achieve higher output power and a good output match. Power division and combining are achieved through the use of Lange couplers. The entire chain exhibits approximately 3 dB of conversion gain and provides a +13 dBm signal level to the subharmonic mixer.

Although the frequency doublers exhibited acceptable performance for this application, the DC bias and RF input power operating points were found to be somewhat critical to optimum performance. As an alternative approach, varactor multipliers are also being developed using Alpha's existing monolithic varactor process. Varactors are the traditional means for performing efficient frequency conversion and have been successfully implemented in waveguide and microstrip configurations (Refs. 2,3) without the bias sensitivity and power consumption of FET-based multipliers.

The MMICs described coupled with a commercially available low noise GaAs MMIC IF amplifier and off chip bypass capacitors are die attached to the floor of a light weight, gold plated aluminum housing. The entire module can be laser sealed in an inert atmosphere to military specifications.

2.2 RF MODULE PERFORMANCE

The RF module noise figure vs. RF frequency is shown in figure 2. This data shows a maximum DSB noise figure of 7.5 dB across a 10% bandwidth at V-Band with a minimum noise figure of less than 5 dB. When integrated without the LNA, the receiver displayed an average noise figure that was 4 dB higher, as shown in figure 3. The RF input VSWR over the RF bandwidth is better than 2:1, while LO leakage out the RF port was negligible, due to the reverse isolation of the LNA and a mixer LO/RF isolation of about 25 dB. DC power consumption was approximately 2.5 watts. The overall module size was 50mm x 23mm x 15mm with a weight of approximately 48 grams.

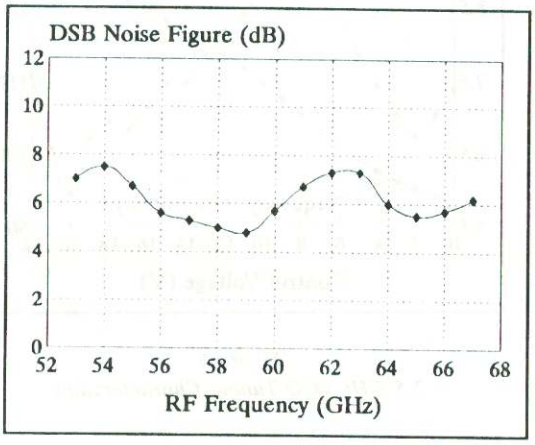

Figure 2
Noise Figure vs. RF Frequency
V-Band Receiver

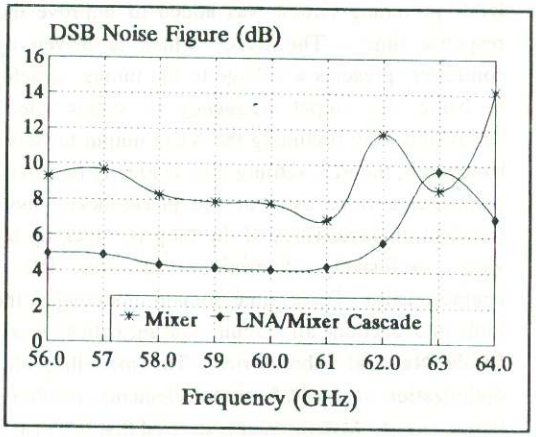

Figure 3
Noise Figure of
Cascaded LNA and Mixer

3. PHASE-LOCKED OSCILLATOR MODULE

System frequency accuracy and stability requirements dictated the use of a phase-locked oscillator (PLO) as the receiver's local oscillator. A PLO was jointly developed by Alpha Industries, as part of the Gamma Monolithics effort previously mentioned, and Sandia National Laboratories. Additional PLOs were also manufactured for a Sandia requirement. A make/buy component and block diagram tradeoff study resulted in the block diagram shown in figure 4 and the selection of a commercially available 7.5 GHz GaAs MESFET-based monolithic oscillator chip, packaged with and controlled by a hyperabrupt varactor diode. The oscillator exhibited a minimum output power of +12 dBm and a tuning slope variation of 2:1 or less over a 1 GHz tuning range (see figure 5), making it appropriate for phase-locked loop applications. A loop was constructed around the oscillator using commercially available GaAs or radiation-hard silicon monolithic chips. (GaAs parts were desired for their inherent radiation hardness.) Following the oscillator is a 7.5 GHz power MESFET amplifier, developed at Alpha using its 0.25 micron foundry, and a 10 dB GaAs microstrip directional coupler, also developed at Alpha. The through arm of the coupler leads to the output of the PLO. The coupled arm leads to

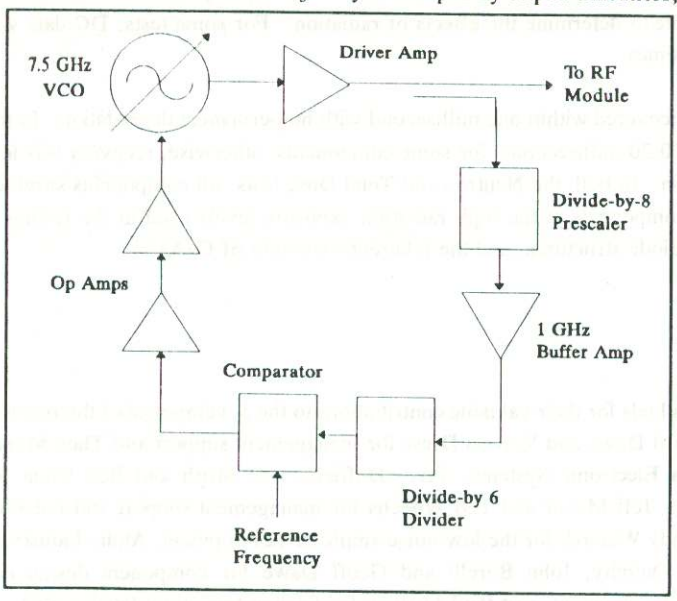

Figure 4
PLO Block Diagram

a cascaded divider chain consisting of a divide-by-eight prescaler, buffer amplifier, and a divide-by-six divider chip. The phase comparator outputs a DC level which is proportional to the phase difference between the reference frequency signal (approximately 150 MHz) and the output of the divide-by-six divider. The op-amp circuitry provides both the required loop gain as well as the active RC filter necessary to control the transient performance of the phase-locked loop. In addition, a DAC pretuning circuit was added to improve the PLL tuning response time. The DAC, which is driven by the system controller, presents a voltage to the tuning varactor of the VCO to bring the output frequency to within the PLL locking bandwidth. By pretuning the VCO output to be within the lock bandwidth, the PLL settling time is greatly improved. Wide-band components were used in the phase-locked loop so that the transient characteristics of the loop (ie. lock-up time or agility) were exclusively determined by the RC active filter characteristics. Direct time-domain modeling of the PLL, which took into account all circuit non-linearities, was performed at Sandia National Laboratories. This modelling allowed efficient optimization of the PLL circuit elements, resulting in maximum tuning speed. Measurements showed that the PLL with the DAC pretuning had a settling time of approximately 1.5 microseconds. This settling time was obtained while switching between output frequencies of 7.1 GHz and 7.9 GHz. As in the RF module, the above mentioned chips were assembled into a gold plated aluminum housing which can be laser sealed in an inert atmosphere.

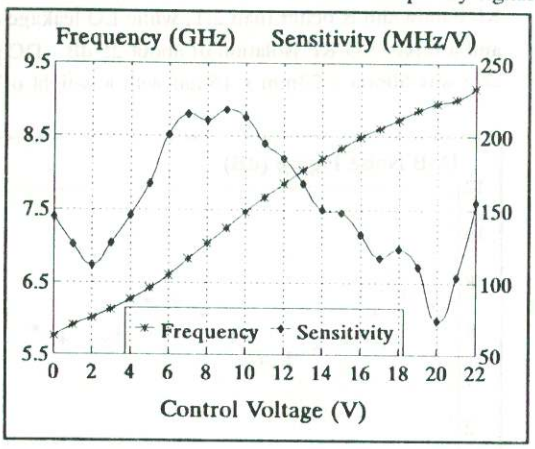

Figure 5
7.5 GHz VCO Tuning Characteristics

4. RADIATION HARDNESS TESTS

Radiation hardness tests using extremely high exposure levels were performed on individual components of the RF and PLO modules. Each component was mounted in its own test fixture and subsequently mounted to a large plate for radiation exposure. Tests were conducted by Sandia National Laboratories at their facilities in Albuquerque, New Mexico. RF and/or DC data was taken before and after exposure to determine the effects of radiation. For some tests, DC data was monitored during exposure to determine recovery times.

In the Gamma transient dose test, all components recovered within one millisecond with no permanent degradation. In the X-Ray transient dose test, RF recovery was slow (10-20 milliseconds) for some components; otherwise, recovery was less than one millisecond with no permanent degradation. In both the Neutron and Total Dose tests, all components survived without degradation. The survivability of these components at the high radiation exposure levels used in the testing is attributed to the material structures, the FET and diode structures, and the inherent immunity of GaAs.

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