INTERDIGITATED PLANAR SCHOTTKY VARACTOR DIODES FOR TUNABLE MMIC APPLICATIONS

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ABSTRACT

Techniques are presented for scale modelling interdigitated Planar Schottky Varactor Diodes (PSVDs) using an equivalent circuit model. A selection of low cost GaAs devices, with variations in the finger width and number of anode fingers, have been fabricated, measured and accurately characterized – well into the millimetric frequency range. From the results, a number of useful design rules are presented for the optimal choice of interdigitated PSVD topography. With the use of these rules, a 24x300μm experimental PSVD was accurately characterized.

Keywords: Varactor Diodes, Tunable MMICs

1. INTRODUCTION

Microwave circuits which facilitate some form of continuous tuning can be divided into two categories. The first category consists of applications where the tuning range is only dictated by the tuning ratio of a variable inductor or capacitor. Here, the tuning ratio is simply the square root of the Total Inductance Ratio ($TIR = L_{max}/L_{min}$) or Total Capacitance Ratio ($TCR = C_{max}/C_{min}$). The required value of TIR can be determined with the appropriate circuit topology for the active inductor. The required value of TCR can be determined with the appropriate topography and fabrication processing of the varactor diode. An application which falls into this category is the cascaded-match reflection-type phase shifter (Ref. 1).

The second category consists of applications where the tuning range is dictated by the difference in the value of the variable inductor ($\triangle L$) or capacitor ($\triangle C$). For example,

$$\triangle C = C_{max} - C_{min} = C_{max}(1 - 1/TCR)$$

Here, the required difference in capacitance can be achieved by selecting a realizable value of C_{max} and/or by using the appropriate device technology. Applications which fall into this category are numerous, including most reflection-type phase shifters (Refs. 2-6), loaded-line phase shifters, filters (Ref. 7), amplifiers and oscillators (Refs. 8-9).

Tunable Active Inductors (TAIs) can provide large values of both L_{max} and TIR. They use minimal chip space and can be fabricated using standard commercial foundry processing, i.e. no additional selective ion implantation/MBE or VPE grown layers are required. In addition, TAIs with very high Q-factors, in the range of tens of thousands, have recently been developed at King's. Applications of TAIs, with a TIR=20, has already been reported (Ref. 6). At present, however, active inductors have a number of major limitations. Their bandwidths are currently limited to a few GHz, the problems associated with their numerous bias requirements may be unacceptable and their power consumption is relatively large. The latter is a major disadvantage for space applications where power is at a premium.

Planar Schottky Varactor Diodes (PSVDs) are extensively used in microwave and millimeter wave monolithic circuits for tuning and mixing applications. For tuning application in the millimetric frequency range, which require small values of C_{max} and negligible parasitics, non-interdigitated diode topographies are used. With an appropriate non-uniform doping concentration profile, a medium value of TCR and a good Q-factor performance can be achieved. For tuning applications up to the millimetric frequency range, medium to large values of C_{max} are usually required. Here, interdigitated PSVD structures can be used to provide the extremes in value and the required TCR.

With a deep active n layer, having a non-uniform doping profile, and a buried n^+ contact layer, a medium value of TCR and a good Q-factor performance can be achieved. With the anode finger lengths increased, for a fixed anode-to-cathode separation distance, an approximately corresponding increase in C_{max} and TCR was found (Ref. 8). Also, with a recessed anode, the Q-factor performance will increase, however, this is at the expense of a significant reduction in the TCR (Ref. 8). An interdigitated PSVD with C(0)=0.8pF and a TCR=C(0)/C(-10)=56 has been reported (Ref. 8).

During fabrication, the PSVDs discussed so far generally require processing stages which are not generally offered as standard by the foundry, for realising the structure and/or providing the necessary doping concentration profile. As a result, these hyperabrupt devices are relatively expensive to produce. If only standard commercial foundry processing is to be used, a varactor diode can be simply realised by connecting together the drain and source terminations of a standard library cell MESFET – resulting in a single Schottky junction with an abrupt characteristic. The bias potential is then applied across the drain/source (cathode) and gate (anode) terminations. MMICs using such devices for tuning applications have been reported (Refs. 1-5,7-9). An illustration of the cross-section of the anode region for a typical $0.5\mu m$ MESFET is shown in Figure 1.

An accurate large signal equivalent circuit model for an interdigitated GaAs PSVD, based on the GEC-Marconi standard library cell F20-FET-6x150, has recently been reported (Ref. 10). The model demonstrates that an interdigitated GaAs PSVD can be very accurately characterized, with both forward as well as very large reverse bias potentials applied – well into the millimetric frequency range. Unfortunately, a great deal of tuning was required to determine the models lumped element values. As a result, the task of characterizing a large array of similar devices would be too labour intensive. An effective solution is to use direct scaling for some of the element values and tuning for others.

A small array of PSVDs, with variations in the finger width and the number of the anode fingers, have been fabricated, measured and accurately characterized. The conditions which enable direct scaling and some useful design guidelines which follow from the results are presented.

2. MODELLING

A photomicrograph of an array of interdigitated PSVDs, based on standard library cell MESFETs, can be seen in Figure 2. The equivalent circuit model for the 6x150μm PSVD, shown in figure 3, was used to accurately characterize the 4x150μm, 2x150μm, 1x150μm, 6x75μm, 4x75μm 2x75μm and 1x75μm PSVDs, by the appropriate scaling of some of the model's element values. Intuitively, the series resistance and all the capacitors should scale directly with the size of the PSVDs. It will be found that the series inductance should increase with an increase in the finger widths and/or a reduction in the number of anode fingers. However, direct scaling should not apply to this inductance, as it is distributed in nature.

It should be noted that direct scaling is only a good approximation. When the finger widths falls below about $75\mu m$, the level of confidence in the approximation deteriorates. This is because the fixed parasitic capacitances associated with the discontinuities between the gate and drain/source feed lines and the end of the fingers become more significant as the finger width decreases. Also, when the maximum differential path length (i.e. the difference between the maximum path length through the PSVD and the finger width) exceeds about $200\mu m$ (which corresponds to a PSVD with 6 anode fingers in this case) the level of confidence in the approximation diminishes. This is because the inductance in the gate and drain/source feed lines increases and becomes distributed in nature.

In addition to the array shown in Figure 2, a very large experimental 24x300μm PSVD was fabricated. For the layout of this device, four identical F20-FET-6x150 library cells were first combined and then the finger widths were stretched to double in size. A photomicrograph of the device is shown in Figure 4. In order to overcome the distributed inductance in the gate and drain/source feed lines, the model for the device was partitioned into 4 sections. Each section consists of a scaled model of a 6x300μm PSVD which taps into the feed lines at appropriate points. This modelling strategy is illustrated in Figure 5.

It should be noted that when the four F20-FET-6x150 library cells are combined during the layout design stage, two source fingers are directly overlapped at three places. As a result, there should be an appropriate reduction in the cathode capacitance to ground, C_k, in the four 6x300μm PSVD models.

3. RESULTS

The devices in Figures 2 and 4 were fabricated at the GEC-Marconi (Caswell) foundry, using their standard F20 process. This process provides 0.5μm gate length MESFETs, having a thin uniformly doped active layer, and very low inductance through GaAs vias. A CASCADE Summit 9000 probe station and a HP8510B automatic network analyser were used to perform measurements between 0.05 to 40.05GHz. Zero bias was applied to the devices.

As a good approximation, the delay and all the capacitance values in the equivalent circuit model, for all the various PSVD structures, were directly scaled to the zero bias values used in the 6x150μm model. The scaling factors for the capacitances are shown for various total gate widths, W_T, in Figure 6(a).

For a PSVD to be accurately characterized, the resulting simulation responses for the magnitude and phase of the anode voltage reflection coefficient, S_{11}, and the anode-to-cathode voltage transmission coefficient, S_{21}, must coincide with those of the measured responses, at all frequencies.

It was found that automatic optimization routines could not determine values of R_S and L_S that would satisfy the necessary conditions. This is due to the placement errors encountered when probing each device. As a result, fine adjustments had to be made to the lengths of the anode and cathode probe pads, l_p, and their corresponding fringe capacitance to ground, C_f. The most effective solution was to tune the values of l_p, C_f, R_S and L_S until the simulated and measured responses coincided across the 0.05-40.05GHz frequency range.

The resulting values of R_S and L_S are shown in Figures 6(b) and 6(c), respectively. From Figure 6(b), it can be seen that a reasonable fit exists between the modelled and directly scaled values of R_S. The overall results presented in Figures 6(b) and 6(c) confirm the trends that were expected intuitively.

The simulation and measured frequency responses for the 2x75μm, 4x75μm, 6x150μm and 24x300μm PSVDs are shown in Figure 7. From the power and phase responses in Figure 7, it can be seen that these PSVDs are accurately characterized. The same level of accuracy was also achieved with the other PSVD sizes.

4. DISCUSSION

The small errors found in the values of R_S and L_S can be attributed to the following factors:

- processing variations from device to device
- level of confidence in the measurement system's calibration
- inaccuracies in the characterization of the probe tip placement errors
- inaccuracies in the initial 6x150μm PSVD model's lumped element values
- level of confidence in the direct scaling approximation

With most of the above, simple techniques can be adopted to reduce the error function

A number of useful design rules for the optimal choice of interdigitated PSVD topology follow from the results presented in Figures 6 and 7.

- The zero bias junction capacitance, $C_J(0)$, linearly increases from 0.096pF to 1.155pF with a corresponding increase in total gate width from $75\mu m$ to $900\mu m$, irrespective of the finger width or number of anode fingers

- For a fixed value of junction capacitance (and, therefore, total gate width), by increasing the number of anode fingers and making the necessary reduction in the finger width results in:

  - a large reduction in the zero bias series resistance
  - a large reduction in the series inductance
  - a medium reduction in the parasitic cathode capacitance

- Reducing the finger width below about $75\mu m$ will no longer make direct scaling a good approximation

- Increasing the number of anode fingers beyond about 6 will no longer make direct scaling a good approximation unless the model is partitioned into sections

5. CONCLUSIONS

An array of interdigitated GaAs PSVDs, with different finger widths and number of anode fingers were fabricated, measured and accurately characterized. An equivalent circuit model for a 6x150μm PSVD has demonstrated that its lumped element values for delay, series resistance and all its capacitances can be directly scaled to accurately characterize PSVDs of different sizes. The results showed that the series inductance could not use the same direct scaling. In addition, a number of useful design rules are presented for the optimal choice of interdigitated PSVD topography.

By interpolation of the results presented, working values of the model's lumped elements can be extracted for a whole range of different interdigitated PSVD sizes – for the GEC-Marconi standard F20 foundry process only. Using this technique, an experimental 24x300μm PSVD was accurately characterized. With maximum dimensions of approx. 0.75mm x 0.35mm, the effective zero bias junction capacitance is 9.24pF.

Although these interdigitated PSVDs have a modest TCR and Q-factor performance, they require relatively inexpensive fabrication processing. As a result, these devices are expected to achieve greater popularity in microwave, millimeter-wave, wideband and ultra-wideband applications.

6. ACKNOWLEDGEMENTS

This work was supported by the Science and Engineering Research Council (SERC) UK, the Rutherford Appleton Laboratory (RAL) UK and by GEC-Marconi Materials Technology Limited, England.

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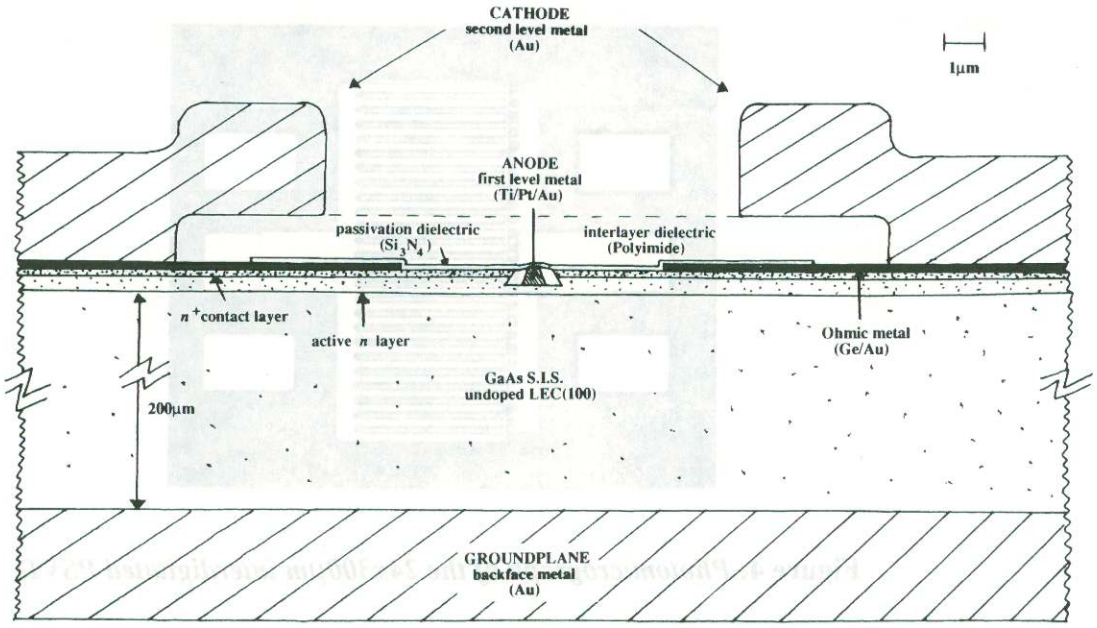


Figure 1: ***Gate region cross-section of a typical 0.5μm MESFET***

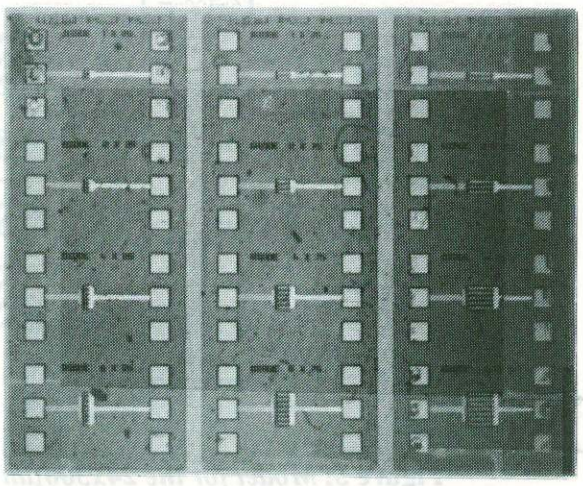


Figure 2: ***Array of interdigitated PSVDs***

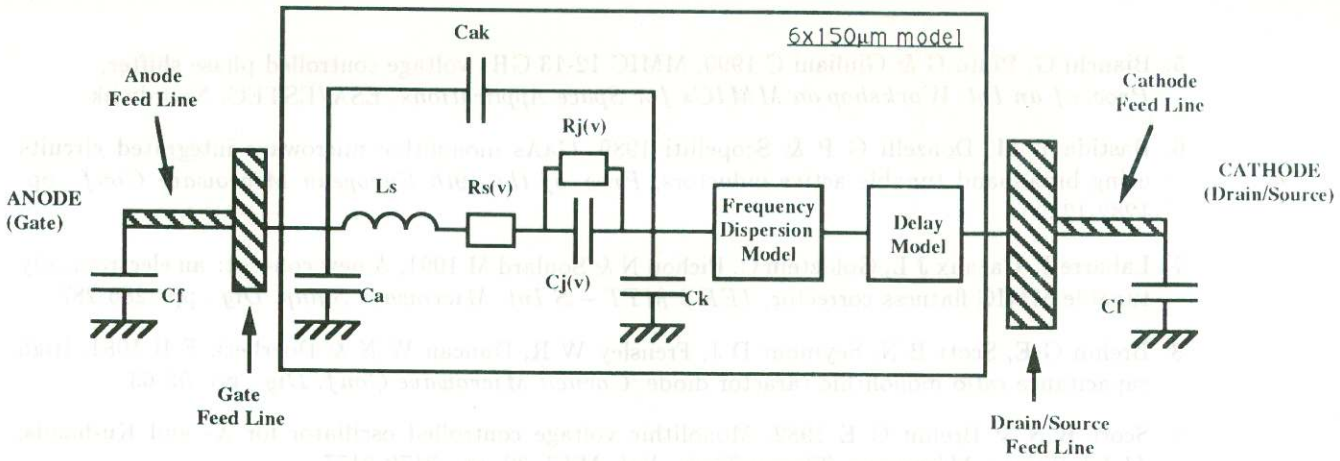


Figure 3: ***Millimeter-wave large signal model for GaAs PSVDs***

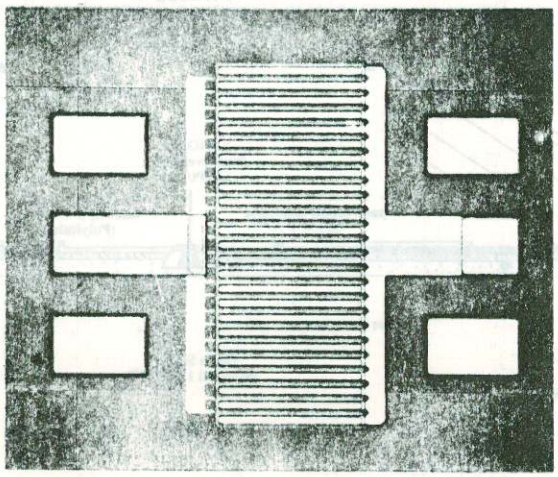


Figure 4: ***Photomicrograph of the 24x300µm interdigitated PSVD***

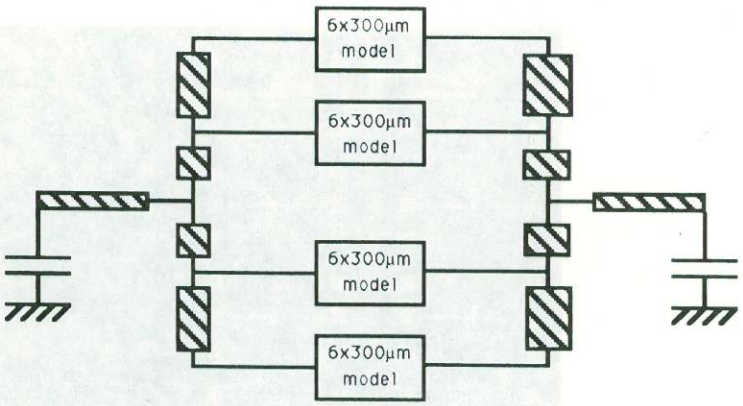


Figure 5: ***Model for the 24x300µm PSVD***

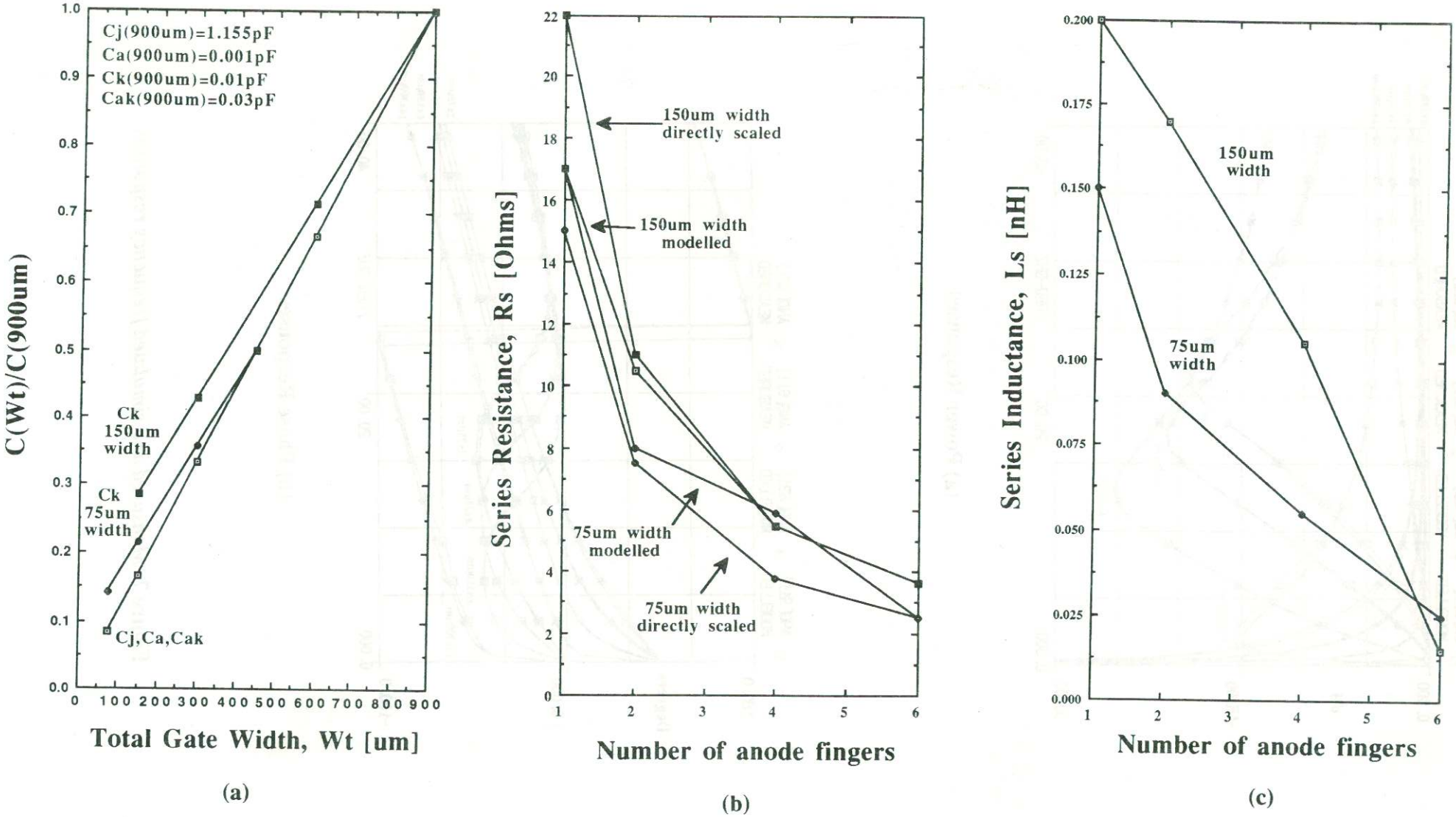
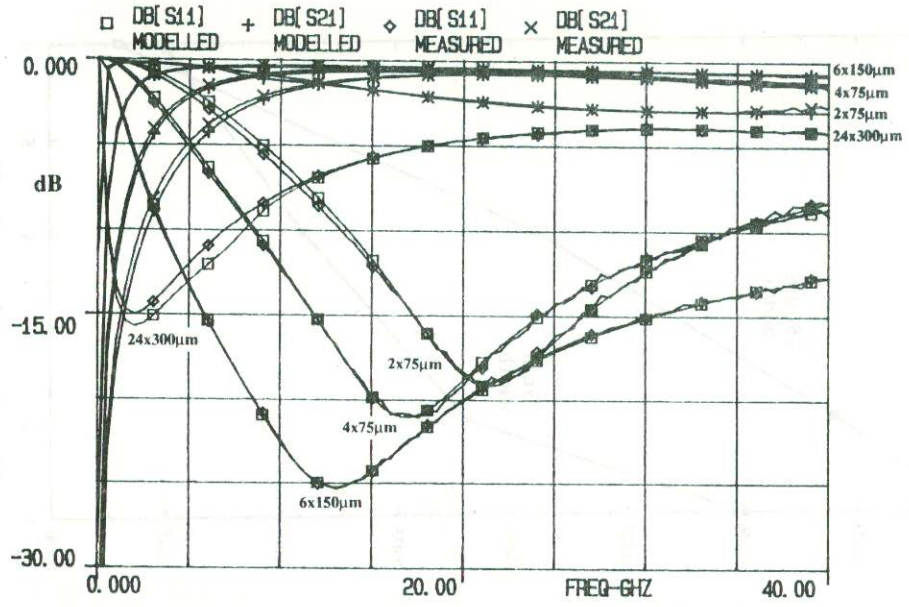
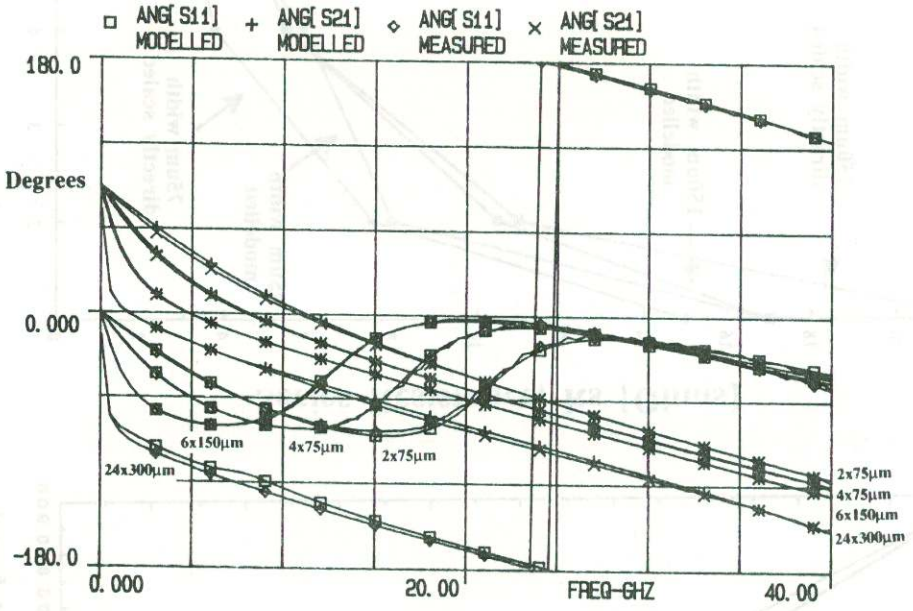


Figure 6: ***Scaled and modelled element values***



(a) Power Responses



(b) Phase Responses

Figure 7: ***Measured and simulated frequency responses***