BIAS CONDITIONS FOR ACCURATE PARASITICS EVALUATION OF MICROWAVE MESFETs UP TO MM-WAVE FREQUENCIES

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ABSTRACT

The correct conditions for the accurate evaluation of parasitic elements in microwave and millimetre-wave MESFETs from measurements are described. The elements are evaluated directly without any "fitting" procedure, and prove to be bias-independent and constant up to mm-wave frequencies. The intrinsic elements can then be accurately evaluated, and a bias-dependent, non-linear model established.

KEYWORDS: Modelling, MESFETs, Equivalent circuit

INTRODUCTION

The accurate evaluation of the parasitic elements of microwave and millimetre-wave MESFETs is a foundamental step in the extraction of a wide-band, accurate equivalent circuit from measurements (Fig.1), for use in linear or non-linear CAD programmes. The preliminary determination of parasitics allows a simple and straightforward evaluation of the intrinsic elements to be performed at low frequency (Ref.1); the results are however valid up to the upper frequency-band limits for the transistor. If the intrinsics evaluation is repeated at each bias point, either a bias-dependent linear or a non-linear equivalent circuit can easily be constructed.

The parasitic elements can be identified from low-frequency measurements by suitably choosing the bias conditions, avoiding lengthy and uncertain "fitting" procedures from wide-band measurements. Many procedures have been given so far (Refs.1-4): their validity has been tested and an improvement suggested. The resulting method has been applied to microwave and millimetre-wave MESFETs and found to give good results up to 50 GHz. Resistive, inductive and capacitive parasitics are separately dealth with in the following.

RESISTIVE PARASITICS

The elements to be evaluated are gate, source and drain resistances. When the gate junction is forward-biased ($V_g > 0, \quad I_g > 0, \quad V_d = 0$), additional resistive elements in the MESFET are the junction and channel resistances (Fig.2). The incremental input resistance if the drain is left open can be expressed as (Ref.3):

$$\frac{\Delta V_g}{\Delta I_g} = R_g + \frac{nV_T}{I_g} + \frac{R_{ch}}{3} + R_s$$

if the limit for Ig $\rightarrow \infty$ is taken (or for $\frac{1}{I_g} \rightarrow 0$, Fig.3), the contribution from the junction resistance vanishes and eqn. (1) in Table I is obtained. In case the source is left open, eqn. (2) is obtained. The coefficient 1/3 of the channel resistance comes from its distributed nature.
The incremental trans-resistance if the drain is left open can be expressed as (Ref.3):

$$\frac{\Delta V_d}{\Delta I_g} = R_s + \frac{R_{ch}}{2} - \frac{R_{ch}^2}{nV_T} I_g$$

the limit for $I_g \rightarrow 0$ yields eqn. (3) in Table I, or (5) if the source is left open. The slope of the plot vs Ig (Fig.4) yields Rch (eqns. (4) and (6) in Table I).
If the gate junction is reverse-biased ($V_g < 0, \quad V_d = 0$), the MESFET can be represented as in Fig.5. If we assume the channel to be uniformly doped, the drain-to-source resistance can be expressed as (Ref.4):

$$\frac{V_d}{I_d} = R_d + \frac{R_{ch}}{1\sqrt{\frac{-V_g+V_{bi}}{V_{po}+V_{bi}}}} + R_s = R_d + R_{ch} \cdot x + R_s$$

the limit for $x \rightarrow 0$ (Fig.7), i.e. channel infinitely wide, yields eqn.(7) in Table I; the slope of the plot vs x yields eqn.(8). The set of 8 equations in 4 unknowns is over-determined; not all of them however are reliable. In particular, eqns. (4), (6) and (8) appear to be affected by unacceptable measurement error. Of the remaining 5 equations, eqns.(1)(2)(3) and (5) are not independent, and cannot be taken as a valid sub-set; the others give consistent results for gate, source and drain resistances whatever sub-set of 4 eqns is taken (Table II). They are therefore assumed as a base for resistance evaluation.
Similar data can be obtained from RF measurements with a Network Analyser, as the low-frequency limit of the real part of the impedance matrix (computed from the S-matrix); however, only eqns. (1), (3) and (7) are available if the source of the MESFET is RF- grounded. The results are equivalent to those from the DC measurements, with a somewhat lesser accuracy.

INDUCTIVE PARASITICS

The inductances are evaluated with the gate junction forward-biased ($V_g > 0, \quad I_g > 0, \quad V_d = 0$) (see again Fig.8, shunt capacitances neglected at low frequency), as the slope of the imaginary part of the impedance matrix elements vs frequency (Ref.1). The measurement is affected by residual gate-junction capacitance, whose equivalent inductive contribution can be expressed as:

$$L_{j,equiv} = -\frac{\omega C_j R_j^2}{1+(\omega C_j R_j)^2} \sim \frac{1}{I_g^2}$$

for large gate currents. Therefore the actual parasitic inductances are evaluated in the limit for $I_g \rightarrow \infty$ (or $\frac{1}{I_g^2} \rightarrow 0$, Fig. 7).

CAPACITIVE PARASITICS

The capacitive parasitics are usually evaluated with the channel totally depleted as the slope of the imaginary part of the admittance matrix elements vs frequency (Fig.8, after removing the series inductances, already known from the previous step). The condition adopted, i.e. $Vgs \quad << \quad V_{pinch-off}$, is however not satisfactory, because the residual substrate capacitance between gate and source or drain is not dependent on bias voltage, and therefore does not vanish for

$V_{gs} \rightarrow -\infty$. These five capacitances (C_{pgs}, C_{pgd}, C_{pds}, C_{gs}, C_{gd}) cannot be determined from the three independent matrix elements unless the hypotheses of $C_{pgd} = 0$ and $C_{gs} = C_{gd}$ are accepted (Ref.1). These hypotheses can be removed if the evaluation is done at near-open-channel conditions ($V_{gs} \sim 0$, $V_{ds} = 0$, see again Fig.5) where the substrate capacitance is shunted by the low channel resistance, and channel capacitances can be expressed as:

$$C_{gs} = \frac{C_{gso}}{1\sqrt{\frac{-V_g + V_{bi}}{V_{po} + V_{bi}}}} = C_{gso} \cdot x \qquad , \qquad C_{gd} = C_{gdo} \cdot x$$

the limit for $x \rightarrow 0$, i.e. $V_{gs} \rightarrow -\infty$ now gives $C_{gs} = C_{gd} = 0$, and the three parasitic capacitances are correctly found (Fig.9).

RESULTS

The present procedure for parasitics evaluation has been applied to the extraction of the equivalent circuit of millimetre-wave MESFETs. Once the parasitics are found and subtracted from the measured data, the intrinsic elements are computed from the intrinsic admittance matrix as the elements of a pi-network at low frequency (Ref.5). Results are shown in Figs.10-12 for a $0.3\mu m$ Siemens MESFET up to 50 GHz for a low-noise bias point (S-parameters, measured and modelled); measurements have been performed with on-wafer probes and SOLT calibration by T. Sporkmann at ArguMens (Duisburg) within the ESPRIT 5018 COSMIC project. In Fig.13 S-parameters at two different bias point are shown, with the parasitics kept constant and different intrinsics: the agreement is excellent, illustrating the correct separation of bias-dependent and bias-independent parameters. In Fig.14 the bias-dependence of the intrinsic gate- source capacitance is shown, illustrating the possibility of constructing an accurate bias-dependent linear model, or an accurate non-linear model.

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Input resistance (source grounded)	Rg + Rs + Rch = 2.834 Ohm	(1)
(drain grounded)	Rg + Rd + Rch = 2.938 Ohm	(2)
Trans-resistance (source grounded)	Rs + Rch/2 = 2.258 Ohm	(3)
	Rch = 0.420 Ohm	(4)
(drain grounded)	Rd + Rch/2 = 2.245 Ohm	(5)
	Rch = 0.389 Ohm	(6)
Output resistance	Rs + Rd = 3.489 Ohm	(7)
	Rch = 0.314 Ohm	(8)

Table I - Measured values for resistive parasitics

Equations	Rg	Rs	Rd	Rch
1 + 2 + 3 + 7	0.944	1.693	1.796	0.596
2 + 3 + 5 + 7	1.032	1.752	1.737	0.508
1 + 2 + 5 + 7	0.843	1.692	1.796	0.898
1 + 3 + 5 + 7	0.945	1.751	1.798	0.815

Table II - Valid sub-sets of equations for resistance computation

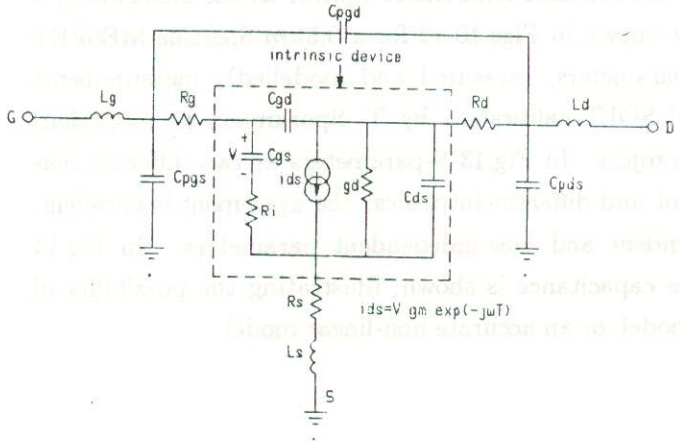

Fig.1 - The complete equivalent circuit

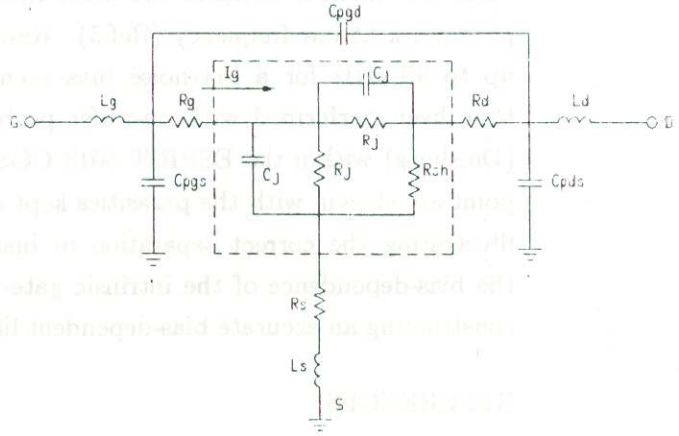

Fig.2 - The equivalent circuit with gate junction forward-biased

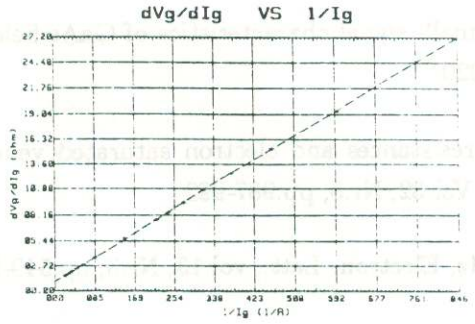

Fig.3 - Input resistance determination

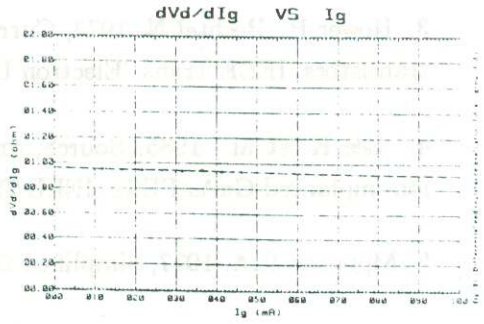

Fig.4 - Trans-resistance determination

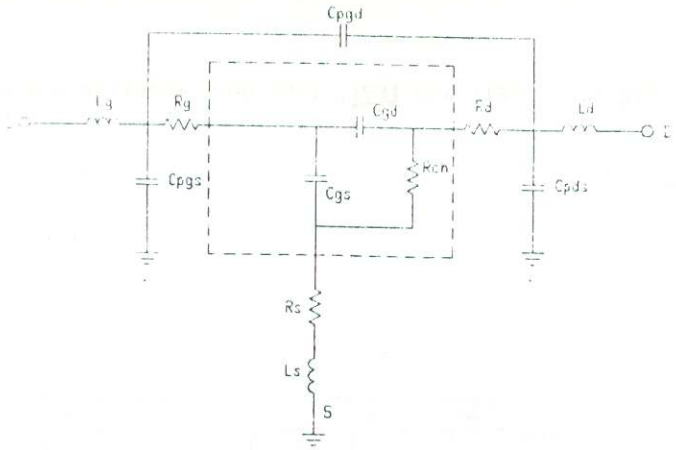

Fig.5 - The equivalent circuit with gate junction reverse-biased

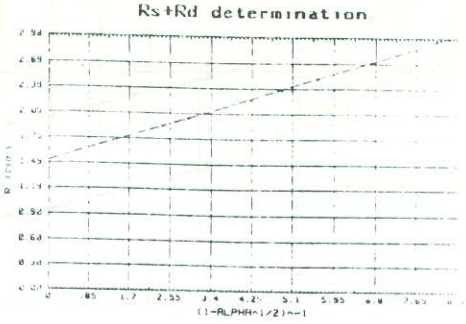

Fig.6 - Output resistance determination

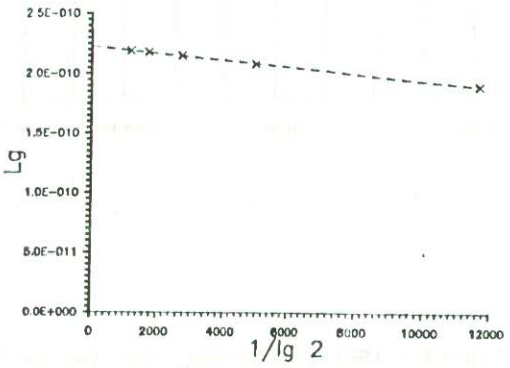

Fig.7 - Inductance determination

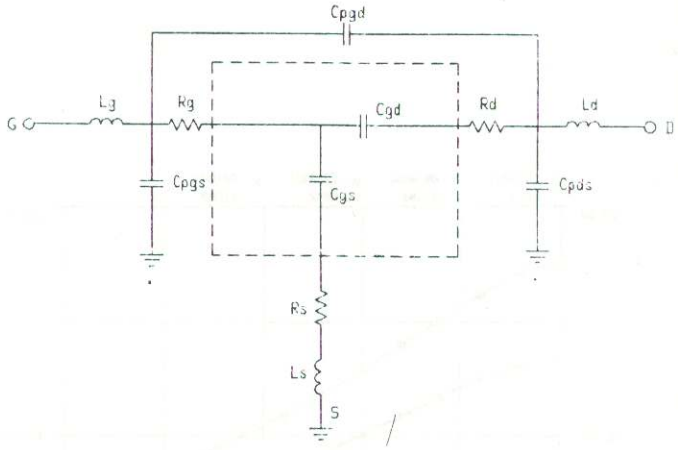

Fig.8 - The equivalent circuit with totally depleted channel

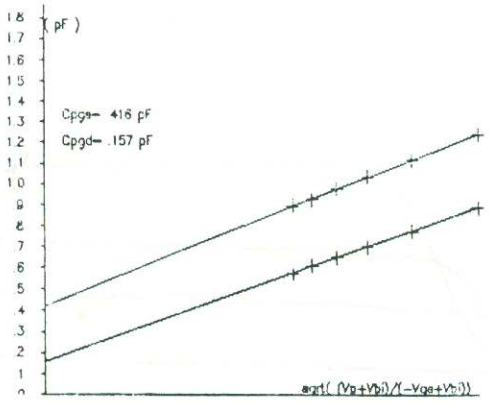

Fig.9 - Capacitance determination

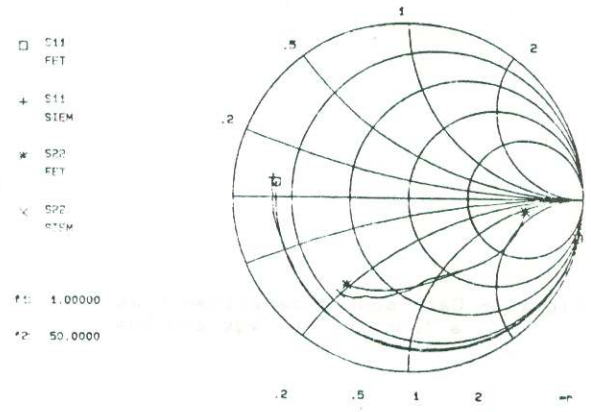

Fig.10 - S11 and S22, 1-50 GHz, modelled and measured

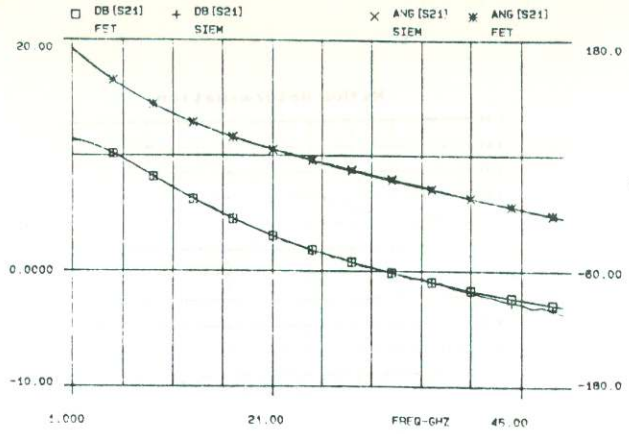

Fig.11 - |S21| and ∠S21, 1-50 GHz, modelled and measured

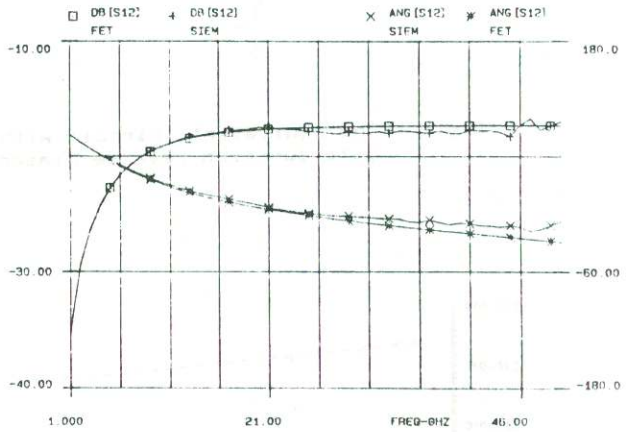

Fig.12 - |S12| and ∠S12, 1-50 GHz, modelled and measured

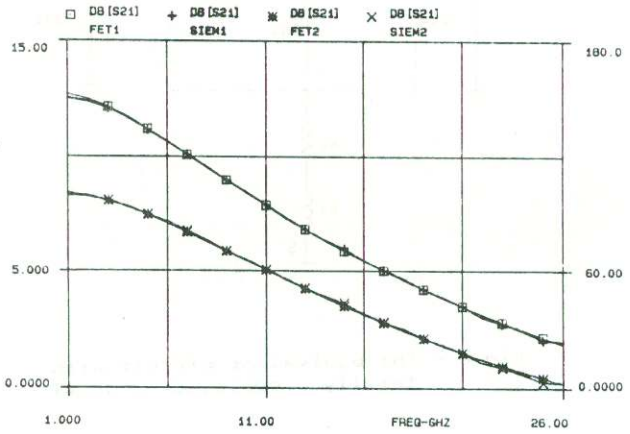

Fig.13 - |S21|, 1-50 GHz, for two different bias points, modelled and measured

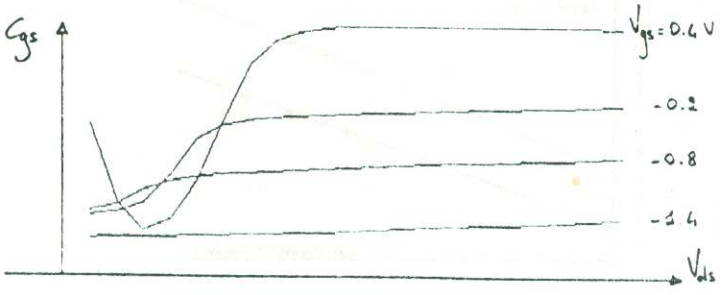

Fig.14 - Gate-source capacitance as a function of Vgs and Vds