FLIGHT MODEL Ga As MMIC PROCUREMENT : INDUSTRIAL CONCERNS

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ABSTRACT

The Gallium Arsenide Monolithic Microwave Integrated Circuits Technology (MMIC) is now mandatory for competitiveness in space business. ALCATEL ESPACE has to face the challenge of providing Flight Model MMIC based equipments by end of 1993. This paper will present how a practical MMIC Qualification program is presently being implemented. The used method consists to procure from a mature enough foundry large size wafers in order to merge foundry qualification and dice flight model procurement into the same operation.

Keywords : GaAs MMIC for Space Application, Foundry Qualification, Flight Model Procurement, LAT, WAT.

1 INTRODUCTION

Today qualification programs are being conducted for Ga As MMIC foundry as well as in Europe or in USA, however none foundry is qualified yet. The proposed paper will aim to describe the Qualification Program ALCATEL ESPACE is conducting with an US foundry for the procurement of "Class S" Ga As MMIC dice. This program is based upon :

- French Agencies Technical Note : a Methodology for the Space Qualification of GaAs MMICs [1],
- ESA Technical Discussion Document : requirements for capability Approval of GaAs MMICs [2].

The considered approach is mainly based on reliability efforts conducted all long of the manufacturing flow, and reliability tests conducted by the user at the end of the fabrication. Reliability tests are composed of two phases :

Phase 1 - Reliability verification on TCVs,
Phase 2 - Characterization of reliability domain on DECs and quality verification on MMIC products.

2 EVALUATION/QUALIFICATION STRATEGY

Due to the fact that future applications (SAR) will require rather large quantities of MMIC (several runs for the same circuit) "Lot Qualification" concept was no longer valid. Consequently ALCATEL ESPACE is today in accordance with Process Line Qualification concept as defined by US, ESA, and French Agencies. A possibility to conduct, in a cost and schedule efficient way, a Process Line Qualification program is to use large size wafers ($\geq$ 3" diameter) in order to associate MMIC qualification and flight model procurement into the same program (MMIC die quantities being sufficient to satisfy both needs). Of course the risk involved must be minimized by selecting a mature enough foundry which has the capability to carry on this program with good chance of success. Further more the packaging and assembly process have to be taken into account for the conduction of this program.

3 FOUNDRY SELECTION

To procure circuits required for the design of competitive MMIC based space equipments, ALCATEL ESPACE decided to select a foundry with a "pre-evaluated" process. MMIC layout is performed with the associated design manual and design tools recognized as reliable by MMIC users community. The following criteria were used :

- balance of the foundry process to the ALCATEL ESPACE application ;
- wafer fabrication performed by an "under control" automated process with evidence of daily SPC charts and trend analysis showing good process stability ;
- perfect knowledge of the reliability limits of the main elements of the foundry cell library (reliability domain well defined : Ea, MTTF for every failure mechanism) [3, 4, 5].

Once this demonstrated, an audit was conducted by ALCATEL ESPACE to the foundry plant in order to consolidate the given informations. This audit was based upon ISO 9001 specification and French Administration questionnaire [1].

4 DESCRIPTION OF ALCATEL ESPACE APPLICATION

The purpose of this foundry run is to develop all the necessary MMICs to realize a Ku-Band channel amplifier. Those circuits are : Low Level Amplifiers, Analog Attenuators, Flatness Correctors.

Low Level Amplifier : This amplifier will be used as well at the input as at the output of the RF chain. The consequences are that this circuit has to present good noise and good linearity performances. It is based on a three feedback stages topology and makes use of 300 μm FETs (Lg = 0.5 μm). The expected performances are a gain equal to 17 dB, VSWR < 1.2, NF > 5 dB, IMP3 > 22 dBm, the power comsumption is lower than 100 mW. The chip size is 2.6 x 1.6 mm2.

Analog Attenuator : This attenuator makes use of a Lange coupler loaded with cold FETs (Vds = O V). The command voltage of the attenuator is applied on the gates of the FETs in order to modify the Lange coupler load impedances. Several Ku-Band reflective attenuators have been already successfully developed by ALCATEL ESPACE and typical performances are : Dynamic > 24 dB, minimum insertion losses < 1.5 dB, VSWR < 1.2. Due to the use of cold FETs, the power consumption of this type of attenuator is equal to 0 mW. The chip size is 2.5 x 1.6 mm2.

Flatness Corrector : The RF chain of the channel amplifier is composed of several cascaded amplifiers and attenuators. In order to correct a possible gain slope within the frequency bandwidth (2 GHz), a flatness corrector is inserted into the RF chain. This circuit is also built around a Lange coupler. Each two branches of the coupler are loaded with coupled lines. One of them is terminated by two cold FETs in order to modify the frequency response of the coupled lines. The voltage controls are applied on the gates of the cold FETs. By a correct combination of those control voltages, different response shapes can be achieved : Slope on the right (to correct slope on the left), slope on the left, valley, hill. The corrective dynamic of each shape type is higher than 3 dB. The size of this circuit is 3 x 1.6 mm2.

Taking into account the number of circuit of each type needed to realize a channel amplifier in accordance with the qualification requirements, the tile presented on figure 3 has been implemented. These circuits are currently being processed on 100 mm GaAs semi-insultating substrate at TRIQUINT Semiconductors foundry (USA).

5 MMIC FOUNDRY PROCESS AND CIRCUIT QUALIFICATION (first run)

To face the challenge of providing flight models equipment by end of 1993 ALCATEL ESPACE is presently implementing the Qualification program summarized in figure 1. The selected foundry was estimated to meet the criteria required to have the "pre evaluated" status. The following task is being conducted :

- "Class S" die procurement.
- Phase 1 Reliability verification on TCV.
- Phase 2 Reliability verification on DEC and MMIC.

5.1 "Class S" die procurement

The following quality assurance informations are given for every wafer :

- Certificate of conformance (material traceability),
- SPC data of this particular production RUN,
- Metallization and glassivation thicknesses,
- SEM on typical patterns,
- Visual inspection results (reject ratio),
- PCM wafer probe data results (100 %),
- Metallization adherence test results (bond pull/die shear),
- MMIC RF wafer probe data results "S" parameters (for information only) with complete traceability including.

At the end of the wafer processing a Wafer Acceptance Review is conducted by ALCATEL ESPACE at the foundry plant to give authorization for delivery. It consists of :

- PCM electrical results and yield analysis,
- 100 % die sort visual inspection and 2.5 % AQL sampling customer source
- inspection,

  Data package review (SEM, die shear and bond pull test results).

PCM electrical parameter distribution is analyzed for every wafer in order to consider (or not) wafers processed in the same batch as a single wafer lot production. Upon reception of dice at ALCATEL ESPACE the Qualification phases will start as follow.

The purpose of phase 2/1 is to characterize the reliability domain for the same type of custom designed MMIC. Failure criteria will be based on RF drift (- 1 dB on gain) and power consumption (+ 10 % on current). A total quantity of 2 x 20 DEC will be assembled into microwave microstrip packages and submitted to accelerated life testing for 4000 hours (or 50 % cumulated failures) at two channel temperatures (200 and 225° C). These hybrid devices are suitable for log normal analysis used to determine the Mean Time To Failure and Activation Energies associated to failure mechanism. A DEC thermal analysis will also be used throughout the phase 2-1. All calculations will be based on the peak hot spot temperature of the hottest FET on the surface of the DEC.

5.2 Phase 1 - Reliability verification

This verification is conducted on 40 TCV (Technological Characterization Vehicle) assembled by ALCATEL ESPACE into dual in line ceramic packages. Once assembly operations completed, devices are sent back to the foundry for reliability tests conduction. The objective of this phase is to verify the intrinsic reliability and reproducibility of the elementary cells used for the design of the MMIC. To satisfy this purpose two files of 20 TCV devices each are submitted to life testing for 4000 hours (or 50 % cumulated failures) at two channel temperatures (200 and 225°C). The foundry accepted to conduct this program based upon the fact that elementary cells are well known and previously characterized. Part of this program includes thermal analysis on every element comprising the TCV in order to determine the actual acceleration factor. Electrical stress conditions are defined in order to cover the largest possible region allowed by the Design Manual (maximum current densities and voltages). Failure criteria are based on DC drift parameters (10 % IDSS, 10 % Vp, 10 % V_{BR}, ...). It has to be understood that this phase 1 is a verification test ; it takes into account the process evolution (validated by Technological Review Board), whose main failure mechanisms have been well identified and characterized by the manufacturer [6]. Phase 1 will confirm and verify these mechanisms at lower channel temperatures (200 and 225° C).

5.3 Phase 2 - Reliability verification on DEC and MMIC

5.3.1 Phase 2/1 - Qualification tests on DEC

This characterization is conducted on Dynamic Evaluation Circuit (DEC) identified as Low Level Amplifier as described in paragraph 4. The choice was based on MIL-I-38535 requirements regarding the Standard Evaluation Circuits (SEC) :

a) It shall exercise the functionality of the process technology, and be of a representative complexity of MMIC to be supplied, and be comprised of major circuit element types ;
b) It shall be a fully functional circuit capable of being tested and screened as if it were an MMIC ;
c) It must exercise all the worst-case electrical and geometrical design rules, and provide for simple failure diagnosis.

A single transistor was previously choosed as "DEC". Meanwhile, the foundry proposed to use the ALCATEL ESPACE - LLA as "Standard Evaluation Circuit" (SEC) for the conduction of its own QML certification under MIMIC phase III program. In order to correlate data and to be more in accordance with the today concept, ALCATEL ESPACE decided to use the LLA as DEC.

The purpose of phase 2/1 is to characterize with RF measurements the reliability domain for the same kind of custom designed MMICs. Failure criteria will be based on RF drift (- 1 dB on gain) and power consumption (+ 10 % on current). A total quantity of 2 x 20 DEC will be assembled into microwave microstrip packages and submitted to accelerated life testing for 4000 hours (or 50 % cumulated failures) at two channel temperatures (200 and 225° C). These hybrid devices are suitable for log normal analysis to determine the Mean Time To Failure and Activation Energy associated to failure mechanism. A DEC thermal analysis will also be used throughout the phase 2-1. All calculations will be based on the peak hot spot temperature of the hottest FET on the surface of the DEC.

5.3.2 Phase 2.2 Reliability verification on MMICs

The purpose of phase 2.2 is to verify the MTTF of the other circuits installed on the reticule. A total of 10 circuits of each type will be assembled individually into the same generic package as for the DEC, and submitted to high temperature accelerated life test (200° C channel temperature) during 4000 hours (or 50 % cumulated failures). As defined for the DEC the same RF failure criteria will be used and failure analysis will be performed the confirm failure mechanisms.

5.4 Qualification status

At the end of phase 2.2, taking into account that the reliability was fully demonstrated and verified by phase 1 and 2.1. The quality of the MMICs, object of the procurement, can be considered as qualified as well as the foundry process used.

6 FLIGHT MODEL MMIC PROCUREMENT (second run)

For any other procurement to be performed from this "Qualified process/foundry" the ALCATEL ESPACE approach is summarized by figure 2; such a procurement occurs for three possible reasons :

a) Additional circuits required,
b) Correction or design improvement on circuit(s),
c) Procurement of new designed circuit (within the capability domain).

In that case wafer acceptance test includes the same requirements as for the first run but an accelerated life test on 10 TCV (168 hours at 200° C channel temperature) is required to verify the reproducibility of the reliability. The acceptance of this wafer acceptance test (WAT) is conditional for the dice delivery (accept : 0; reject : 1). Upon reception of the MMICs, ALCATEL ESPACE will conduct a lot acceptance test (LAT) in the same way as for phase 2.
Lot acceptance test sequence is as follow :

- Assembly of 10 DEC with the addition of 4 x MMICs of each type,
- Screening : 96 hours burn-in at 150°C
- Accelerated life test : 240 hours life test at 225°C
  criteria (accept (0), reject (1)).

7 CONCLUSION

ALCATEL ESPACE is definitely engaged in a "Class S" MMIC dice procurement. The implemented strategy is the result of permanent negotiation and trade off. This kind of program could be reconducted with European Space Agencies agreement for the next coming foundry qualifications for dice procurement.

8 REFERENCES

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9 FIGURES

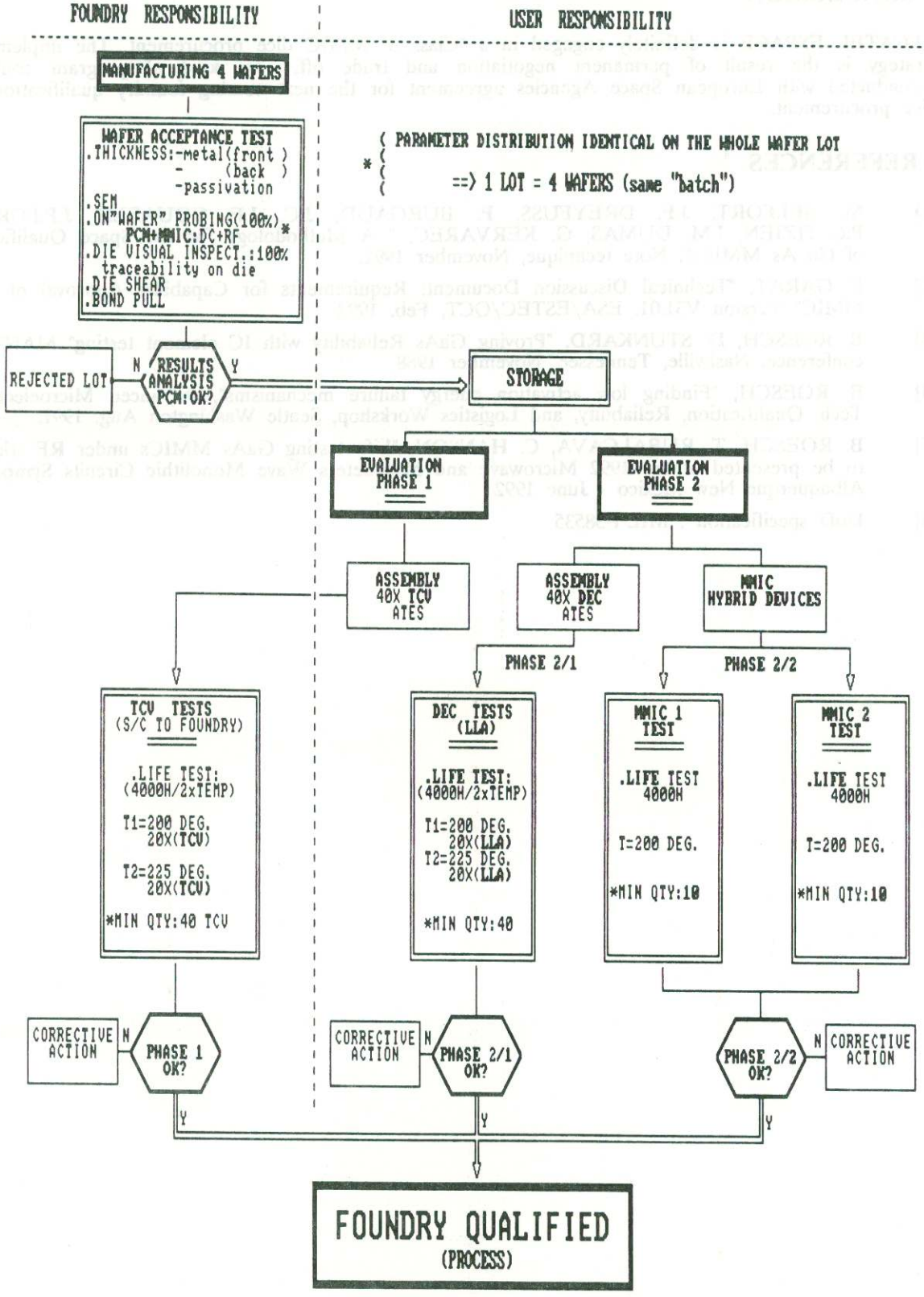

FIGURE 1 : MMIC DIE QUALIFICATION AND PROCUREMENT PLAN FIRST RUN

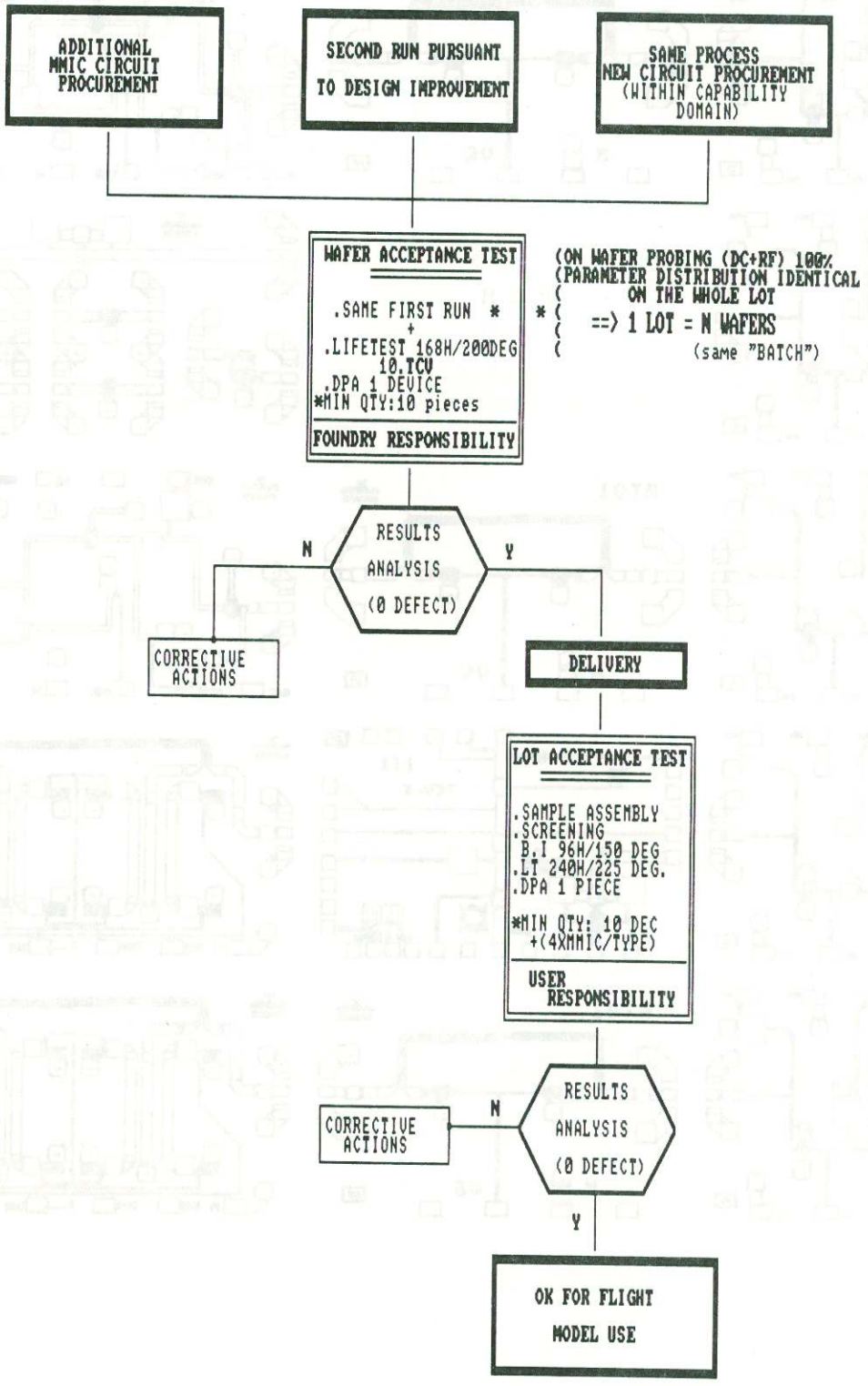

FIGURE 2 : MMIC DIE QUALIFICATION AND PROCUREMENT PLAN
SECOND RUN

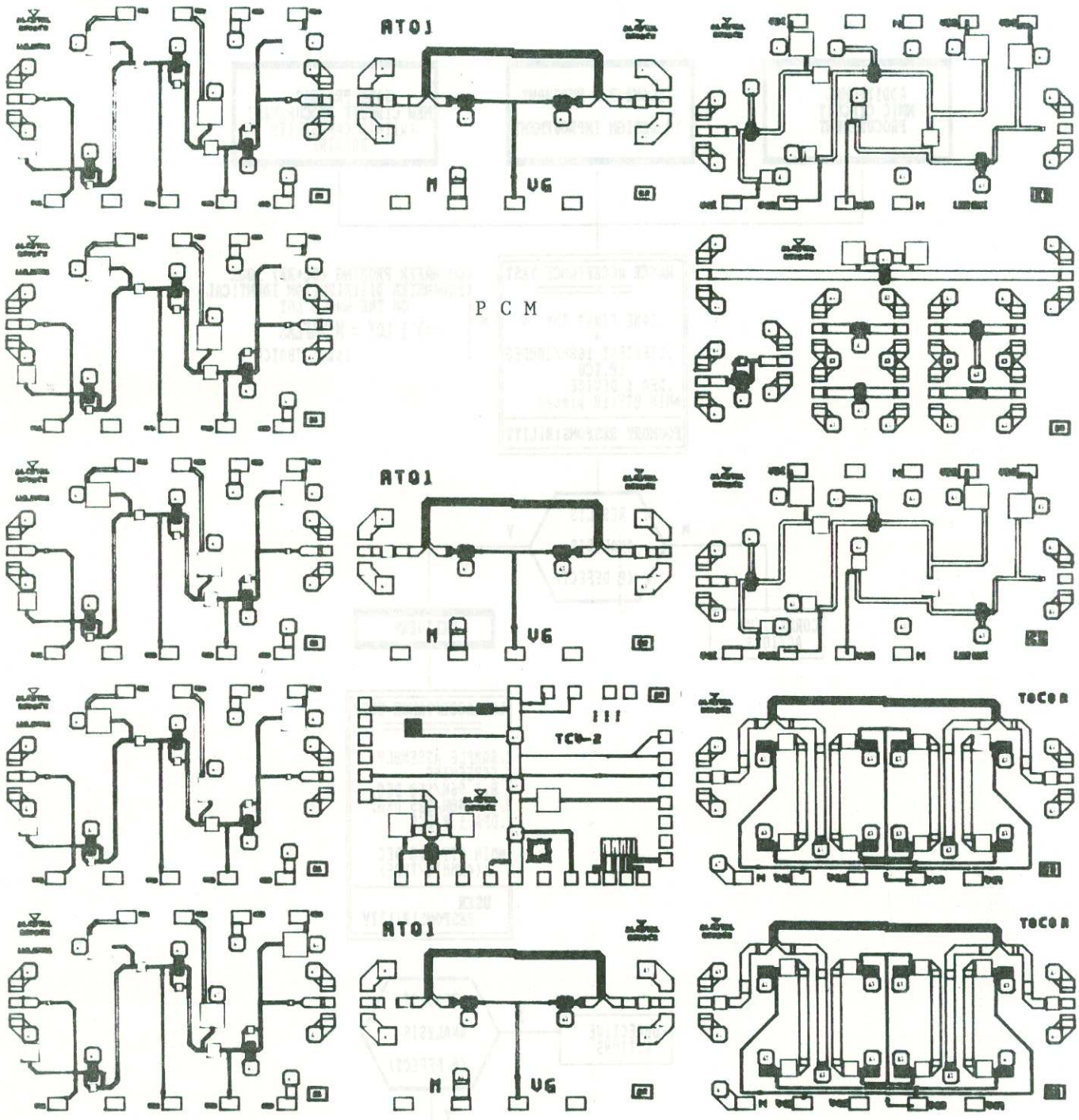

FIGURE 3 : TILE LAYOUT