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MONOLITHIC FIVE-BIT PHASE SHIFTER FOR ARTEMIS SPACE APPLICATION

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ABSTRACT

A five-bit MMIC switched filter phase shifter has been successfully designed, produced and characterised for application in 2.2 - 2.3 GHz inter-orbital communications. This paper demonstrates the consistency of chip to chip performance achievable on a well controlled MMIC process. This is a particularly important aspect in phased array applications where a large number of chips are utilised in a single system.

Keywords: MMIC, Phase Shifter, S-band, Switched Filter

1. INTRODUCTION

This paper presents results from the first design iteration of a five bit switched bit phase shifter. The circuit has been designed as part of the receive phased array antenna for the Artemis experimental communications satellite. Its performance parameters track particularly closely over the complete sample of RF functional chips. The chips exhibit good VSWR and low insertion loss with minimal variation between states. Key parameters have been measured over the -10°C to 50°C temperature range. The paper describes the excellent performance and temperature stability that has made GaAs MMICs the most popular medium for the realisation of switched filter phase shifters.

2. MMIC DESIGN AND FABRICATION

Switched filter phase shifters have been widely reported since the early 1970's (1). Each component circuit achieves differential phase shift by switching between high pass and low pass filter configurations using MESFET switching elements. The phase shifter uses the common binary bit-weighting implementation to cover a 360° range in 32 steps of 11.25°. This is achieved by the cascading of five component circuits with differential phase shifts of 180°, 90°, 45°, 22.5° and 11.25°. Every component circuit has the optimum topology to achieve the required phase shift while maintaining a good VSWR and minimal insertion loss variation between states. The 45° component uses two SPDT switches to route between a π low pass filter or a T high pass. Reconfigurable filters were found to produce better solutions for the other component stages. These circuits utilise the 'off' state parasitics of the MESFETs as filter components. This design technique requires fewer FETs than the SPDT switched filter and is more tolerant to FET processing variations. Each stage is controlled by complementary 0V and -7V control lines.

The five component circuits were ordered to produce optimum VSWR and phase shift error when terminated in a 50Ω impedance. A complete circuit diagram is given in Figure 1. Individual bits and the complete phase shifter were simulated using commercial CAD software. Process specific scalable models have previously been developed for each circuit element (2) (3) and were used throughout.

The circuits were fabricated at GEC-Marconi Materials Technology using the standard Foundry (3) process which is currently undergoing ESA capability approval. A chip photograph is given in Figure 2. The switch MESFETs have 0.7µm gate length and are silicon doped with a carbon compensation implant. Integrated 4kΩ mesa resistors provide isolation between the control logic and the gates. The complete circuit has a total gate width of 18.9mm in order to produce a low insertion loss.

3. MEASURED RESULTS

Each fabricated chip was tested RF on wafer using a computer controlled Hewlett Packard 8510 network analyser. In-house software controlled D.C. switching, data storage and analysis. A dedicated test jig was used for temperature cycling and power measurements. The low pass configuration was taken as the 0° reference state. Table 1 summarises the typical phase shifter performance.

Table 1. Typical Phase Shifter Performance (21°C)

Frequency	2.2 - 2.3GHz
Phase Shift	5-bit
VSWR	<1.55:1
Phase shift error (i)	7°rms
Insertion Loss	4.9dB
Insertion Loss variation (ii)	±0.5dB (0.21dBrms)
Group delay variation (ii)	±0.1ns
1dB compression point	26dBm
D.C. control voltage	0V and -7V complementary
Chip size	5.9mm x 2.9mm x 0.2mm

note (i) over all phase states
note (ii) over all phase states and across frequency band

The presented results are from a first pass design and compare very favourably with similar previously reported circuits, (4) (5). The mean VSWR at input and output ports was measured at 1.2:1 with several states producing values around the worst case of 1.55:1. Although 7° r.m.s. phase error is reasonable for a first pass design a second iteration is currently being fabricated to improve this value to less than 3° rms. Figure 3 shows that the MMICs exhibit good coverage of the phase shift range in all 32 states over the 2.0 - 2.5GHz band.

The circuit's sensitivity to gate bias level was checked by varying the gate voltage by ±2V about the -7V off state and no measurable phase shift or insertion loss change was observed. A typical R.F. to D.C. isolation of 40dB was measured on each of the control lines. The circuits insertion loss increases by 1dB at an input power of 26dBm.

3.1. STATISTICAL SPREAD

A very coarse screening test was applied to the complete set of RF on wafer measurements. 50% of the fabricated chips were classed as RF passes. The data from all these chips is presented in Tables 2 and 3. In practice a smaller sample of chips was required for delivery. These were selected using more stringent screening parameters producing an even tighter distribution of performance.

Table 2. Statistical spread of phase shift from 50% of fabricated chips

Nominal phase shift (deg)	Standard Deviation	Variation coefficient (S.D./Mean)x100
11.25	0.22	1.74
22.5	0.23	1.00
45	0.36	0.74
90	0.63	0.74
180	1.31	0.78

Table 3. Statistical spread of insertion loss from 50% of fabricated chips

Circuit state	Standard Deviation	Variation coefficient (S.D./Mean)x100
low pass configuration	0.10	2.24
high pass configuration	0.17	3.29

Table 2 shows the phase shift standard deviation over the complete sample of RF passes for the five primary phase states. It demonstrates the excellent chip to chip reproduction available from a well controlled foundry process. The high pass configuration produces a phase shift which is dependent upon variations from each component circuit. Figure 4 shows that in this worst case the complete sample of chips lie within ±5° and 91% are within ±3° of the mean.

Table 3 shows the standard deviation of the insertion loss for the high pass and low pass states. These two configurations encompass both states of each component circuit. For the high pass state 93% of the chips lie within ±0.3dB of the mean.

3.2. TEMPERATURE MEASUREMENTS

One of the advantages of switched filter MMIC phase shifters over rival techniques is that they exhibit a high degree of insertion loss and phase shift stability over temperature. Insertion loss and phase shift were recorded at -10°C, 10°C, 30°C and 50°C. Table 4 gives the gradient of phase shift variation with temperature for the five primary phase states and high pass configuration.

Table 4 phase shift variation with temperature

Nominal phase shift	11.25°	22.5°	45°	90°	180°	348.75°
Phase shift change $(x10^{-3})$/°C	2.0	0.5	-1.0	6.0	7.0	14.0

Since the low pass state is taken as the phase shift reference the high pass state reflects the temperature variation of every circuit element. Even in this worst case the phase shift varies by only 0.87° across the 60°C range. Each of the measured states shows a $-5x10^{-3}$dB/°C insertion loss variation.

4. SUMMARY

The measurements show good performance for a first iteration five-bit phase shifter. The statistical analysis demonstrates closely reproducible results over a large sample of chips. Performance parameters are highly independent of temperature. These results demonstrate some of the advantages of this approach to phase shifter implementation.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

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Figure 1.Phase shifter circuit diagram.

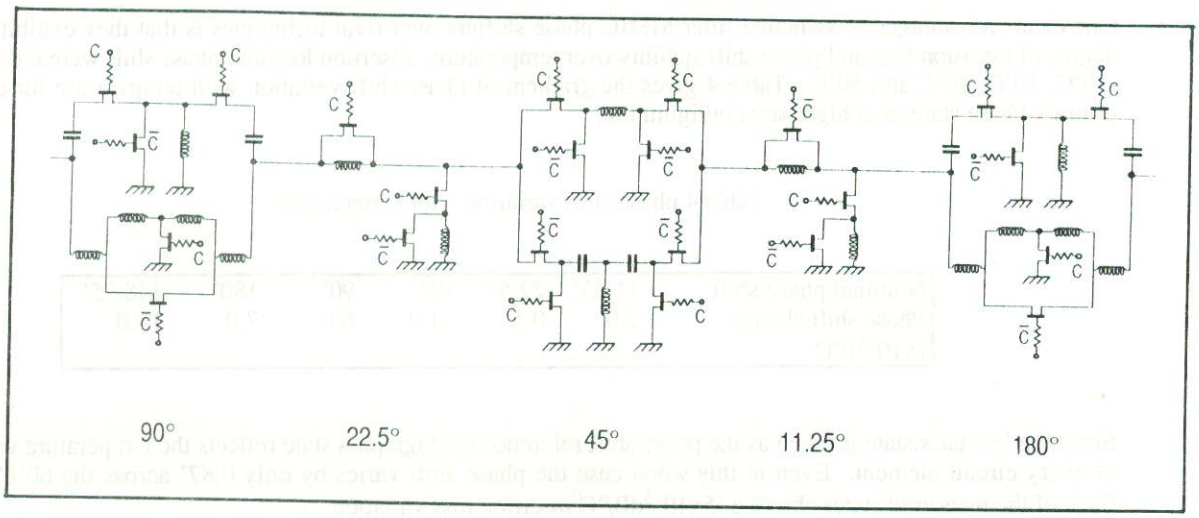

Figure 2.Chip photograph.

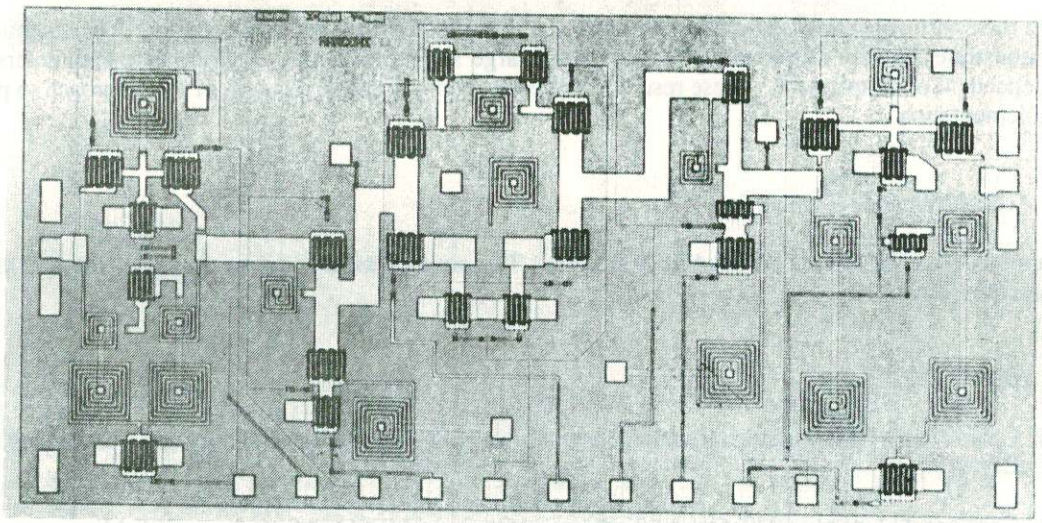

Figure 3.Phase shift in all 32 states.

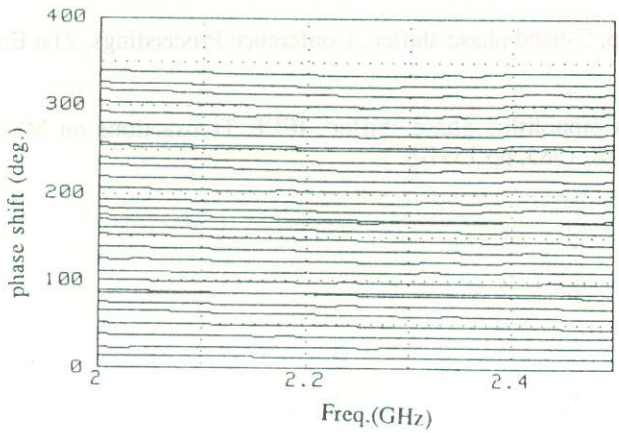

Figure 4.Distribution of phase shift in high pass configuration.