SMALL SIZED HIGH-GAIN PHEMT HIGH-POWER AMPLIFIERS FOR X-BAND APPLICATIONS

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ABSTRACT

The development of two small sized broadband X-band high-power amplifiers is discussed. The amplifiers are realised with the help of the pseudomorphic HEMT technology of the Fraunhofer Institute for Applied Solid State Physics (FhG-IAF). With the help of this technology the feasibility of integrating a driver and high-power amplifier on a single, small sized, chip is demonstrated. This integration will reduce the number of chips necessary in a Transmit/Receive (T/R) module used in e.g. a phased-array radar antenna. Consequently, the cost of a T/R module is reduced.

INTRODUCTION

Component cost is of vital importance for the successful development of Transmit/Receive (T/R) modules for phased-array radar applications. A way to realise cost reduction is the integration of several functions on one chip. The block diagram of the T/R module, which is currently being developed by TNO-FEL, is depicted in figure 1. The steering of the antenna beam and the switching between the receive and transmit mode is realised with help of one multifunction chip. The design and measurement results of this chip are described in [1]. Another goal of TNO-FEL is the integration of the driver and high-power amplifier on a single chip. In this paper two different high-power amplifiers, which are steps towards the realisation of this goal, are described.

To make the realisation of a single chip combined driver and high-power amplifier feasible, a technology having high gain and high output power per transistor is required. Such a technology is the pseudomorphic HEMT (PHEMT) technology, developed by FhG-IAF in the scope of an European technology program. This program aims at the development of X-band high-power amplifiers in MESFET and PHEMT technologies. A consortium consisting of Infineon, Thomson Detexis, FhG-IAF, IEMN and TNO-FEL carried out the work within this program. Earlier work obtained in the scope of the before mentioned program is reported in [2,3,4].

The technology used and the design and measurement results of the realised amplifiers are discussed in more detail in the remainder of this paper.

TECHNOLOGY

The pseudomorphic HEMT technology of FhG-IAF is used for the development of the discussed amplifiers [5]. This technology is optimised for high-power applications. The technology consists of 0.3 μm PHEMTs, E-beam gates, MIM capacitors and airbridges. Infineon performed the viahole etching and backside processing of the presented amplifiers.

The discussed amplifier designs are based on transistors that have a fishbone layout [4]. The measurements of these transistors are performed, at TNO-FEL, with the help of the active loadpull measurement system described in [6,7]. The measurement results depicted in figure 2, show a saturated output power of 900 mW/mm. Furthermore a maximum power added efficiency (PAE) of 50 % and a small-signal gain of more than 16 dB are measured. The high output power in combination with the high gain make the integration of a driver and high-power amplifier on a single, small sized, chip feasible.

AMPLIFIER DESIGN AND MEASUREMENT RESULTS

Two amplifiers are designed with the help of the discussed PHEMT technology. The first amplifier is a two-stage amplifier, which focuses on the demonstration of an output power of at least 5 Watt on a small chip size. The second amplifier under consideration is a three-stage amplifier. This amplifier focuses on the demonstration of a single chip combined driver and high-power amplifier with an output power of more than 5 Watt. Both amplifiers aim at a frequency bandwidth of 30% at X-band and a PAE of approximately 30%. Photographs of the two amplifiers are shown in figure 3 and 4 respectively.

The two-stage amplifier uses eight transistors in parallel in the output stage. These transistors have a total gate width of 11.52 mm. In the input stage four transistors are used that have a total gate width of 5.76 mm. The design methods used

and the way the source and load impedances of the matching networks are determined, is described in [4,6]. A photograph of the realised amplifier is depicted in figure 3. The realised amplifier has a size of only 16 mm^2. This small size demonstrates the potential of the used PHEMT technology for the integration of a driver and high-power amplifier on a single chip.

Typical measurement results are depicted in figure 5. The results show, for a drain voltage of 8 V, that from 7.0 to 11.0 GHz, an average output power of 6.1 Watt, an average PAE of 36%, and a gain of more than 21 dB has been measured. These results demonstrate the capability of the used technology to realise high output powers on a small chip size.

The gain realised with the two-stage amplifier is high, but not sufficient, when used in combination with the multifunction chip described in [1]. Then still a driver amplifier is needed. A gain of 28 dB is needed to remove the necessity of the application of a separate driver amplifier. To combine the driver and the high-power amplifier a three-stage amplifier is designed. This three-stage amplifier uses eight transistors in parallel in the output stage. These transistors have a total gate width of 17.28 mm. The intermediate stage uses four transistors with a total gate width of 5.76 mm. The input stage uses two transistors that have a total gate width of 2.88 mm. Larger transistors in the output stage, when compared to the two-stage amplifier, have been used to create both a higher output power and extra output power margin to account for process variations.

A photograph of the realised amplifier is depicted in figure 4. The realised amplifier has a size of only 20 mm^2. The chip size is still very small taking into account the additional amplifier stage. Large-signal measurement results of the three-stage amplifier are depicted in figure 6. The results show, for a drain voltage of 8 V, from 8.0 to 11.0 GHz, an average output power of 6.5 Watt, an average PAE of 29%, and a gain of more than 29 dB. These results demonstrate that it is possible to integrate a driver and high-power amplifier at X-band on a single, small sized, chip with the help of the before mentioned PHEMT technology. The measured output power is lower than expected. This is due to an unexpected process variation, which resulted in a shift of the location of the optimum load impedance and a corresponding reduction of the output power.

CONCLUSIONS

With the help of the PHEMT technology of FhG-IAF two small sized high-power amplifiers have been realised. These amplifiers are suited for application in future T/R modules for phased-array radar applications. The feasibility of the integration of a driver and high-power amplifier on a single, small sized, chip is demonstrated. This integration will reduce the number of chips necessary in a Transmit/Receive (T/R) module used in e.g. a phased-array radar antenna. Consequently, the cost of a T/R module is reduced.

The measurement results of the two-stage amplifier show an average output power of 6.1 Watt, a PAE of 36% and a gain of 21 dB over a relative bandwidth of 40% at X-band. For the three-stage amplifier an average output power of 6.5 Watt, a PAE of 29% and a gain of 29 dB is measured over a relative bandwidth of 30% at X-band.

ACKNOWLEDGEMENT

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[7] A.P. de Hek, “A Novel Fast search algorithm for an active load-pull measurement system”, *GAAS’98 symposium digest*, pp. 268 - 273, October 1998

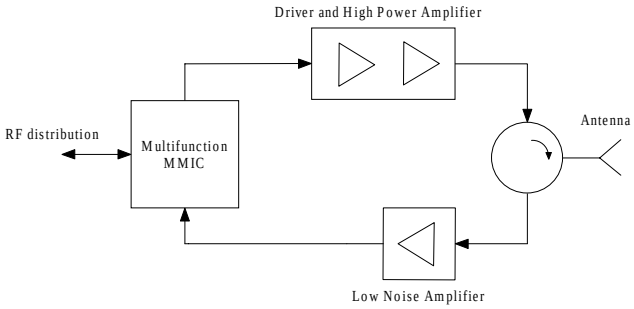

Figure 1: Block diagram TNO-FEL T/R module.

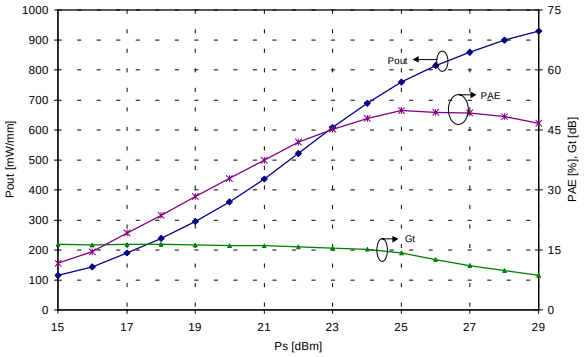

Figure 2: Large-signal measurement results of a 1.4 mm PHEMT (f=8 GHz, Vd=8 V, Vg=-0.4 V).

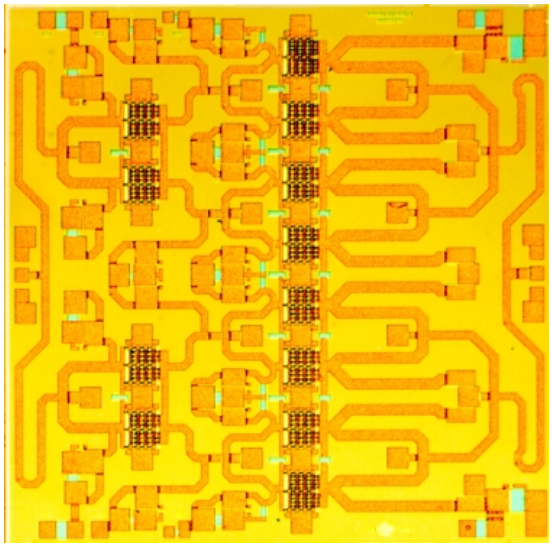

Figure 3: Photograph of the two-stage high-power amplifier (4x4 mm²).

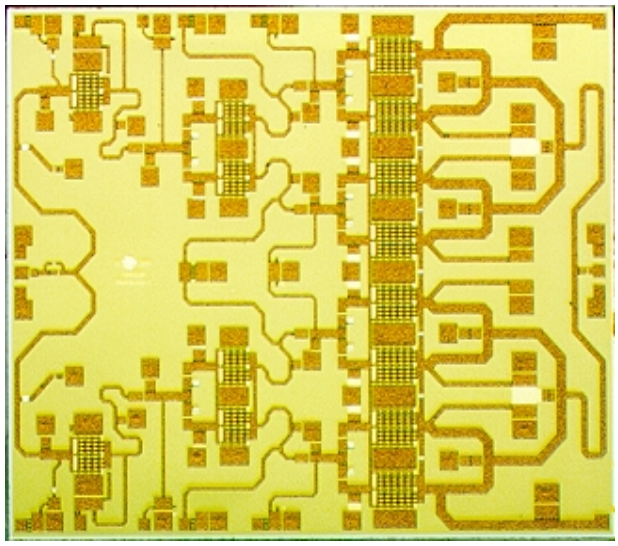

Figure 4: Photograph of the three-stage high-power amplifier (5x4 mm²).

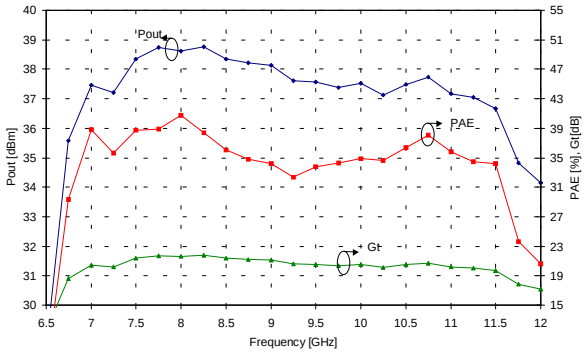

Figure 5: Measured large-signal performance of the two-stage high-power amplifier. (Vds=8 V, Vgs=-0.3 V, Pulse width=10 µs and PRF=20 kHz).

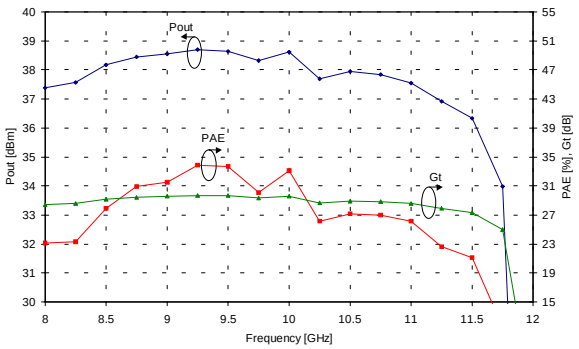

Figure 6: Measured large-signal performance of the three-stage high-power amplifier. (Vds=8 V, Vgs=-0.15 V, Pulse width=10 µs and PRF=20 kHz)