RELIABILITY EVALUATION OF GaAs MMICs

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ABSTRACT

GaAs MMICs offer significant advantages for space applications. As the technology reaches maturity and as applications are being identified, GMMT together with ESA have embarked upon the first stage of space qualification of the GMMT GaAs foundry. The most appropriate procedure for qualification of a foundry process which is required to produce relatively small quantities of a wide range of custom designs is capability approval. This paper presents results from the early stages of the evaluation phase of the ESA capability approval programme which is currently underway.

The principal test vehicle designs, test methods, bias conditions and DC/RF measurement schedules are all described. Results from the initial step stress programme and the early stages of the accelerated life tests are presented. Metal lines and interconnects, capacitors, resistors and FETs all behave as expected from previous less extensive studies. Mesa resistors in particular show exceptional stability at surface temperatures approaching 330°C. The techniques used to determine channel temperatures are described and provisional reliability assessments are included together with an outline of the remaining test programme.

Keywords: Reliability, MMIC, GaAs, Capability Approval.

1. INTRODUCTION

The rationale behind the current programme is discussed in detail in the paper "An Evaluation Programme for the Capability Approval of GaAs MMICs" by Conlon et al;[1] presented at the 1990 ESA Electronic Components conference. The major components of this programme are step stress testing, accelerated life test, endurance tests, radiation hardness assessment and long term thermal shock testing. The test vehicles, a range of discrete components and functional MMICs, are designed at or beyond the limits of the capability domain proposed for the GMMT GaAs Foundry. The programme started in March 1991 with the detailed definition and layout of the test vehicles. To date a step stress programme on the entire range of discrete components has been completed and accelerated life testing has commenced. Thermal analysis to determine channel temperatures has also been undertaken allowing the provisional lifetime predictions described in this paper to be made.

2. TEST VEHICLES

The test vehicle array has been extended and updated since the original proposals detailed by Conlon et al [1]. The vehicles are designated GS350A through to L, each representing a different component or circuit except for GS350A and G which are identical. The vehicles were manufactured using the standard F20 process, but incorporating two different implants on the same wafer tailored to maximise switch or gain FET performance. Evaluation samples were selected from two process batches to ensure a representative statistical spread of process parameters. The passive test vehicles were assembled into 16 PIN ceramic DIL packages, while FETs and MMICs were assembled into either a standard 8 lead flat pack which allows RF testing up to 3GHz or onto coplanar alumina tiles allowing testing up to 21GHz. Devices were assembled and inspected to standard foundry release criteria (including MIL-STD-883 2010 Condition B) but are otherwise unscreened by either stabilisation bake or burn-in. Electrical test and selection criteria were based on DC and RF limits defined within the foundry Design Guide. A summary of the test vehicle designs and the design or test limits represented by each vehicle appear as Table 1.

3 TEST CONDITIONS

A summary of the test conditions and sample sizes for both step stress and accelerated life tests appears as Tables 2 and 3. All evaluation testing is carried out at elevated temperatures under DC bias conditions. For low-noise (small signal) devices and passive components, operational RF voltage levels are considered small enough for degradation to be accurately simulated by stressing under DC bias only. Bias and measured parameters have been chosen according to component function and maximum operational stress. During the elevated temperature tests, DC monitoring records changes in selected critical parameters. This is supplemented by comprehensive periodic room temperature DC and RF re-characterisation.

For the step stress programme the test interval was 48 hours followed by 1000 hours at the maximum stress level. This 1000 hour extended step stress was not undertaken for devices which would form part of the accelerated life test programme.

The accelerated life tests will run for a maximum of 4000 hours or until 75% of the devices have reached the predefined failure criteria. Room temperature re-characterisation will be carried out at a minimum of five selected intervals during this test period. FETs and resistors are the principal life test components as previous work has indicated that only these components are expected to experience significant degradation under realistic stress conditions.

The failure criteria will be a 20% change in I_{dss} for FETs and MMICs, 10% change in resistance for resistors, 100% resistance change for metal lines and interconnects and 1nA leakage current for all capacitors.

The majority of the components are stressed in ovens using high volume hot air flow to maintain temperature uniformity and stability. Individual constant current, constant voltage or I_{ds} feedback control circuits, appropriate to each test vehicle, are used to maintain device bias. The only exceptions are the FETs on coplanar tiles which are mounted on a custom designed hot plate with integral biasing.

4. CHANNEL TEMPERATURES

An accurate knowledge of the channel temperature of a device under operating conditions is essential to the determination of activation energy and hence prediction of operating life. Three methods have been employed to determine these temperatures. Firstly thermal modelling has been undertaken by Dr. P. Webb at University of Birmingham from data supplied by GMMT. This has been supplemented by infrared thermal imaging carried out at the same establishment. A table of results appears as Table 4. There is good agreeement between modelled and IR measured data throughout, with the possible exception of the M3 line for which the IR measurement is suspect. In addition the IR measurements produce detailed thermograms of the devices (Figure1) showing, for example, the excellent thermal uniformity across the very wide 10Ω resistor . Where possible these results have been checked against various electrical techniques. This has proved particulary important for the high dissipation components where air flow is used to maintain the package temperature. The modelling and IR data only considers thermal impedance to the package base which is assumed to be mounted on an infinite heat sink, the electrical methods accommodate the additional thermal impedance to free air where relevant. Electrical measurements have shown that the actual resistor surface temperature for the 10Ω resistor is 330°C at 250°C ambient . The 6x175µm FETs are mounted on a large heatsink and do not therefore require a compensatory measurement. The M2 and M3 lines as measured by temperature co-efficient of resistance are running at 240°C and 230°C respectively for an ambient of 150°C.

5. STEP STRESS TEST RESULTS

The results from selected step stress and extended step stress tests on the passive structures are summarised in Figures 2 to 4. The metal lines, M2 and M3, show only a small increase in resistance (Figures 2 and 3) whilst the M2/M3 interconnects and GaAs vias show negligible changes. The changes in M1/M3 interconnect resistance (Figure 4) result from changes in the Ml metal which is used as a lateral current carrying layer to form this test structure. In circuit applications Ml forms only a vertical ohmic contact. The 'Through GaAs Via' is designed to carry 200mA explaining the excellent stability observed. However, for all the other structures 200mA represents four times the permitted Jmax of 5mA per µm of line width.

The 10Ω resistors which are designed beyond the foundry limits show exceptional stability with only a 4% change after 1000 hours at a surface temperature of 330°C. Switch and gain implant resistors behave identically (Figures 5 and 6). A standard 50Ω resistor shows almost no change, (Figure 7) after the same stress.

Capacitors were subjected to three 48 hour duration voltage steps from 10V to 50V extended to 1000 hours at 50V. Table 5 summarises the results. As expected the silicon nitride capacitors, which have a typical room temperature breakdown voltage of about 60V, degraded rapidly at the highest bias. Previous silicon nitride capacitor life tests at 15V and up to 1000 hours at 200°C failed to induce any failures.

A range of FET geometries and bias conditions were employed during the step stress programme. Figures 8 and 9 show changes in I_{dss} for 2x75µm, and 6x175µm FETs respectively after 48 hour steps from 175°C to 250°C. A separate test on a 2x75µm FET at a constant 175°C but with Vds stepped from 6 to 9V produced the results shown in Figure 10. The step stress test aimed to establish the minimum temperature required to produce significant changes in I_{dss} over the proposed 4,000 hour accelerated life test duration. The small sample sizes and short duration of each step make analysis difficult as stabilisation and degradation effects may be confused. However, at 175°C and $^1/_2$ I_{dss} bias it appears that adequate changes in I_{dss} can be induced. Life test temperatures of 175°C, 200°C and 225°C were therefore chosen.

Small changes in noise figure were recorded for the 6x175µm FET at the highest temperature step (Figure 11) but S-parameters through to 21GHz show no significant changes. A typical family of S-parameter curves after each temperature step appears as Figure 12.

6. DISCUSSION AND CONCLUSIONS

The first objective of the step stress test programme was to establish operating temperatures for the accelerated life tests to follow. The 10Ω resistors showed excellent stability even at the highest test temperature. However, the surface temperature reached at this point (330°C) is only 20°C below the polyimide curing temperature used during processing and effectively sets 250°C ambient as the maximum permissable temperature for the accelerated life test. Samples are also being tested at 200°C and 225°C in order to determine an activation energy for the major degradation mechanism. It is, however, too early in the programme to draw any conclusions which would enable operating life to be predicted.

The changes in FET performance observed during step stress tests are typical of the gate sinking phenomenon which is expected to be the dominant degradation mechanism. The more rapid changes to the 6x175µm FET characteristics, when compared to the 2x75µm device can be attributed to the higher temperature in the 6x175µm device. Accelerated life test temperatures must be kept as low as possible to avoid activating anomalous high temperature mechanisms hence 225°C was chosen as the maximum test temperature with further test groups to run at 200°C and 175°C. Insufficient data has been accumulated from these tests, as yet, to estimate activation energies and predict operating life. The co-packaging of some components means that the diode and TLM structure will also be life tested at these temperatures, while the MMICs which are included principally to examine possible component interactions will run at the middle temperature (200°C). At this temperature the MMICs should experience significant degradation without the risk of activating anomalous mechanisms.

The tests on lines and interconnects have established safe operating limits for the interconnects and vias whilst sufficient data is available from the M2 and M3 line tests to predict operating life at normal temperatures. Previous programmes have established that line resistance increases are caused by the formation of electromigration voids. A pessimistic estimate of the current acceleration factor for this process is J^2 whilst a typical activation energy would be leV. Using these figures an operating life to 100% resistance change of at least 10^9 hours at 70°C and J_{max} is predicted.

Previous test programmes on capacitors have established their exceptional stability at normal operating voltages and high temperatures [2]. This is the first test to examine performance at voltages close to breakdown. Progressive increases in leakage current were observed. Samples at varying stages of breakdown are therefore available for the failure analysis programme.

Roesch et al [3] have shown that analysis of discrete components can be used to predict the lifetime of complete MMICs because the contribution from the least reliable component will dominate MMIC degradation. The proposed accelerated life test programme (Table 3) is therefore restricted principally to FETs and resistors but also includes MMIC endurance tests in order to confirm this assumption.

The full evaluation programme will additionally examine the radiation hardness of selected components and circuits as well as die integrity when subjected to long term thermal shock. A summary of these aspects of the programme which are yet to commence appears as Table 6.

Acknowledgements

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References

(1) *An Evaluation Programme for the Capability Approval of GaAs MMICs* Conlon, R.F.B., Lindsay, C.E., Brydon, G.M., Bensoussan, A., Proceedings ESA Electronic Components Conference, 1990, pp 85 - 91.

(2) *Reliability Testing of Polyimides for GaAs MMIC Application.* Conlon, R.F.B. and Turner, J.A., ESREF 90, pp.465-470

(3) *Proving GaAs Reliability with IC Element Testing.* Roesch, W.J. and Stunkard, D., U.S. Conference on GaAs Manufacturing Technology, November, 1988, pp 94-98

TABLE 1

Test Vehicle	Limits Examined	Cell Reference
6x175µm FET (Switch Implant)	Largest Foundry FET	A/G
6x175µm FET (Gain Implant)	Largest Foundry FET	A/G
2x 75µm FET (Gain Implant)	Typical Small FET	D
6x 75µm FET (Gain Implant)	Typical Midrange FET	L
Diode	Not Currently Supported by Foundry	L
10Ω Resistor (Gain Implant)	Maximum Power Dissipation per Unit Area	J
10Ω Resistor (Switch Implant)	Maximum Power Dissipation per Unit Area	K
60pF Silicon Nitride Capacitor	Largest Foundry Value	F
2.5pF Polyimide Capacitor	Largest Foundry Value	F
Interdigital Capacitor	Maximum Aspect Ratio of M2 Line/Gap	F
M2 Meander	Typical Line Width	C/I
M3 Meander	Minimum Line Width	E
M1-M3 Interconnect	Minimum Dimension Interconnect	C/I
M2-M3 Interconnect	Minimum Dimension Interconnect	C/I
Through GaAs Via	Standard foundry	C/I

	Package Type	Sample Size	Step Stress	Other Conditions	Monitor	Test Vehicle
Ig FET (6 X 175um)	Tile	16	175 to 250°C.	Vds=6V; Ids=50mA (=½Idss).	Vgs	A/G
Sw FET (6 X 175um)	Tile	16	175 to 250°C.	HTRB: Vds=0V; Vgd=-8V (=¾Vbd).	Igd	A/G
Ig Resistor (10 ohm)	DIL	8	175 to 250°C.	2V bias.	Current	J
Sw Resistor (10 ohm)	DIL	8	175 to 250°C.	2V bias.	Current	K
Capacitor Nitride	DIL	13	10/20/50V.	150°C.	I(leakage)	F
Capacitor Polyimide	DIL	13	10/20/50V.	150°C.	I(leakage)	F
Capacitor Interdig.(M2)	DIL	13	10/20/50V.	150°C.	I(leakage)	F
M2 Meander	DIL	16	Jmax - 4xJmax: 50/100/200mA.	150°C.	V	C/I
M1 - M3 Interconnect	DIL	16	Jmax - 4xJmax: 50/100/200mA.	150°C.	V	C/I
M2 - M3 Interconnect	DIL	16	Jmax - 4xJmax: 50/100/200mA.	150°C.	V	C/I
Through GaAs Vias	DIL	16	Jmax - 4xJmax: 50/100/200mA.	150°C.	V	C/I
M3 Meander	DIL	16	Jmax - 4xJmax: 50/100/200mA.	150°C.	V	E
Ig FET (2 X 75um)	8L FP	10	175 to 250°C.	Vds=6V; Ids=2mA (=0.1xIdss).	Vgs	D
Ig FET (2 X 75um)	8L FP	10	Vds=6/7/8/9V.	175°C; Ids=7.5mA (=½Idss).	Vgs	D
Diode	DIL	10	175 to 250°C.	HTRB: Vrev=4V.	IR	L
M3 Line	DIL	10	175 to 250°C.	Imax=50mA.	V	L
Stab. FET (6 x 75um)	DIL	10	175 to 250°C.	Vds=5V; Ids=22mA (=½Idss).	Vgs	L

Note: Dividing lines in the above table indicate co-packaged and co-tested components

Table 2 *Outline plan for step stress test*

	Package Type	Sample Size	Temps.	DC Bias	Monitor	Test Vehicle
Ig FET (6 X 175um)	Tile	32x3	T2,T3,T4.	Vds=6V; Ids=50mA (=½Idss).	Vgs	A/G
Sw FET (6 X 175um)	Tile	32x3	T2,T3.T4.	HTRB: Vds=0V; Vgd=-8V (=¾Vbd).	Igd	A/G
Ig Resistor (10 ohm)	DIL	16x3	T1,T2,T3.	2V bias.	Current	J
Sw Resistor (10 ohm)	DIL	16x2	T1, T3.	2V bias.	Current	K
Functional MMIC (Gain)	8LFP	16x1	T3.	Vds=6V; Ids=45mA (=½Idss).	Vgs	B
Functional MMIC (Sw)	8LFP	16x1	T3.	HTRB: Vds=0V; Vgd=-8V (=¾Vbd).	Igd	E
Ig FET (2 X 75um)	8L FP	10x3	T2,T3,T4.	Vds=6V; Ids=7.5mA (=½Idss).	Vgs	D
Diode	DIL	10x3	T2,T3,T4.	HTRB: Vrev=4V.	IR	L
M3 Line	DIL	10x3	T2,T3,T4.	Imax=50mA.	V	L
TLM Structure	DIL	10x3	T2,T3,T4.	Imax=30mA.	V	L
Stab. FET (6 x 75um)	DIL	10x1	T3.	Vds=5V; Ids=22mA (=½Idss).	Vgs	L

T1, T2, T3, T4 To be agreed following Step Stress Tests (provisionally 175 / 200 / 225/ 250°C)

Life Test duration = Up to 4000 hours

Note: Dividing lines in the above table indicate co-packaged and co-tested components.

Table 3 *Outline plan for accelerated life tests*

Test Vehicle	Component	Base Temp.	Power Dissipation	Simulation Tmax	Power Dissipation	IR Meas Tmax
E	M3	70°C 200°C	100mW	100.9°C 233.1°C	174mW	93.6°C
I	M2	70°C 200°C	200mW	89.6°C 227°C	358mW	100.0°C
K	Resistor (10ΩSw)	70°C 200°C	400mW	92.7°C 229.6°C		
J	Resistor (10Ω Gain)	70°C 200°C	400mW	91.0°C 227°C	400mW	91.6°C
J	Resistor (50Ω Gain)	70°C 200°C	80mW	81.3°C 215.4°C		
C	TLM	70°C 200°C	150mW	81.1°C 215.3°C		
D	FET (2X75 μm)	70°C 200°C	60mW	86.4°C 222.7°C	45mW 60mW	82.5°C 84.7°C
L	FET (6X75 μm)	70°C 200°C	110mW	83.5°C 218.7°C		
B	FET (6X150 μm)	70°C 200°C	270mW	96.5°C 235.3°C		
A	FET (6X175 μm)	70°C 200°C	300mW	99°C 238.3°C		

Table 4 *Comparison of simulated vs. infra red maximum chip temperature*

Stepped voltage 10/20/50V 150°C T(amb); 13 Samples

	48 Hrs 10V	48Hrs 20V	48Hrs 50V	+168Hrs 50V	
Nitride	0	1(8%)	5(38%)	11(73%)	Failures
Polyimide	0	0	0	0	Failures

Table 5 *Capacitor step stress test results*

	Package	Sample Size	Stress	DC Bias	Test Vehicle
Sw FET (6 X 175um)	8L FP	15	To 100K Rad	Ids=50mA	A/G
Sw Resistor (10 ohm)	DIL	15	To 100K Rad	2V Bias	K
Capacitor Interdigital (M2)	DIL	15	To 100K Rad	6V Bias	F
Capacitor (Nitride)	DIL	15	To 100K Rad	6V Bias	F
Capacitor (Polyimide)	DIL	15	To 100K Rad	6V Bias	F
Mesa/Mesa Isoln. Structure	DIL	15	To 100K Rad	10V Bias	C/I
MMIC (Gain)	8LFP	15	To 100K Rad	Ids=50mA	B
MMIC (Switch)	8LFP	15	To 100K Rad	Ids=50mA	E

	Package	Sample Size	Cycles/Temp	Test Vehicle
Ig FET (2 X 75um)	8L FP	10**	500 cycles -65 to +150°C	D
Diode	DIL	10**	500 cycles -65 to +150°C	L
Max. Size Chip	DIL	10**	500 cycles -65 to +150°C	

** 5 epoxy, 5 eutectic (AuSn) die attach in hermetic package.

Note: Dividing lines in the above table indicate co-packaged and co-tested components.

Table 6 *Outline test plan for radiation and temperature cycling tests*

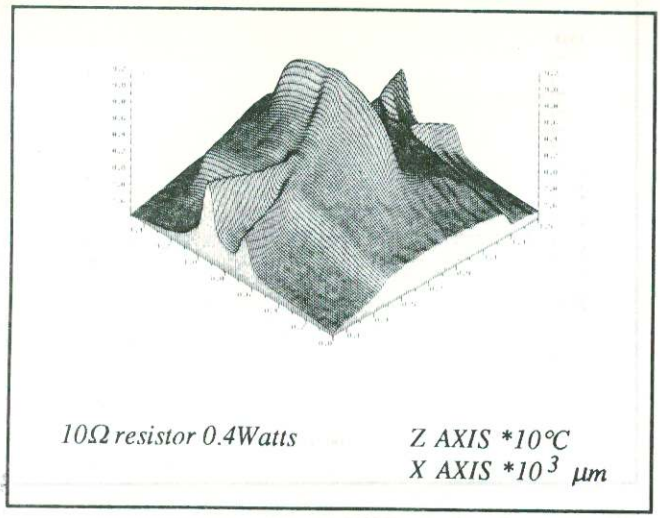

Figure 1 *Infra-red thermograph 10Ω Resistor (400mW)*

T(amb) = 150°C; stepped J = 50/100/200mA (Jmax = 50mA)

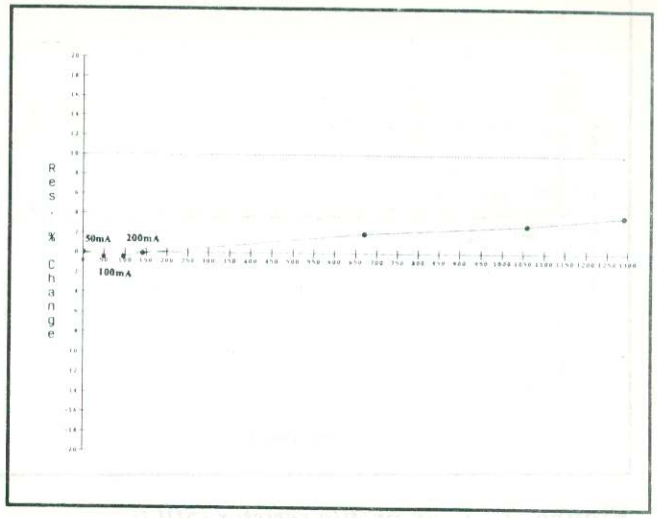

Figure 2 *M2 meander line - step stress test*

T(amb) = 150°C; stepped J = 50/100/200mA (Jmax = 50mA)

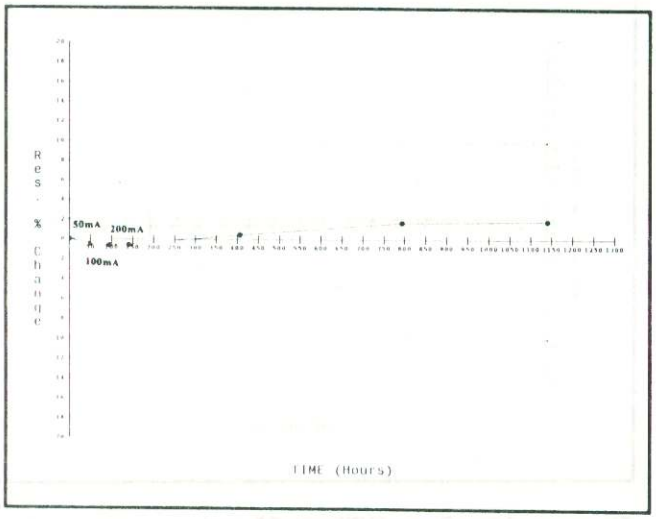

Figure 3 *M3 meander line - step stress test*

T(amb) = 150°C; stepped J = 50/100/200mA (Jmax = 50mA)

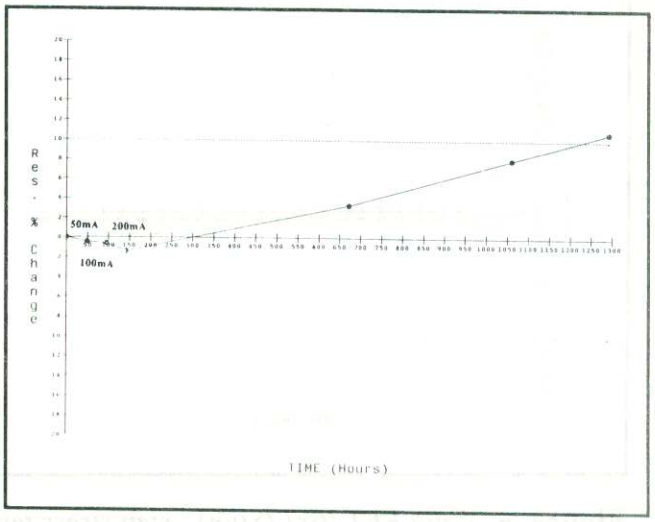

Figure 4 *M1/M3 interconnect - step stress test*

2V bias; stepped temp = 175/200/225/250°C

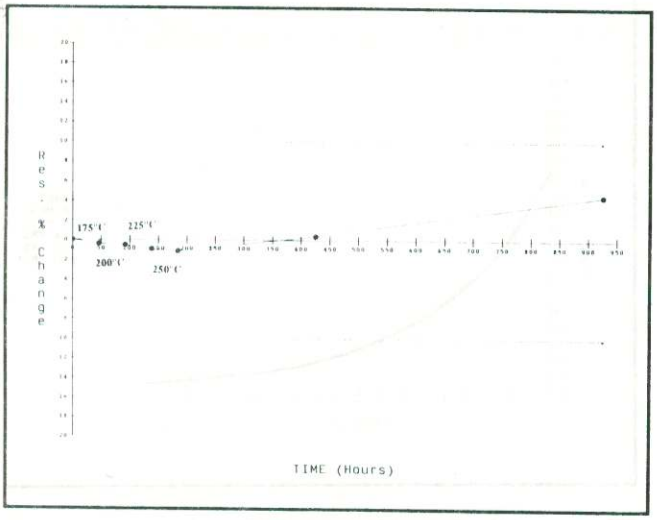

Figure 5 *Switch profile resistor (10Ω) - step stress test*

2V bias; stepped temp = 175/200/225/250°C

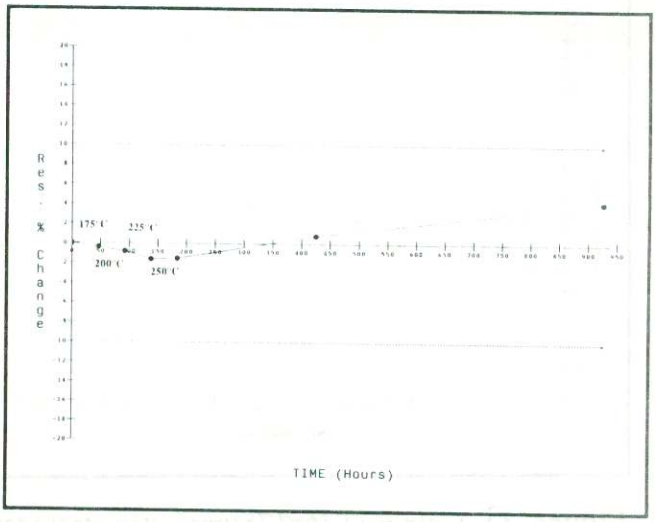

Figure 6 *Gain profile resistor (10Ω) - step stress test*

2V bias; stepped temp = 175/200/225/250°C

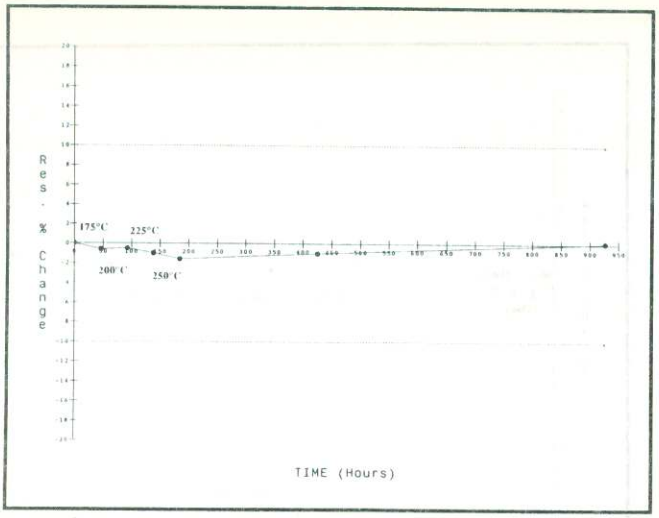

Figure 7 *Gain profile resistor (50Ω) - step stress test*

2V bias; Stepped temp = 175/220/225/250°C

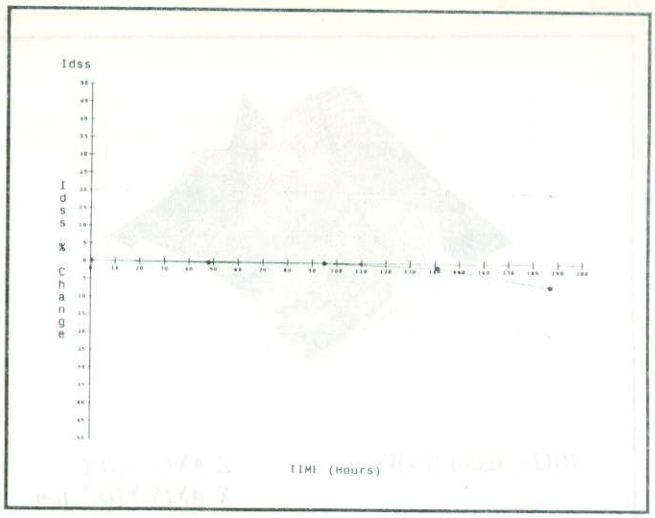

Figure 8 *Gain FET (2x75µm) -step stress test*

1/10 Idss; stepped temp = 175/200/225/250°C

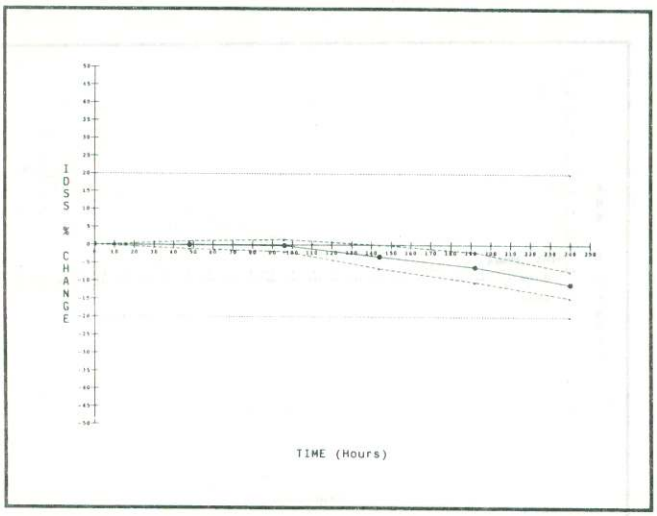

Figure 9 *Gain FET (6x175µm) - step stress test*

1/2 Idss; stepped temp = 150/175/200/225/250°C

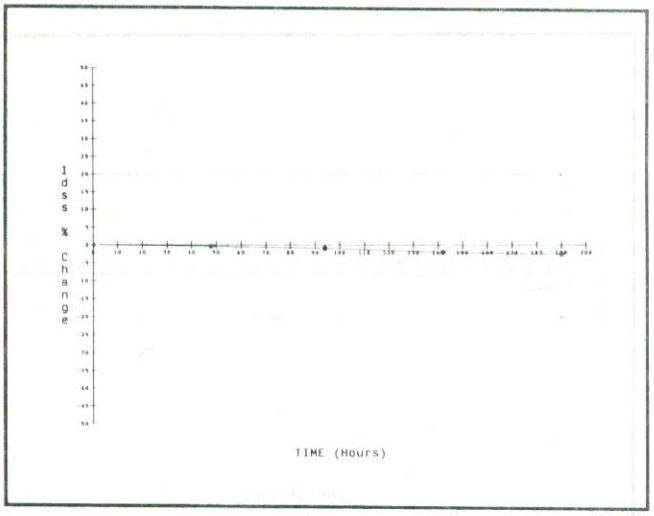

Figure 10 *Gain FET (2x75µm) - step stress test*

1/2 Idss; stepped Vds = 6/7/8/9 V

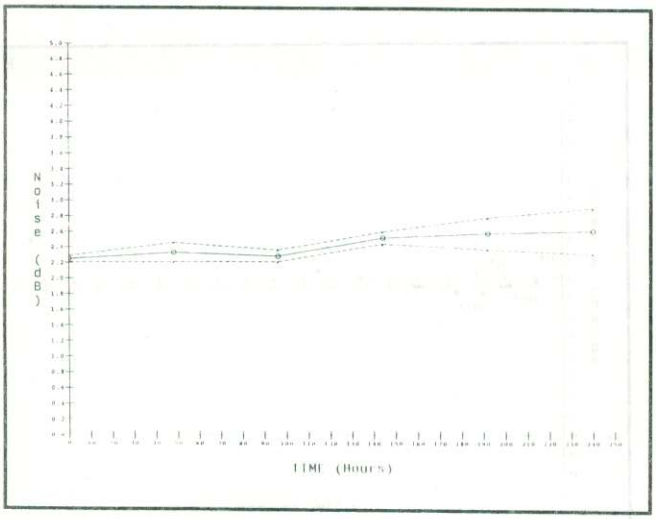

Figure 11 *Gain FET (6x175µm) - step stress test*

1/2 Idss; stepped temp = 150/175/200/225/250°C

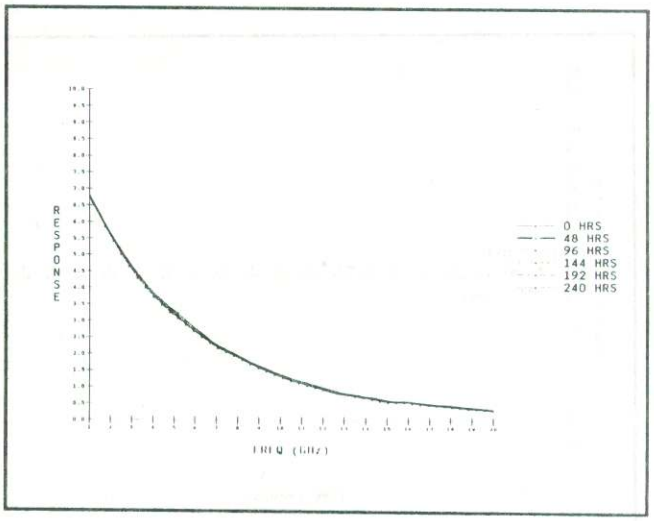

Figure 12 *Gain FET (6x175µm) - step stress test*

1/2 Idss; stepped temp = 150/175/200/225/250°C