METHODOLOGY FOR SPACE QUALIFICATION OF MMIC's

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1. INTRODUCTION

The use of microwave monolithic integrated circuits (MMIC) in future space applications is becoming increasingly probable because of their high performance and low mass. Moreover, certain equipments, such as large active antennas, are only conceivable with MMIC solutions.
In order to make sure that such products have quality levels compatible with space requirements, it becomes necessary to establish a qualification methodology taking all the specificities of GaAs MMIC's into consideration.
An inter-administration working group with members from France Télécom (CNET), the Délégation Générale de l'Armement (CELAR) and the Centre National d'Etudes Spatiales has been set up to lead thinking on this subject and dialogue with national industry (designers and manufacturers).
Apart from the technical characteristics proper to MMIC's, it appeared that three important points have to be taken into account :

- These technologies are relatively recent, which means that they are evolving fast and there is virtually no feedback on experience.
- It is very difficult to "fix" a fabrication procedure during a space programme time sequence.
- It is necessary to work with a manufacturer having his process well under control so as to be able to respond to changes in the fabrication procedure.

To take all these necessities into account, our methodology is based on human expert appraisal, which provides great flexibility in the way of working and can manage technological changes without calling established knowledge into question.
The approach we propose is centred around three steps : audit, evaluation and procurement.

2. AUDIT

This stage contains various objectives, which we shall look at more closely.
First of all, the concept of customized circuits, which supposes a relatively small production volume, taken together with the recent nature of the technologies used in making these components, has led us to imagine a concept for managing developments in the fabrication procedure. It would maintain possible a qualification status compatible with the planning requirements of space programmes.
It is necessary to evaluate the technology in advance of the procurement for the flight models, and yet it does not seem reasonable to ask a manufacturer to freeze his process for several years, as developments generally tend to improve performance, efficiency or reliability.
If this evolving situation is to be managed, a very close partnership must exist among all involved partners (agency, designers and manufacturers).
The basis of this partnership need to be laid during the audit phase. It is imperative that the qualifying agency would have a thorough knowledge of the manufacturer's technology and be able to dialogue with the personnel directly involved in the various production steps.

It is, as an example, indispensable to possess a tool in order to control any drift in the procedure, such as SPC (Statistical Process Control).
Thus, the audit is the time sequence to make sure that the manufacturer has his production methods well in hand for a long time and is able to respond efficiently to possible developments.
It is also during the audit phase that an analysis of the reliability results available from the manufacturer would determine at which level the evaluation phase should be initiated.
Finally, it must be checked that the manufacturer's quality assurance system is organized in such a way as to satisfy the demands imposed by the space industry requirements.

3. EVALUATION

A few points should be stated before going into the details of the evaluation plan.
Considering the limited experience we have of MMIC technologies, it appears difficult to define a generic function capable of guaranteeing a satisfactory level of quality and reliability over the whole range of functional applications. In our opinion, each individual function needs to be validated from a reliability point of view.
Moreover, the fabrication yield currently obtained by manufacturers and the number of test pieces required by our programme have led us to limit our methodology to technologies using 3" or larger wafers.
The evaluation plan can be splitted into two successive steps. Figure 1 illustrates the generic evaluation diagram.

3.1 Pre-evaluation

Pre-evaluation phase takes place ahead of the project needs, which means that the functional domain of the circuits has not been defined. It is presented on figure 2.
Its aim is to obtain information on the technology's generic degradation mechanisms and the parasitic effects penalizing the monolithic integration.
Two test vehicles are used for this purpose.
The TCV (Technical Characterization Vehicle) is made up of elementary cells (MESFET, Capacitor, Self inductance, etc.) available in the process, which are designed according to the most stringent design rules.
The DEC (Dynamic Evaluation Circuit) is a circuit enabling microwave measurements to be made so that their drift during testing can be assessed. The design of this circuit is left up to the manufacturer/designer responsibility.
The tests performed on these pieces are :

- high temperature storage (250°C to 300°C), which will lead to purely temperature-dependent degradation mechanisms mainly affecting the behaviour of the metallic layers;
- bias aging tests, in which the devices are subjected to high electrical fields. The operating temperature of devices under tests should not exceed 225°C, in order to investigate the bias conditions contribution to the failure mode.

3.2 Validation of the MMIC

This is the step immediately before MMIC procurement. It consists of validating each design from the reliability point of view and also of checking the stability of the production process and its reliability with respect to the results obtained in pre-evaluation phase. This step is illustrated in figure 3.
For cost and scheduling reasons, MMIC validation may start even if the electrical performance of the run does not meet the specifications. In this case, expert assessment will be needed to give a ruling of the representativity of the samples relative to the corrected design used in the following runs.

A short life tests program is initially carried out on TCVs and DECs. The outcome of these tests must be in agreement with the pre-evaluation results. It verifies the technological process did not drift along all the qualification procedure.
Depending on the conclusions reached and the changes made in the fabrication procedure between pre-evaluation and validation, additional evaluation may be decided upon.
Once it has been demonstrated that the reliability is reproducible, life tests can begin on the functions. This enables the maximum information to be obtained from the prototypes of the flight models during the short period before procurement. At this time, the fabrication procedure is frozen, and remains so until all the functions necessary for the application have been supplied.
In the case where validation was performed on functions not meeting the electrical specifications, acceptance of the final design will be performed on a batch satisfying the specifications before procurement proper takes place. A programme similar to the validation one, but lightened, will be used.

4. PROCUREMENT

The objective here is to guarantee the quality and reliability of the components procured whilst limiting costs and delays. The defined procedure must also take current production rates into consideration so that sampling for tests does not significantly reduce the number of components at the end of the selection process. To this end, it is preferable to limit the number of different functions per wafer. Indeed, the lack of experience in MMIC technologies and their specificity oblige us to restrict the notion of lot to a single wafer for the moment. However, this point is subject to change according to the potential future maturity of GaAs MMICs.
Finally, present applications using MMIC's often require deliveries to be made in chip form. It is for this reason that the selection process covers procurement of components as chips and as individually packaged units.

4.1. Wafer acceptance test (WAT)

It is reported in figure 4. After manufacture, all the MMIC's present on the wafer are measured under probes to obtain the DC and RF electrical yield. The WAT includes a number of tests that will be carried out on the test vehicles to avoid reducing the number of MMIC's available.
The reportability of the chips is also verified during this phase.
When chips are delivered as such, each unit is marked so as to provide individual traceability of results, which will make subsequent selection of MMIC's easier.

4.2 Selection

This methodology draws on specifications already in force, PSS-01-608 for chips and SCC 9000 for encapsulated integrated circuits.
For deliveries in chip form, the originality of the method lies in the use of minor optical rejects for lot validation tests.
The life test will depend on the results obtained during the evaluation.
When an uncut wafer is delivered, the chip selection tests will be performed under the responsibility of the hybrid manufacturer.
For package delivery, screening and LAT will be carried out. LAT 1 will be required for each new lot of package. Environment testing will be performed on minor optical rejects so as not to reduce the lot of flight models.

5. CONCLUSION

In the changing context of MMIC technologies, we have put forward a quality assurance approach, compatible with space applications, that does not reduce the competitivity of MMIC's relative to other technologies. This has been done by taking industrial realities into account.
By sharing the competence of CNET, CELAR and CNES, and thanks to the cooperation of various French industrialists, it has been possible to produce a document that is recognized and applicable at national level.
This methodology should now be applied without delay to concrete cases involving French and foreign manufacturers.

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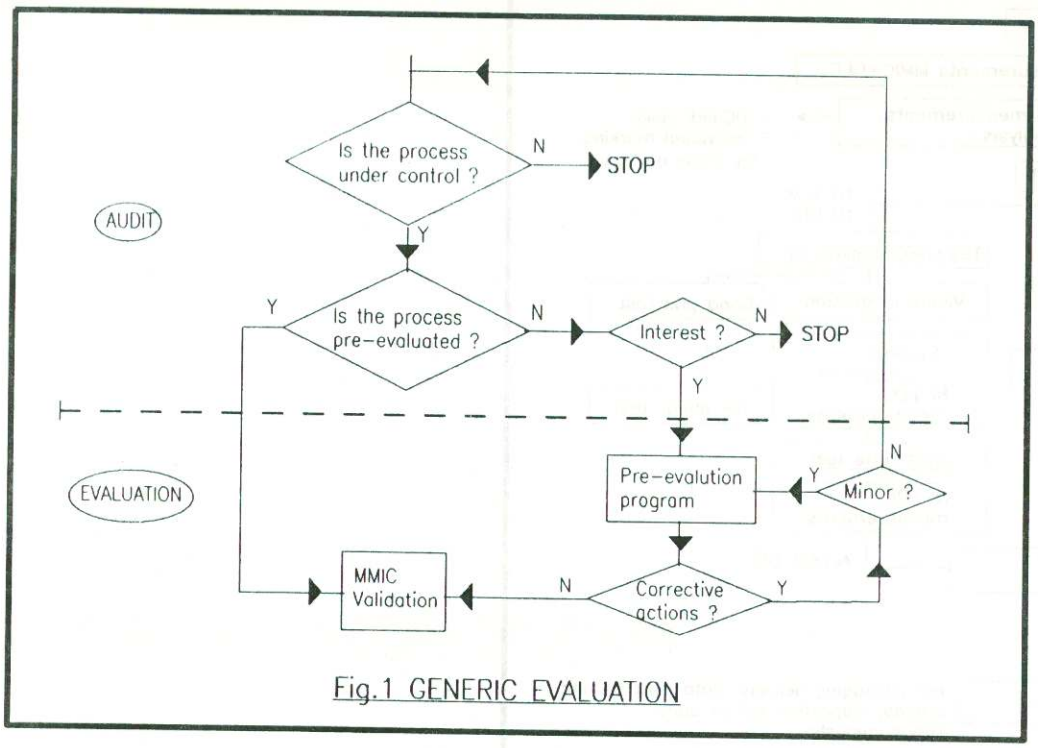

Fig.1 GENERIC EVALUATION

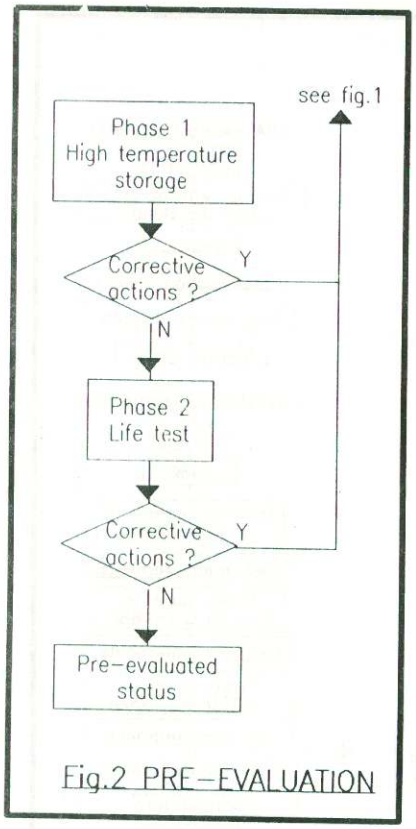

Fig.2 PRE-EVALUATION

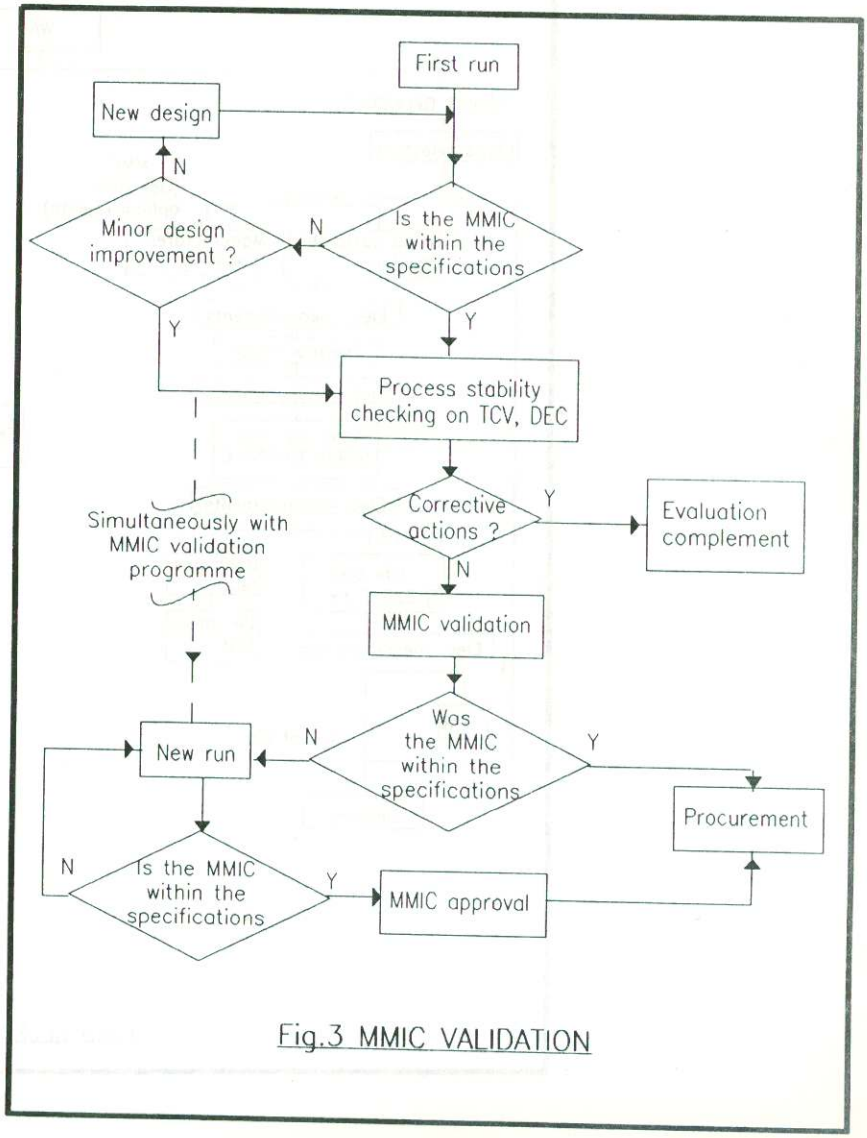

Fig.3 MMIC VALIDATION

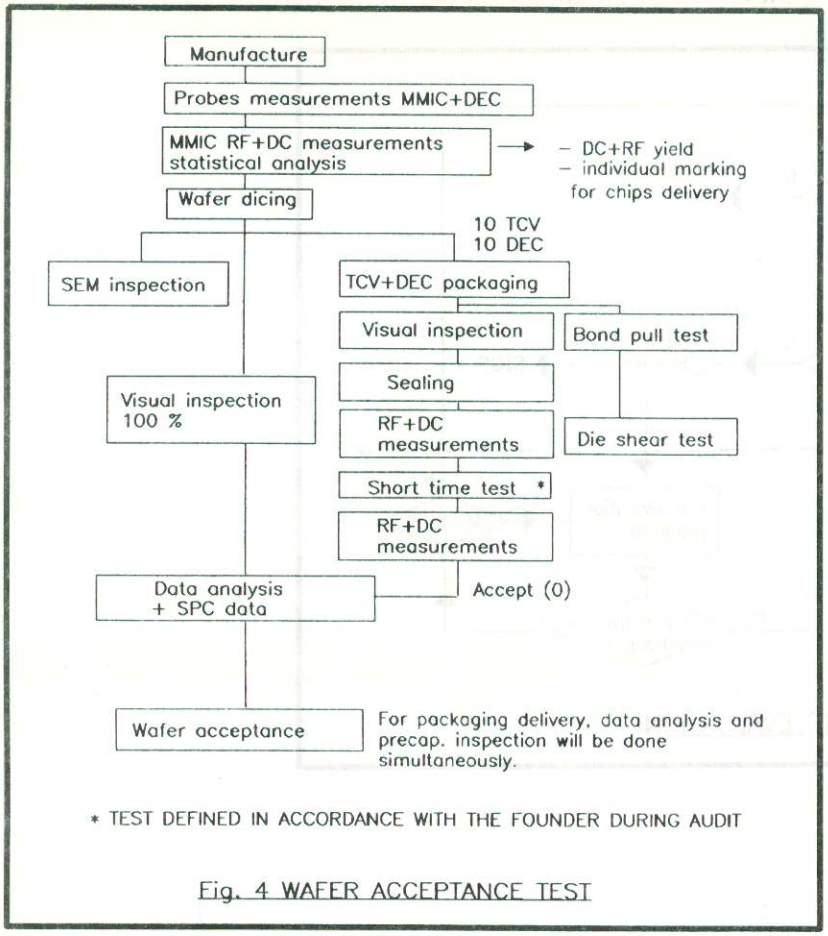

Fig. 4 WAFER ACCEPTANCE TEST

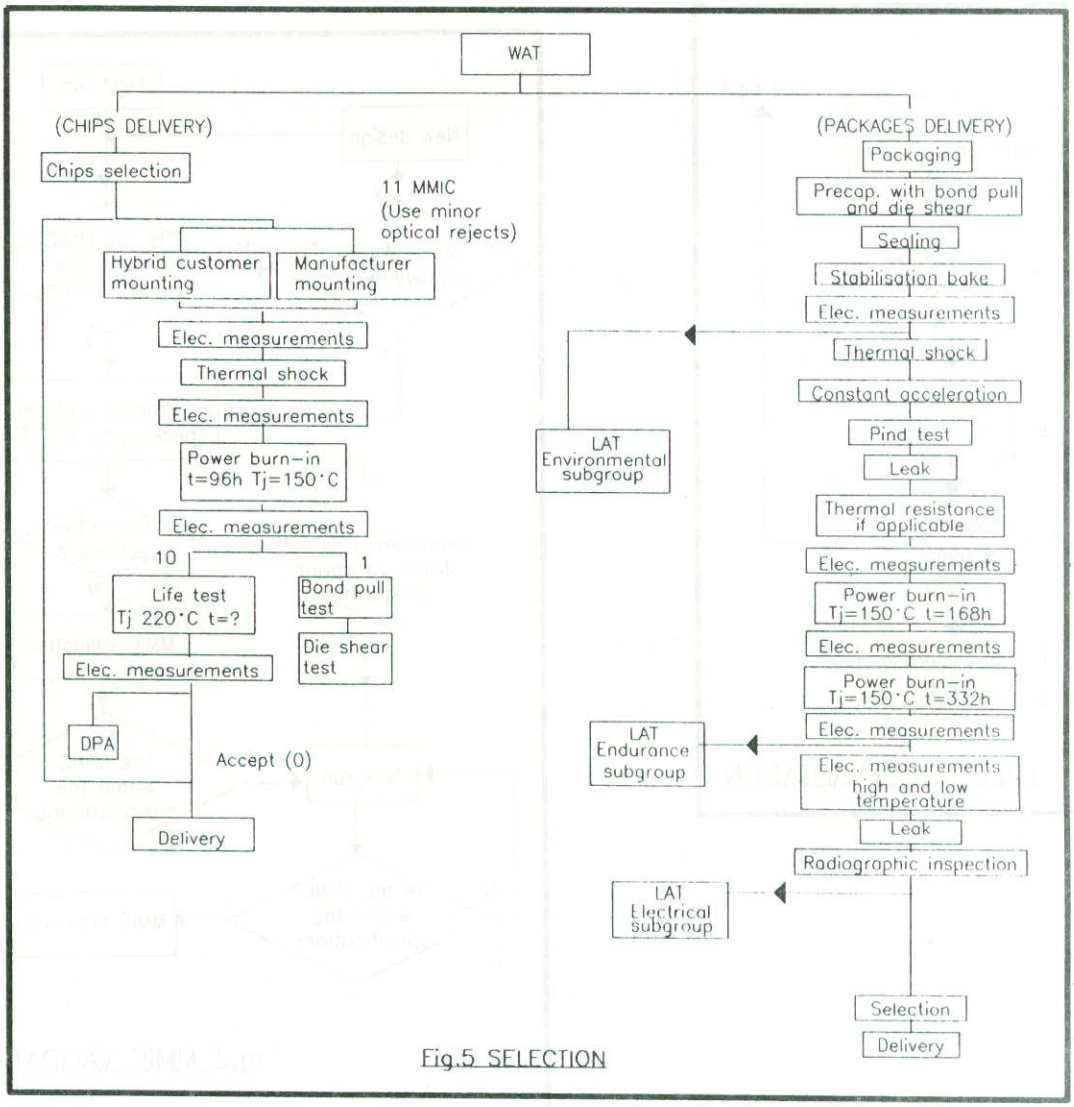

Fig.5 SELECTION