GAAS MMIC DIE ASSEMBLY

P. LAUTIER, C. DREVON, A. COELLO VERA
ALCATEL ESPACE
Service Technologie
26, Avenue J.F. Champollion
B.P. 1187.
31037 TOULOUSE CEDEX, FRANCE

ABSTRACT

The widespread use of GaAs MMICs in microwave systems require assembly technologies with high yields and high reliability, while preserving the intrinsic performance of the die. This is a difficult task, given the large lateral dimensions and reduced thickness of MMICs, complicated by the presence of via-holes.

This paper will present some of the results obtained during assessment of various techniques used for die-attach. These results show that the major reliability concern is the behaviour of the die attach medium within the via-holes. We will present a new process designed to control this behaviour.

Keywords: GaAs MMICs, Die attach, Epoxy, Au/Sn solder, Via-holes.

1 SURVEY OF ASSEMBLY TECHNIQUES FOR MMIC ASSEMBLY

1.1 Chip and wire

This is the most traditional and also the most commonly used method for MMIC assembly. The die attach may be done by either conductive (silver filled) epoxy die attach, or Au/Sn brazing. Given the extremely high activation energies of the failure mechanisms observed in GaAs integrated circuits (Ref. 1), there are no other die attach system used for GaAs ICs. The higher temperatures commonly used for die bonding silicon-based IC's, such as with the Au/Si eutectic solder (363°C), or with silver/glass based systems (380 to 420°C), would considerably affect the potential lifetime of GaAs-based ICs.

The wire interconnects can be bonded by either a thermocompression or a thermosonic process. Gold wire is universally used, given the nature of the interconnection layers within the chip. While the brittleness of the GaAs material is higher than of silicon, our experience is that no failure is induced by the ultrasonic power used for bonding fine (25 microns diameter) wire.

1.2 Microwave T.A.B.

This approach is being developed notably by NTT Applied Electronics Laboratories (Ref. 2). The main objective of this development is to minimize the parasitic effects of the connecting wires. In this variant of T.A.B., the system of interconnections is coplanar, and there is a a matching coplanar structure on both the chip itself and the interconnections external to the chip/T.A.B. ensemble. This places some restrictions on the design of the chip, but, on the other hand, alleviates some of the problems brought by the specific features of the non-coplanar MMICs, such as the reduced thickness and the via-holes. In the coplanar T.A.B/chip approach, the only purposes of the die attach are thermal transfer and mechanical attachment. It can be conceived that a non-electrically conductive epoxy could be used for die-attach in this case.

1.3 Flip Chip

While flip-chip interconnection systems (either tin/lead or gold based) have been developed for decades for silicon IC's, they are still in the early stages of development for MMICs. They would require an uniplanar design of the chip, similar to the T.A.B. system, and would present the same problems as the flip-chip bonded silicon ICs, such as a heat transfer problem, and difficulties to perform visual inspection of the chip after assembly, which can be a serious drawback for high reliability applications.

2 SPECIFIC PROBLEMS RELATED TO THE DIE ATTACH OF GAAS MMIC

The major distinctive features of GaAs based MMIC's, from a packaging point of view, are the presence of metallized via-holes that connect the topside and bottomside metallizations, and the reduced thickness of the chip, which is needed for manufacturing via-holes of acceptable lateral dimensions, and, in the case of power MMICs, for thermal transfer reasons. These two features must be accounted for in the selection of the die attach system, or they can lead to serious reliability problems.

2.1 Epoxy die attach

Epoxy die attach is a relatively straightforward technique, widely used in the manufacturing of low frequency and microwave low power hybrids. Probably for these reasons, it is not frequently discussed in the literature related to MMIC assembly. During the assessment of this technique for MMIC die attach, we have found, however, two problems that can be related to the specific features of GaAs MMICs: via-hole metallization collapse, and shift of electrical characteristics during high temperature storage.

2.1.1 Via-Holes

After bonding with silver-epoxy MMICs with via holes, we have, in some instances, observed a collapse of some of the metallized areas covering via-holes (see Figure 1). This, in turn, caused the passivation layer to fracture at the top edge of the via-hole (see Figure 2). Microsectioning (see Figure 3) revealed that in the case of this particular IC, the epoxy-silver adhesive had completely filled the via-holes. This created a pulling force on the top metallization layer, and the passivation cracking.

2.1.2 Electrical performance stability

Step-stress testing is commonly used during the qualification exercises of MMICs foundries, in order to identify failure mechanisms and their activation energies. During one of these exercises, it was found a significative difference in results between Au/Sn soldered dice, mounted by Alcatel Espace, and silver-epoxy attached dice, mounted by the foundry.

Figure 4 shows an example of this phenomenon. The devices tested are diodes, part of a test structure. They are stored at high temperature under reverse bias (HTRB). The steps are 175°C, 200°C and 225°C, for 48 hours at each step. Top curves, which show increase of leakage current along time and temperature, are epoxy die attached parts. Bottom curves are Au/Sn die attached parts.

These temperatures are not typical of the ones found during the normal life of spacecraft hardware, and these results must be therefore interpreted with care. They show, nevertheless, that there is some interaction between the active components and epoxy by-products within the package cavity.

2.2 Soldering

Au/Sn soldering of GaAs components can be performed in two different ways:

- Hand soldering, where the GaAs dice is manipulated with tweezers, and scrubbed in a circular motion on the molten solder preform, placed on a hot plate set slightly above the solder melting point (280°C).
- Furnace soldering, where GaAs dice, placed in fixtures over solder preforms, are run through a temperature cycle that peaks at 300°C.

Given the properties of the Au/Sn solder, soldering of GaAs dice has to be made in a non-oxidizing atmosphere. During hand soldering, this is accomplished by flooding the work surface with nitrogen. As for furnace soldering, the temperature cycle can be performed in a vacuum, under a nitrogen atmosphere, or a combination of vacuum/nitrogen cycles.

2.2.1 Hand soldering

The circular motion needed to break the oxide film that forms on the molten solder is generally considered as leading to the formation of voids in the solder joint (Ref. 3). These voids are then believed to be detrimental to the reliability of the assembly (Ref. 4), creating hot spots in power devices, and fracture initiating sites during temperature excursions.

In our experience, however, the size and extent of these voids can be minimized during hand soldering, with proper operator training and process parameter control. See for example Figure 5, which shows a cross section through a hand-soldered MMIC chip. In the solder joint, only very small voids can be seen.

The hand-soldered assemblies made in this way have been subjected to thermal cycling (up to 500 cycles, -55°C to +125°C), without degradation. GaAs dice have been soldered to alumina , Kovar and Cu/W composites with similarly good results, somewhat in contradiction with the results of (Ref. 5).

The major reliability concern apparent in the hand-soldering technique is the difficulty in controlling the amount of solder build-up inside via-holes. Upon small differences in the process, the solder buid-up can range from a concave fillet (see Figure 6), to a wetting of the metallized inner surfaces of the via-holes (see Figure 7), and even to a complete filling of the via-holes with solder (see Figure 8). In the latter case, given the large difference in the thermal expansion coefficients of GaAs (5.3 ppm/°C) and Au/Sn (16 ppm/°C), pulling forces are exerted on the GaAs and on the top metallization, leading to cracking of the material (see Figure 9).

2.2.2 Furnace soldering

Furnace soldering of GaAs MMICs has been developed recently, primarily as a mean to reduce or suppress voids. Most developments, however, have been carried out by using special backside preparation (Ref. 6), or thin film deposition of Au/Sn (Ref. 7). These two processes are difficult to implement by the end-user, who is generally reduced to use the backside preparation process of the foundries.

A technique commonly used in these developments is the application of mechanical pressure on top of the chip, in order to break the oxide films present on both surfaces of the solder preform (Ref. 8).

This technique is difficult to rely on for real-life MMICs, which have generally air-bridges as a second layer of metallization. Making contact to or applying pressure on the top surface causes the air bridge to collapse (see Figure 10), a type of defect for which visual inspection is particularly difficult to perform.

3 QUALITY AND RELIABILITY IMPROVEMENTS BY PROCESS CONTROL

Given the results exposed above, our view is that:

- Au/Sn die attach is more reliable than epoxy based systems, due to the complete absence of outgassing by-products within the package cavity.
- Whatever the die attach system chosen, it is of prime importance of controlling the amount of die attach material build-up in the via-holes. This is the predominant reliability factor to consider, rather than the amount of voiding under the die, which is traditionnally the one scrutinized in the literature.

Under development at Alcatel Espace is a furnace sealing process with a controlled atmosphere, which does not use mechanical pressure on top of the chip. Preliminary results of this process, shown on Figure 11, show that by parameter control, it is possible to set precisely the amount of solder build-up inside via-holes, thus maximizing reliability of the assembly.

Figures

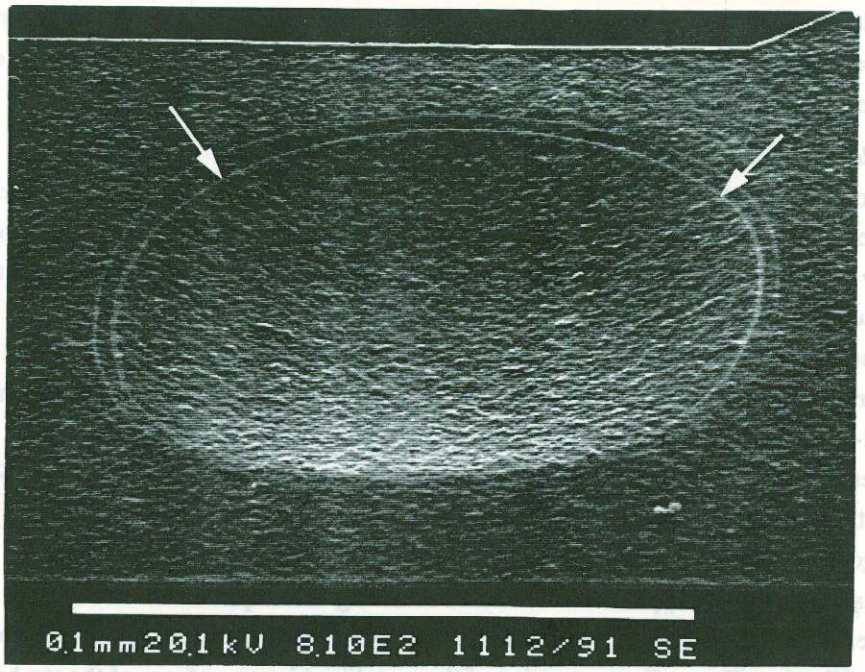

Figure 1: *Collapse of via-hole top metallization*

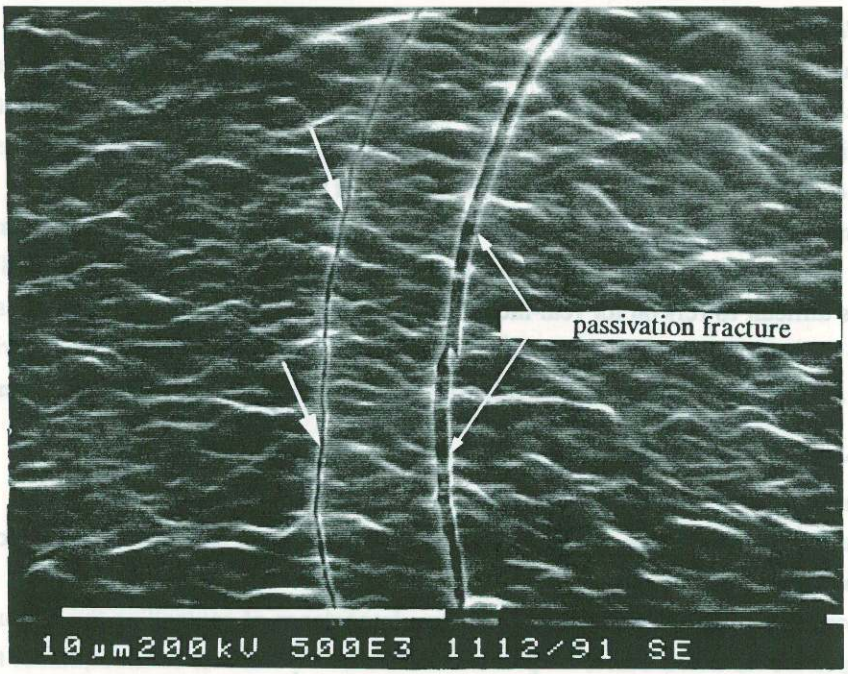

Figure 2: *Close-up of Figure 1 showing passivation fractures*

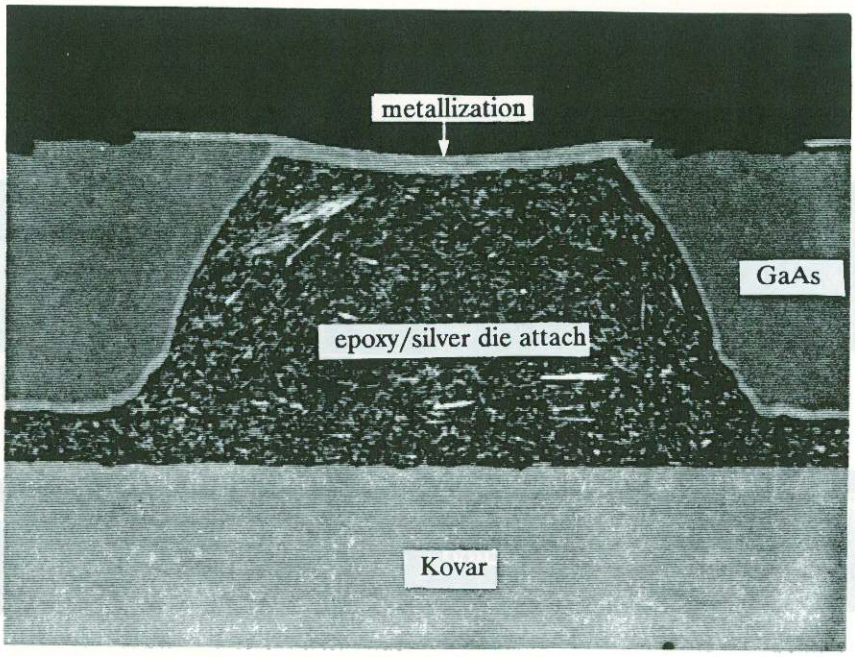

Figure 3: *Cross-section of silver-epoxy filled via-hole*

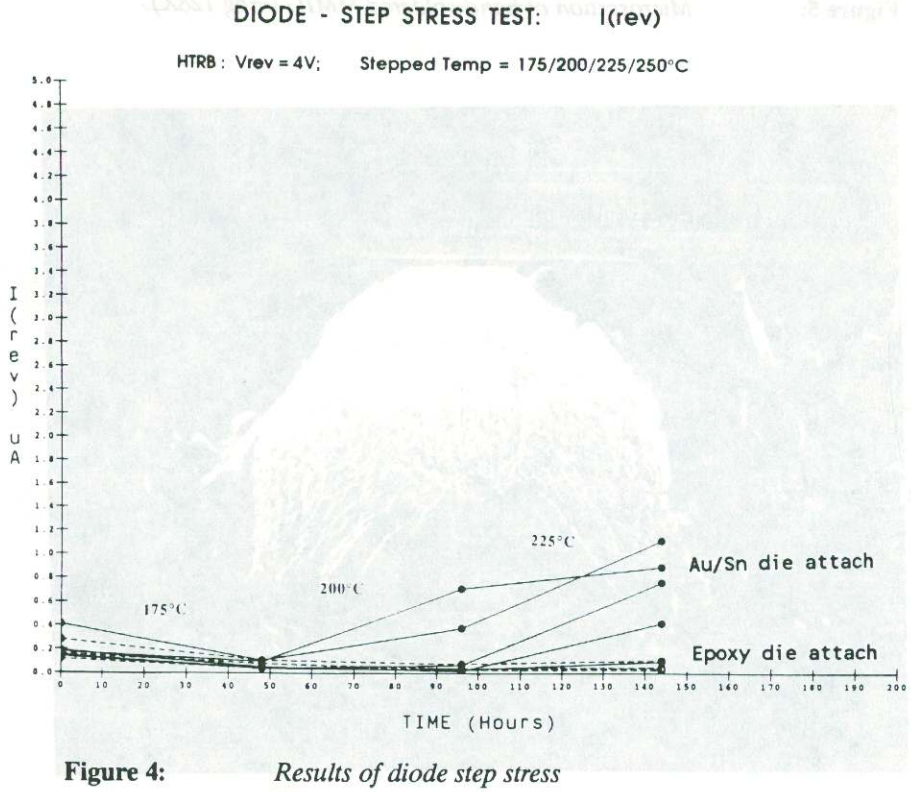

Figure 4: *Results of diode step stress*

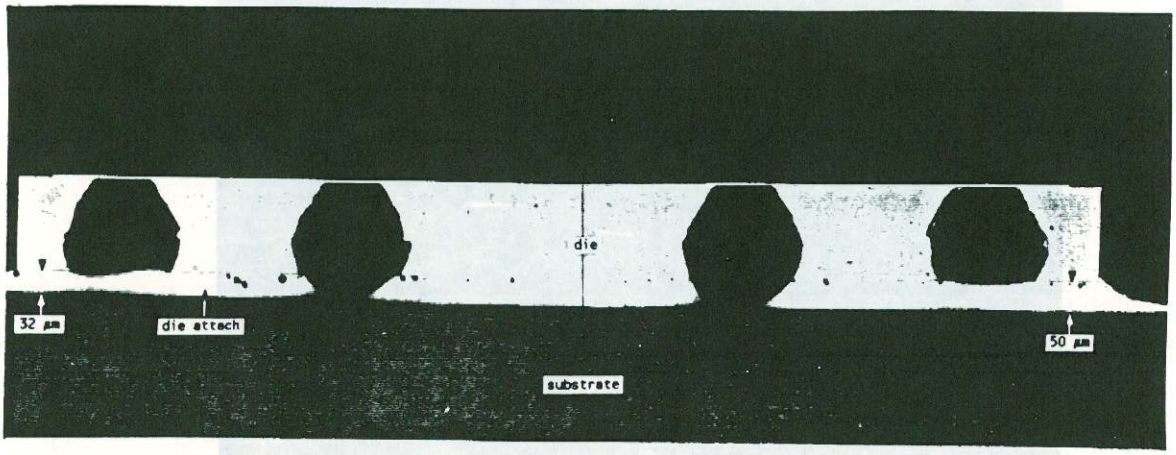

Figure 5: *Microsection of hand-soldered MMIC (mag 128X)*

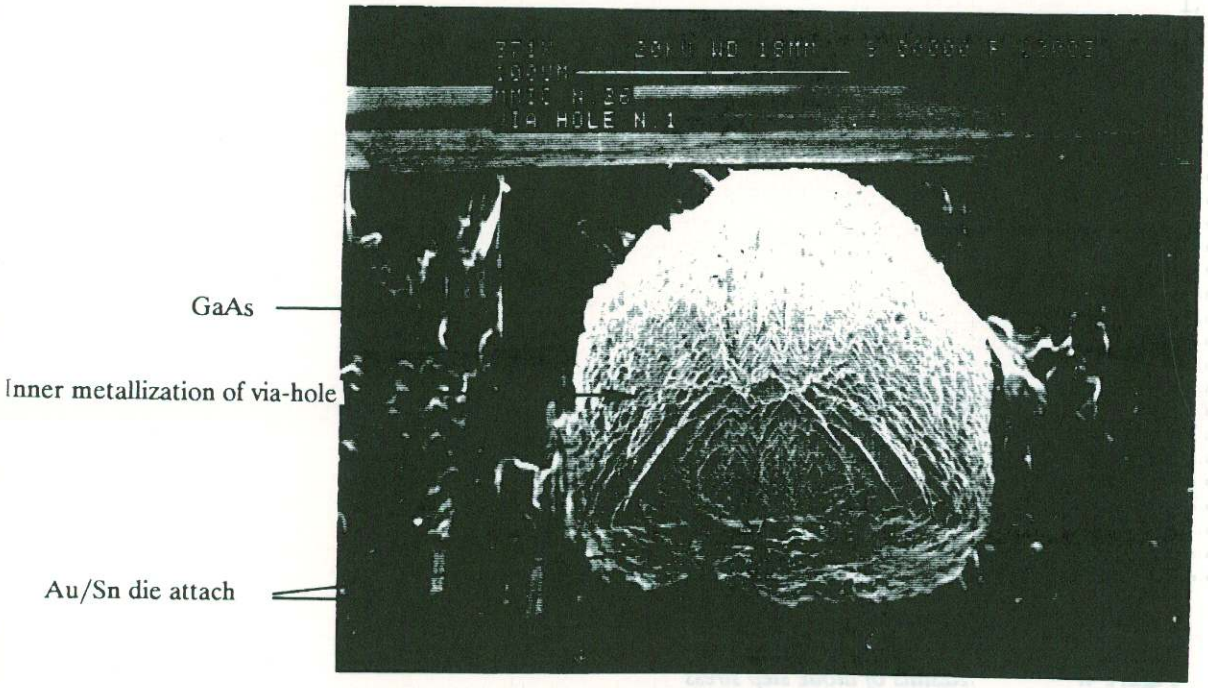

Figure 6: *Microsection of via-hole with no filling by solder*

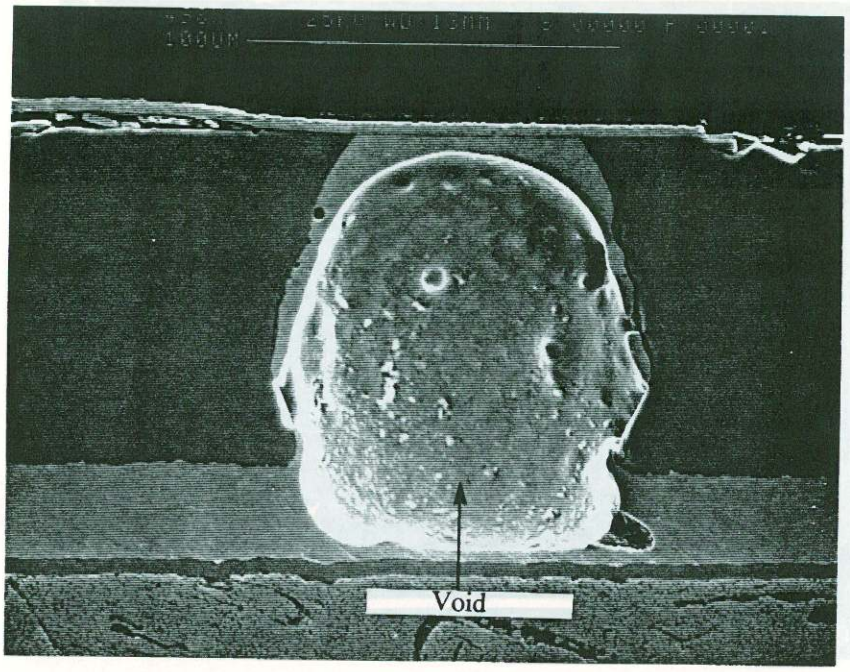

Figure 7: *Microsection of via-hole with partial filling by solder*

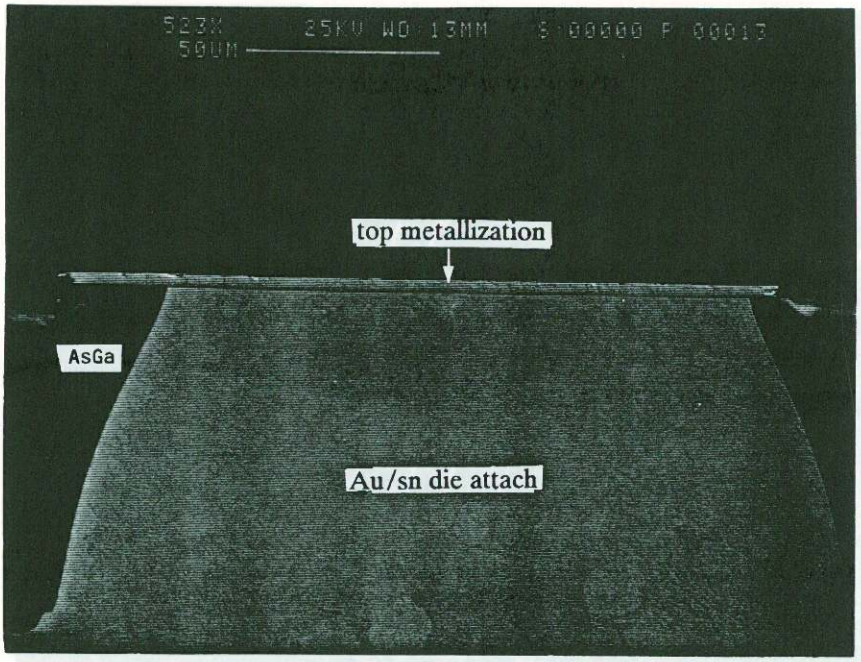

Figure 8: *Micosection of via-hole with complete filling by solder.*

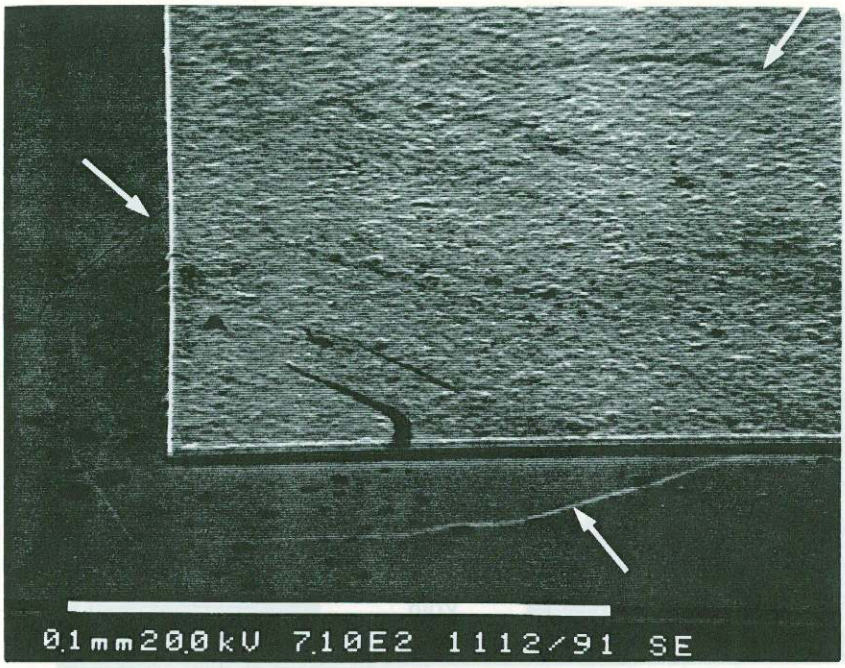

Figure 9: *View of the topside showing GaAs fracture.*

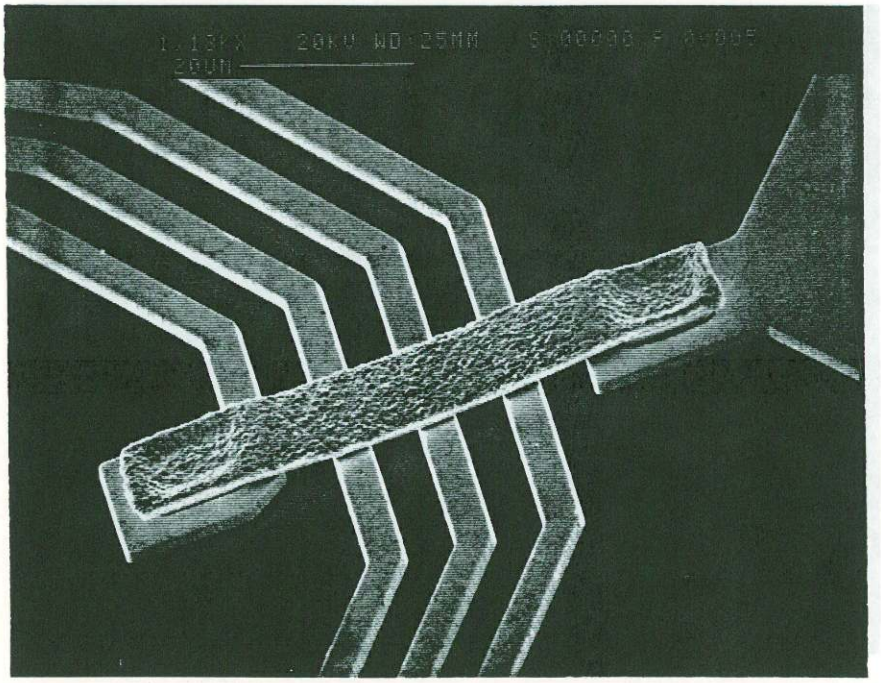

Figure 10: *Air-bridge damaged by mechanical pressure*

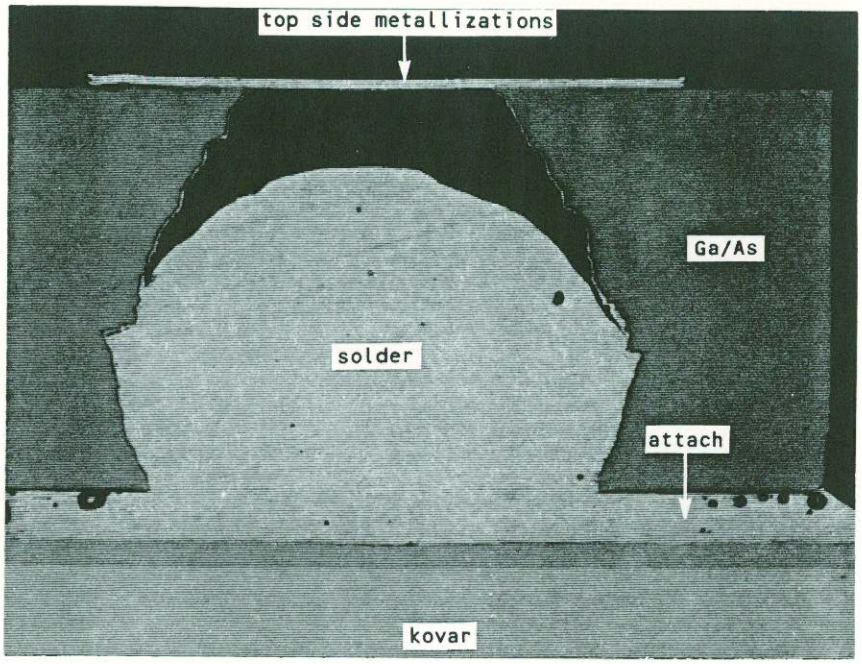

Figure 11: *Microsection of via-hole in MMIC soldered with new process.*

References

1. W.J. Roesch, 1988 : Thermo-Reliability Relationships of GaAs ICs, *GaAs IC Symposium*.
2. Tomimuro et al., 1989 : A new packaging technology for GaAs MMIC modules. *GaAs IC Symposium*
3. Nishigushi et al., 1991: Highly reliable Au-Sn eutectic bonding with background GaAs LSI chips. *IEEE transactions on components, hybrids, and manufacturing technology, Vol. 14, N°3.*
4. Matijasevic et al., 1990 : Void free bonding of large silicon dice using gold-tin alloys. *IEEE transactions on components, hybrids, and manufacturing technology, Vol. 13, N°4.*
5. Pavio & Hyde, 1991 : Effects of coefficient of thermal expansion mismatch on solder attached GaAs MMICs. *IEEE MTT-S Digest.*
6. Lee & Matijasevic, 1989: Highly reliable die attachment on polished GaAs surfaces using gold-tin eutectic alloy. *IEEE transactions on components, hybrids, and manufacturing technology, Vol. 12, N°3.*
7. Wang & Lee, 1991: A bonding technique for thin GaAs dice with via holes using gold-tin composites. *IEEE transactions on components, hybrids, and manufacturing technology, Vol. 14, N°4.*
8. Matijasevic & Lee, 1989: A reliability study of Au-Sn eutectic bonding with GaAs dice. *Proceedings of the IEEE reliability physics symposium.*