DESIGN AND REALIZATION OF 20 GHZ DISTRIBUTED AMPLIFIER MMICS

Hartmut Kapusta, Ewald Pettenpaul, Andreas Weisgerber (*)
Ingo Wolff (**)

Abstract

A distributed amplifier design and optimization program has been developed and used to design a family of broadband distributed amplifiers up to 20 GHz. The program is a fast and accurate CAD tool.Simulation, layout and process are described and on-chip measurement results are presented. The realized demonstrators show a high level state-of-the-art performance.

1. Introduction

The distributed amplifier MMICs discussed in this paper are of interest for mulitoctave broadband applications offering gain flatness, high return loss, and high stability. The principle of distributed amplifiers is based on the idea of absorbing the bandwith limiting input and output capacitors of the transistors into artificial transmission lines. This compensation technique ist not only restricted to microwave amplifiers but also of growing interest for attenuators, phase shifters and mixers. The multipurpose application possibilities of the broadband distributed circuit principle together with the use of enhanced devices (SAG MEFETs, HEMTs, cascoded FETs) will result in future in further performance improvement and in consequence in an increased importance.

2. Software

Especially for the design of distributed amplifiers a user-friendly menu driven FORTRAN program called DAMP

(*) SIEMENS AG, Semiconductor Group
Balanstr. 73, 8000 Munich 80, FRG
(**) ArguMens GmbH, Bismarckstr. 67, 4100 Duisburg, FRG

(Distributed AMPlifier) has been developed. The field effect transistor is described by an equivalent circuit which is derived from microwave S-parameter measurements without using optimization routines by applying an intelligent measurement strategy. The design program package is a menu driven program which may be used as a stand-alone program but which is also prepared to be used as a special option of other general microwave circuit design programs.

An arbitrary number of stages may be asssumed in the distributed amplifier, the field effect transistors which are used in the amplifier have not to be equal in their properties, arbitrary transistors with different parameters can be used without any restrictions. Gate- and drain-lines as well as the transistor drain connection lines may be defined by the operator. Microstrip line technique is used normally, other line techniques can be implemented easily. Losses and line discontinuities are considered in the design process, so e. g. the needed microstrip T-junctions are described by efficient and accurate CAD models which can be applied over a wide frequency range.

The program package has the optional possibility to optimize the amplifier circuit in the sense that e. g. the network parameter for a wanted gain characteristic or minimum reflection coefficient or even for both together are found using an optimization routine. The lengths and widths of the different used line sections as well as the line loads are considered in the optimization process.

3. Electrical Design and Layout

Using the DAMP - program four different distributed amplifiers have been designed for the bandwidths 15, 18 (2 x) and 22 GHz. Common design goals were VSWR <= 2:1, gain as high as possible and flat in the regarded band. By tuning the gate widths the gain was maximized for each amplifier to achieve the best tradeoff between gain and bandwidth. Extending the bandwidth above 18 GHz based on present state of technology is possible only with compromises in the gain. To fulfil gain demands beyond 8 dB two stage versions have been added. Table I is an overview of the studied DAMPs.

#	fmax	#FETs	#gates	width um	length um	process	stages
1	18	4	6	35	Ø.3	EBL	1
2	22	4	4	4Ø	Ø.3	EBL	1 and 2
3	15	4	4	5Ø	Ø.8	DIOM	1
4	18	4	4	45	Ø.3	EBL	1 and 2

Table I: Realized distributed amplifiers

The layout (example see Fig. 1) is compatible to CASCADE on-wafer measurements. Passive components are realized using microstrip lines of different characteristic impedances, MIM capacitors, CrNi thin film resistors, plated gold air-bridges and substrat via holes. The realized mask set is an experimental one. Test precautions are provided generously. Key components are placed on each chip as process control monitors (PCM) so that technological parameters may be determined even after dicing hardly effected by parameter deviations across the wafer. The single FETs provided with CASCADE footprints have been placed onto each chip too with appropriate gate width. So the FETs' S-parameters can be measured even after chip dicing separately.

4. Process

The 18 and 22 GHz amplifiers are designed to be realized with our enhanced Ø.3 um E-Beam high performance process (ft = ~3Ø GHz), while the 15 GHz amplifier was manufactured using the Ø.8 um standard DIOM *) process (ft = ~15 GHz). The technology was performed using a 3"-wafer process based on ASET I-line stepper lithography. Only the Ø.3 um gates were written with a Philips Electron Beam Pattern Generator.

Doping was done by ion implantaion. EBL-FETs are additionally doped by Be+ (p-buried layer) besides the

---

*) DIOM (Double Implantation One Metalization)
a cost effective self aligned FET process

common n-type Si implant; this improves the transconductance significantly. EBL-type FETs are processed using recess gate technology, while DIOM-type FETs have an unrecessed channel. MIM dielectric as well as passivation consist of photo-enhanced SiN layers.

Air-bridges and passive elements are made of 5 um plated gold. Substrate via holes are used in 100 um thick substrates.

5. Measurements

The measurements have been performed using a CASCADE on wafer measurement system and a hp 8510 network analyzer. Table II shows an overview of the characteristics.

DAMP #	bandwidth (designed) GHz	bandwidth (verified) GHz	s11 dB	s22 dB	s21 dB
1	2 - 18	2 - 18	8	10	8.1 +-0.9
2	2 - 22	2 - 19*)	8	12	6.2 +-0.8
3	2 - 15	2 - 16	11	13	4.8 +-0.4
4	2 - 18	2 - 18	8	11	7.8 +-0.8

Table II : Measured characteristics of distributed amplifiers
(*) restricted by measurement setup)

The results closely agree to the simulations (Fig. 2 and 3). The S-parameters of all the four amplifiers are shown in Fig. 4. The frequency limit for reliable data was restricted by the measurement system at that time to 19 GHz. Measurements beyond that point should only be regarded as clues for extrapolation. The gain ripple of the EBL - type DAMPs and the input VSWR are higher than calculated. There are two reasons for these deviations. The first is that the realized FETs did not reproduce the simulated ones exactly. The second one is that the realized load resistances deviate from the simulated ones by + 20 %. Reproducing runs have shown that the matching can be improved.

Two stage versions of the DAMPs have shown that the amplifiers can be cascaded.

6. Summary

A fast and user-friendly CAD program for the design and optimization of distributed amplifiers has been developed. Experimental verification showed good accordance between simulation and on-wafer measurement up to at least 20 GHz.

Note

This work has been supported by the European Community ESPRIT Research Project. The authors alone are responsible for the contents.

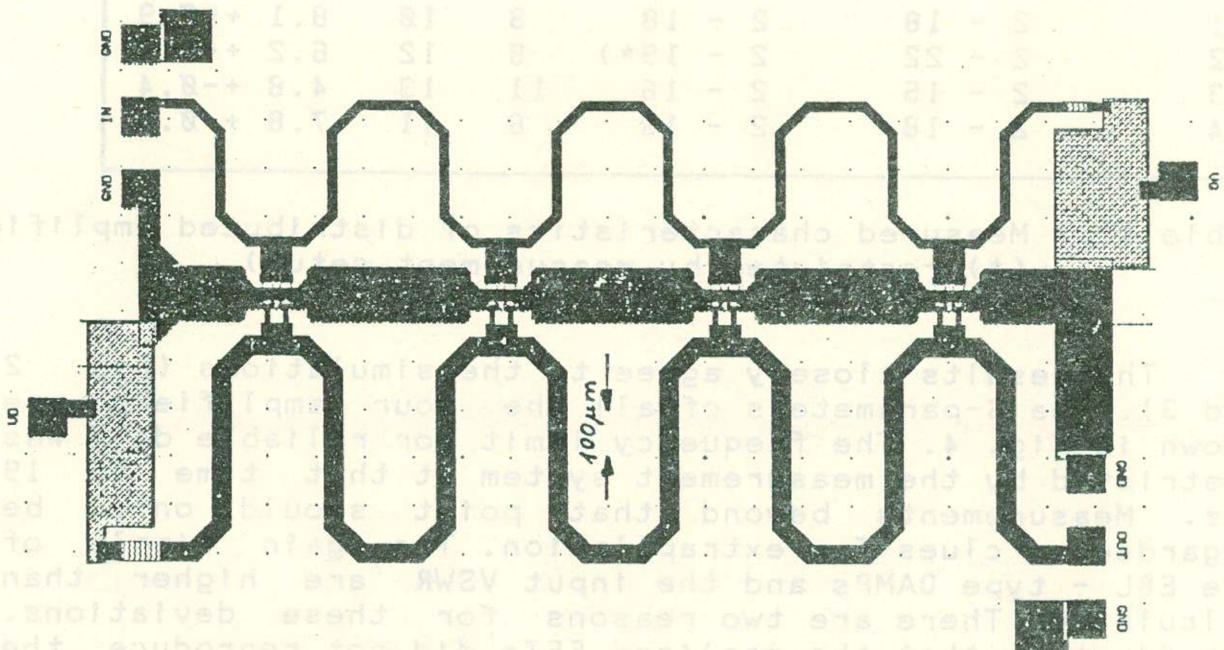

Fig. 1: Layout of distributed amplifier #4

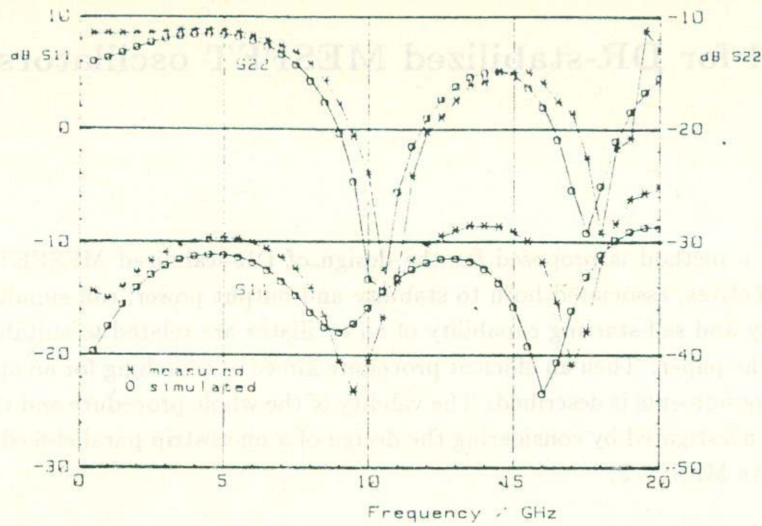

Fig. 2: Comparison between simulated and measured reflection coefficients (DAMP #4)

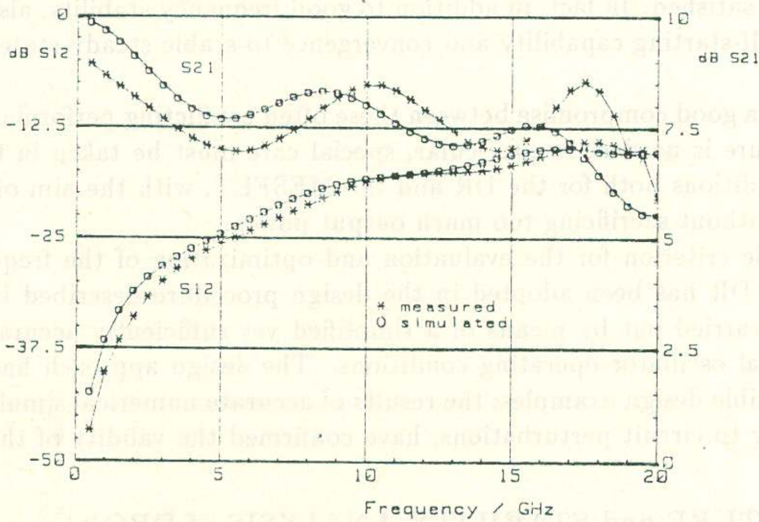

Fig. 3: Comparison between simulated and measured transmission coefficients (DAMP #4)

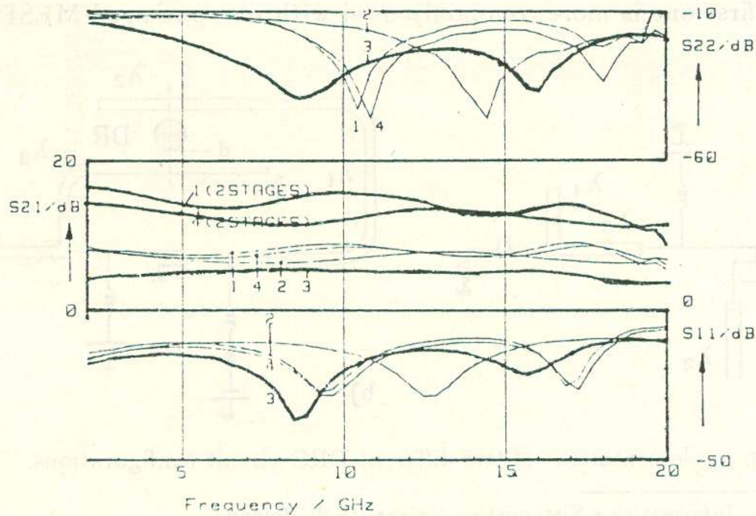

Fig. 4: Measured properties of distributed amplifiers