A PHYSICAL SIMULATOR FOR THE EXTRACTION OF MESFET CIRCUIT MODELS

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Abstract

We present a 2-D physical simulator intended for the computer-aided-design of GaAs MESFETs. Numerical schemes for DC and small-signal analysis are briefly described. Small-signal simulation of a submicron device is compared with on-wafer measurements.

Introduction

Two dimensional physical simulation has been traditionally used to have a better insight into the device operation and to study the effect of different parameters over its final performance [1-4]. Results reported so far are, however, more qualitative than quantitative and one can not find many comparisons between simulated and measured results in the literature, specially at high frequency.

In the last years there is a growing interest in obtaining accurate predictions through physical simulation, so that it can be used for the design, optimization and even characterization of devices. This is a great deal motivated by the present impact of MMICs.

There are two basic requirements that a practical CAD-oriented simulator should meet: First, it has to use physical models that can accurately describe the device operation and whose model parameters can be easily evaluated. Secondly, it has to use reliable and efficient numerical schemes capable of a fast and free from numerical problems analysis.

We have developed our simulator trying to meet these two key points. Concerning the physical model we consider that the classical drift-diffussion model is the most suitable for the aforementioned purpose, since its model parameters have been intensively studied and it can be much more efficiently solved than other more sophisticated models. Though it is generally accepted that non-stationary effects can play an important role in devices showing submicron features, it is also a fact that devices fabricated with standard foundry processes do not seem to show these effects in a clear form. It seems, therefore, much more practical to introduce these effects, if necessary, through the inclusion of effective parameters (such as an effective saturation velocity).

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The physical model

Figure 1 shows the typical structure of a recessed-gate MESFET along with the simplified geometry used for the simulation. The analysis can be constrained to the inside of the rectangular domain, provided that we can neglect the effect of the external coupling between electrodes over the internal field distribution. In order to properly account for the effect of the impurity profile the analysis domain should include a considerable thickness of the semi-insulating substrate. The gate-recess is modeled through an equivalent surface charge at both sides of the gate as proposed in [3]. Thus, the same geometry is valid for gate-recessed and self-aligned technologies.

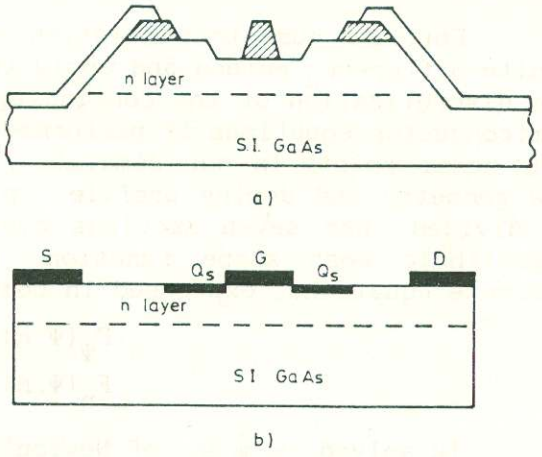

Fig. 1. a) Structure of a recessed-gate MESFET and b) geometry used for the simulation

Electron dynamics in the bulk semiconductor are described by Poisson and electron current continuity equations

$$\varepsilon\varepsilon_o\Delta\Psi - q(n-N_d+N_A) = 0 \qquad (1)$$

$$\nabla J_n + \frac{\partial n}{\partial t} = 0 \qquad (2)$$

with

$$J_n = \mu_n n\nabla\Psi - D_n\nabla n \qquad (3)$$

where all symbols have their usual meaning. The dependence of electron mobility on the electric field in GaAs is described by the well-known empirical relationship

$$\mu(E)E = \frac{\mu_o E + v_{sat}(E/E_o)^4}{1 + (E/E_o)^4} \qquad (4)$$

being $v_{sat} \cong 10^5$ m/s and $E_o \cong 4$KV/cm. The low-field mobility μ_o is a function of the net impurity concentration $C=N_d+N_A$ and the temperature. We model this dependence through the empirical formula

$$\mu_o = \frac{\mu_{oo}}{1 + \left(\frac{\log(C+1)}{B}\right)^n} \left(\frac{300}{T}\right)^{\alpha} \qquad (5)$$

where μ_{oo} is the mobility of the intrinsic semiconductor and T is the temperature in °K. The dependence with C is of the form suggested by Abusaid and Hauser [4] and fits very well to empirical data. We have evaluated n=12.53 and B=17.15 for μ expressed in $m^2/V\,s$ and C in cm^{-3}.

Numerical schemes

For the numerical solution of the problem we make use of the finite-difference method and apply the Scharfetter-Gummel approach [5] in the discretization of the continuity equation. The discretization of the semiconductor equations is performed on a non-uniform rectangular grid of NxNy nodal points. In our simulator, the mesh is generated according to the geometry and doping profile. In the horizontal dimension the device is divided into seven seccions over which the mesh is conformed by a logarithmic mesh shape function. The resulting non-linear system of discrete equations, expressed in compact form as

$$\begin{aligned} F_{\Psi}(\Psi, n) &= 0 \\ F_{n}(\Psi, n) &= 0 \end{aligned} \qquad (6)$$

is solved by means of Newton's method

$$\begin{bmatrix} \frac{\partial F_{\Psi}}{\partial \Psi} & \frac{\partial F_{\Psi}}{\partial n} \\ \frac{\partial F_{n}}{\partial \Psi} & \frac{\partial F_{n}}{\partial n} \end{bmatrix}^{k} \begin{bmatrix} \delta\Psi \\ \delta n \end{bmatrix}^{k+1} = -\omega \begin{bmatrix} F_{\Psi} \\ F_{n} \end{bmatrix}^{k} \qquad (7)$$

where $\delta\Psi^{k+1} = \Psi^{k+1} - \Psi^{k}$ and ω is a relaxation parameter. We have also implemented Gummel's uncoupled scheme. However, we have seen that, despite of doubling the order of the system, Newton's method becomes clearly more efficient when the exact Jacobian is calculated. In order to more efficiently perform the analitical calculation of the Jacobian we do not interpolate the diffusivity at the midpoints as it is usually done [6], but calculate it as

$$Dn_{i+1/2,j} = Dn(E_{i+1/2,j}) \qquad (8)$$

i.e., we interpolate the electric field at (i+1/2, j). With this simple modification we reduce the bandwidth of the Jacobian from $4N_y$ to $2N_y+2$ in a natural ordering by columns. To compute a new bias point (with typical voltage steps of, say, 0.5V in V_{ds} or 0.1V in V_{gs}) will thus normally require only one factorization and 10-15 backward substitutions to achieve a maximum error $\|\delta\Psi\|_{i} = 10^{-5}$.

The small-signal analysis is performed using the time-domain linear technique [7]. The discrete system is linearized around the bias point resulting into the small-signal system

$$\begin{bmatrix} \frac{\partial F_{\Psi}}{\partial \Psi} & \frac{\partial F_{\Psi}}{\partial n} \\ \frac{\partial F_{n}}{\partial \Psi} & \frac{\partial F_{n}}{\partial n} \end{bmatrix} \begin{bmatrix} \tilde{\Psi} \\ \tilde{n} \end{bmatrix} = \begin{bmatrix} B^{\Psi} \\ B^{n} \end{bmatrix} \qquad (9)$$

where the vector B contains the boundary conditions in space and time. By applying voltage steps $v_j = \Delta v_j u(t)$ to the device ports and solving the linear transient with (9) the admittance matrix can be calculated as

$$Y_{i,j} = \frac{1}{\Delta v_j} \left[i_i(\infty) + jwF\{ i_i(t) - i_i(\infty) \} \right] \qquad (10)$$

In solving the transient response the Jacobian needs only be evaluated when the time step is changed. Since the first time steps have to be very small (1-10fs) in order to reproduce a sharp current spike, an optimum number of 4-5 factorizations are typically required for a minimum computational cost. The accuracy in the frequency resolution depends on the transient resolution. In our computations, 300 to 400 time steps are normally required to estimate the transition frequency with 1% accuracy.

Analysis of a submicron MESFET

We have tested the simulator with a MESFET of our own fabrication. A gate length of 0.35μm and 0.15μm of recessed length at each gate side were measured with a SEM. The GaAs substrate had no compensation and the doping profile (fig.2) shows a peak concentration of $10^{18}cm^{-3}$, aproximately. Figure 3 shows the mesh generated by the simulator and the two-dimensional potential for bias conditions V_{ds}=2V and V_{gs}=0.2V. Since we had no precise knowledge about the surface potential it was "tuned" to fit the DC data. It was estimated to be $\Phi_s \cong 0.45V$.

Simulated S-parameters and on-wafer measurements up to 15GHz for a device with a gate width W=2x50μm are shown in fig.4. In order to correctly compare measurements and simulations the small-signal equivalent circuits were optimized with the TOUCHSTONE program. After de-embedding the intrinsic elements from measurements, the agreement with the simulation is very good as can be seen in Table I.

These first results are very encouraging. However, further effort concerning device characterization and more intense simulations have still to be done to confirm the real utility of the simulator.

TABLE I

Intrinsic elements obtained from measurements and simulations

	g_m (mS)	C_{gs} (pF)	C_{gd} (pF)	R_i (Ω)	R_{ds} (Ω)	τ_o (pS)	f_T (GHz)
Meas.	27.1	0.127	0.011	2.96	358	2.11	33.9
Simul.	26.9	0.120	0.011	3.00	400	1.84	35.7

Aknowledgements

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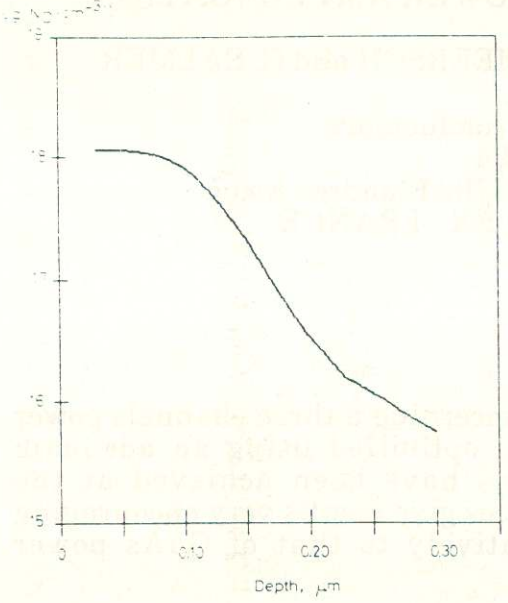


Fig.2. Doping profile of the simulated MESFET

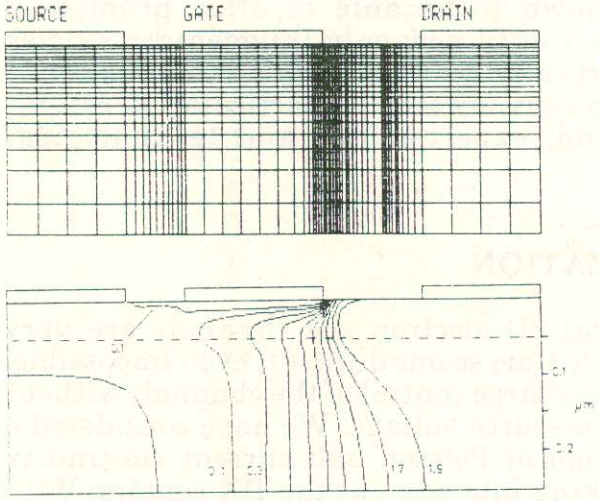


Fig.3. Generated mesh (59x24 nodes) and equipotential curves for bias conditions V_{gs}=0.2V and V_{ds}=2V.

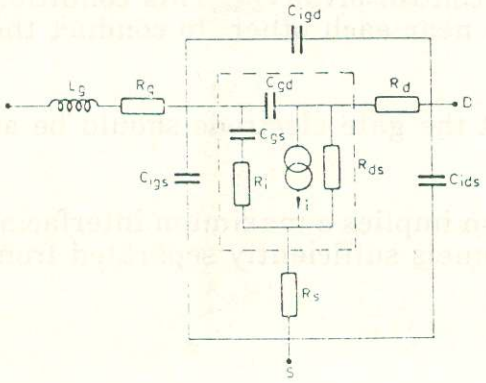
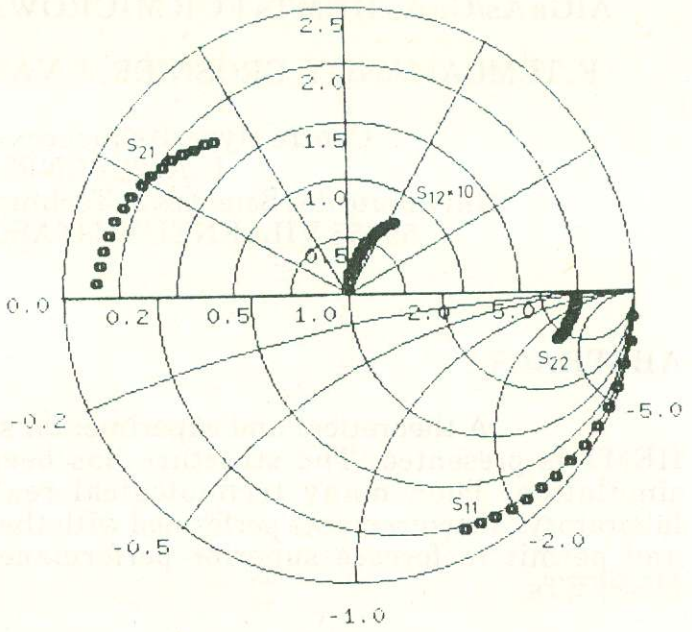
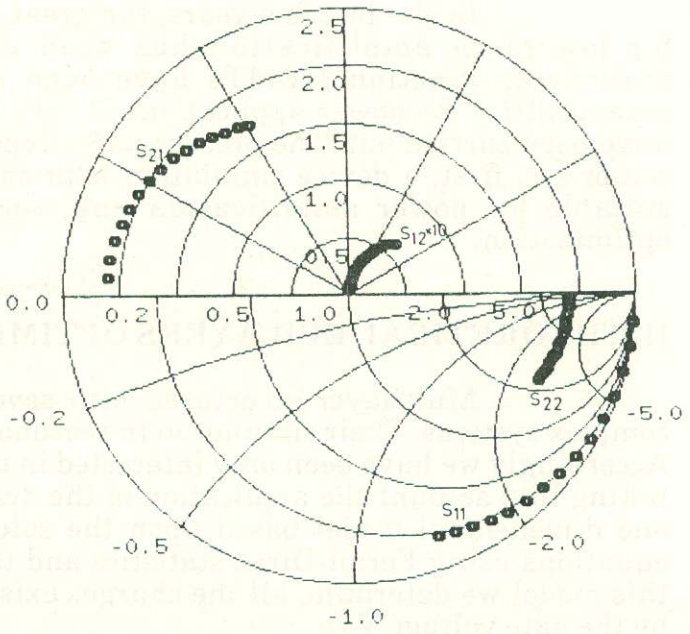


Fig.5. Small-signal equivalent circuit of the MESFET. The intrinsic elements are enclosed by the dotted lines



a)



b)

Fig.4. a) Simulated and b) on-wafer measured S-parameters from 1 to 15 GHz