# THERMAL MODELS FOR LOW- AND HIGH-POWER GAAS MESFET DEVICES

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**Abstract.** *The paper addresses the problem of thermal design of MESFET devices. Two CAD models are proposed for performance evaluation: a closed-form thermal resistance model and a two-dimensional self-consistent coupled physical model. The two models are complementary and allow both to optimize the geometry and to correctly estimate the small-scale temperature distribution and the influence of heating on the electrical performances. Results from both models are discussed and compared with measurements.*

## Introduction

Form the standpoint of MESFET design, the assessment of thermal performances is important under several respects. First, the average operating temperature of the device must be kept under acceptable limits, i.e. the device *thermal resistance* must be suitably low. This goal can be usually achieved through proper layout rules and choice of the substrate thickness. However, such a geometrical optimization is not necessarily straightforward in complex, multi-gate devices, since the large-scale, 3D heat simulation of a multi-gate MESFET is still a formidable and CPU intensive task when performed in 3D through a finite-element based simulator.

A second important parameter is the small-scale *temperature distribution* on the active region, in particular the peak temperature, which affects the device lifetime and reliabilty. Finally, an estimate of the influence of device heating on the *electrical* (DC and small-signal) performances should be available. Neither information can be derived from a thermal resistance model, whose spatial resolution is intrinsecally low and which is not self-consistent, i.e. does not account for the feedback existing between thermal and electrical phenomena.

In order to provide a complete CAD tool for MESFET thermal design, two models are proposed. The first is a self-consistent, two-dimensional model coupling the drift-diffusion and heat equation [3,5,6]. Such a model can provide the self-consistent temperature distribution on the active region and the DC and AC parameters in non-isothermal conditions. The second model is a closed-form thermal resistance model for multi-gate MESFETs, which allows geometry optimization to be performed at low computational cost. Since in the self-consistent model the large-scale heat flow is accounted for through equivalent distributed thermal resistances connected to the periphery of the simulated region [3,5,6] the two models are coupled.

The paper is structured as follows. First, a complete closed-form model for the thermal resistance of multi-gate backside-mounted MESFETs is discussed. Details on the self-consistent model can be found in [3,5,6] and are omitted here for the sake of brevity. Then, the thermal resistance model is used to analyze the thermal behaviour of both conventional and air-bridge TELETTRA devices, and comparisons with measurements are carried out. Finally, DC data obtained from the self-consistent physical model are compared with measurements.

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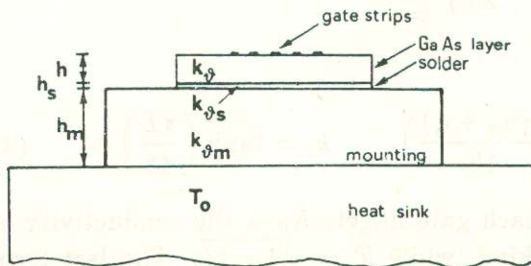


Figure 1: Structure of multigate back-side-mounted MESFET with mounting and solder layer geometry.

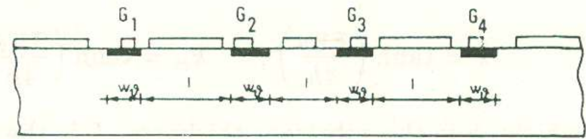


Figure 2: Characteristic thermal parameters of MESFET first-order cell

## Thermal resistance of multi-gate MESFETs

Thermal resistance models of MESFETs [1, Ch.5] are based on the assumption that a hot, isothermal strip lies on the device surface, whereas the rest of the device is free from heat sources [1]. Concerning the width $w_\theta$ of the strip-like hot spot into which thermal power is injected, it has been shown (see e.g. [1]) that, for a given geometry, the best agreement with measurements occurs for $w_\theta = 8\ \mu$m in a 1 $\mu$m device. In contrast with this, the self-consistent simulation yields a considerably smaller width (1-2 $\mu$m). The discrepancy can be explained from the intrinsically averaged nature of temperature measurements. In fact, owing to the lack of spatial resolution, measurements tend to *underestimate* the peak temperature; as a consequence, the parameter $w_\theta$ which should physically correspond to the width of the hot spot (1-2 $\mu$m), actually refers to a wider region, roughly encompassing the source-drain spacing. In order to provide closed-form approximations, the overall thermal resistance of a MESFET is segmented into three series contributions: the GaAs layer, the solder layer, and the mounting. All contributions can be approximated, taking into account 3D effects, with analogy to the theory of stripline resonators.

High-power multi-gate MESFETs usually are a periodic structure obtained by assembling several lower-order cells, i.e. one starts from a first-order cell made by $N_1$-gates, with $N_1$ equispaced "hot strips" of width $w_\theta$ at a distance $l_1$ (corresponding to the spacing between gate sides, see Fig.2), and assembles $N_2$ first-order cells into a second-order cell by putting them side-to-side at a distance $l_2$. From $N_3$ second-order cells a third-order cell can be obtained, with cell-to-cell spacing $l_3$, and so forth. If $M$ is the order of the maximum order cell, the total number of gate strips is $N = \prod_{j=1}^{j=M} N_j$.

The temperature-dependent thermal resistance of the device can be defined as

$$R_\theta(T_2, T_0) = (T_2 - T_0)/P \tag{1}$$

where $T_0$ is the heat sink temperature, $P$ the dissipated power, and $T_2$ is the channel temperature, obtained through Kirchhoff trasformation [7]:

$$T_2 = T_1 + [0.74(\tau_2 - T_1)T_1^{-0.26} + T_1^{0.74}]^{1/0.74} \tag{2}$$

$\tau_2 = T_1 + P/G_\theta$ is the apparent active region temperature. $G_\theta$ is the GaAs layer thermal conductance:

$$G_\theta = LK_\theta \left\{ 2\left[2 - \prod_{i=1}^{i=M} N_i\right] \frac{K(k)}{K(k')} + 4 \sum_{i=1}^{i=M-1} (N_i - 1) \frac{K(k_{ei})}{K(k'_{ei})} \prod_{j=i+1}^{j=M} N_j \frac{K(k)}{K(k')} + \right.$$

[1]The temperature distribution is therefore supposed to be (at least approximately) *uniform* along the gate strips and between neighbouring gates; an extension of the thermal resistance concept to the case wherein strong temperature dis-uniformities arise between neighbouring gates or along the gate fingers (thermal resistance matrix model and distributed thermal resistance model) is discussed in [5,6].

$$
\left. 4(N_M - 1)\frac{K(k_{eM})}{K(k'_{eM})}\right\} + 2w_\theta K_\theta \left\{\frac{K(k_\delta)}{K(k'_\delta)} - \frac{L}{2h}\right\} \prod_{i=1}^{i=M} N_i \tag{3}
$$

where:

$$
k = \tanh\left(\frac{\pi w_\theta}{4h}\right), \qquad k_{ei} = \tanh\left(\frac{\pi w_\theta}{4h}\right)\tanh\left(\frac{\pi(w_\theta + l_i)}{4h}\right), \qquad k_\delta = \tanh\left(\frac{\pi L}{4h}\right) \tag{4}
$$

in which: $h$ is the substrate thickness, $L$ is the length of each gate finger, $K_\theta$ is the conductivity of GaAs. $K(k)$ is the complete elliptic integral of the first kind, while $k' = \sqrt{1-k^2}$. The last term between curl brackets in (3) refers to the fringing thermal conductance of the gate tips.

The solder temperature $T_1$ can in turn be evaluated as $T_1 = T_0 + R_1 P$, where $R_1 = 1/G_{\theta s} + 1/G_{\theta m}$. $G_{\theta s}$ is the thermal conductance of solder, which can be approximated as a simple parallel-plane contribution:

$$
G_{\theta s} \approx \frac{W_{ts} L_s}{h_s} K_{\theta s} \tag{5}
$$

with parameters:

$$
W_{ts} = W_s \prod_{i=2}^{i=M} N_i, \qquad W_s = N_1 w_\theta + (N_1 - 1) l_1 + 2h, \qquad L_s = L + 2h. \tag{6}
$$

$W_{ts}$ is the equivalent solder total width, while $W_s$ is the equivalent solder width for each first-order section, including fringing effects from the GaAs layer. $L_s$ is the equivalent solder length.

The conductance of the *mounting* can be expressed again with reference to the capacitance of a set of rectangular patches (the bottom of the solder layer for each first-order section) on a dielectric layer. The resulting expression is similar to the one of the GaAs layer, only all summations start from the second-order sections:

$$
\begin{aligned}
G_{\theta m} = \; & K_{\theta m}\left\{ L_s \left[ 2\left(2 - \prod_{i=2}^{i=M} N_i\right)\frac{K(\kappa)}{K(\kappa')} + 4\sum_{i=2}^{i=M-1}(N_i - 1)\frac{K(\kappa_{ei})}{K(\kappa'_{ei})}\prod_{j=i+1}^{j=M} N_j \right.\right. \\
& \left.\left. + 4(N_M - 1)\frac{K(\kappa_{eM})}{K(\kappa'_{eM})}\right] + 2W_{ts}\frac{K(\kappa_1)}{K(\kappa'_1)} - \frac{W_{ts} L_s}{h_m}\right\}
\end{aligned} \tag{7}
$$

where:

$$
\kappa = \tanh\left(\frac{\pi W_s}{4h_m}\right), \qquad \kappa_{ei} = \tanh\left(\frac{\pi W_s}{4h_m}\right)\tanh\left(\frac{\pi(W_s + l_i - 2h)}{4h_m}\right), \qquad \kappa_1 = \tanh\left(\frac{\pi L_s}{4h_m}\right) \tag{8}
$$

$h$ is the substrate thickness, $h_m$ is the mounting thickness, and $K_{\theta m}$ is the thermal conductivity of mounting.

In order to correctly implement the formulae (3) and (7) one should notice that they hold, as they are written, for $M \geq 2$ and for $M \geq 3$, respectively. Instead of deriving particular, simpler forms for lower values of $M$, it is easier to note that a structure described by $M = 1$ can be equivalently interpreted as a structure with $M = 3$, $N_2 = 1$, $N_3 = 1$. When $N_i = 1$ the distance between $i$-th order blocks is of course immaterial. Similarly, for $M = 2$ one can put $M = 3$, $N_3 = 1$. Thus, the particular cases for $M < 3$ are reduced to the case in which expressions (3) and (7) hold.

Examples of computed thermal resistances for different geometrical parameters are reported in Fig.3. The results obtained are in good agreement with numerical data computed through FEM and reported in [1, Fig.6, pag.322].

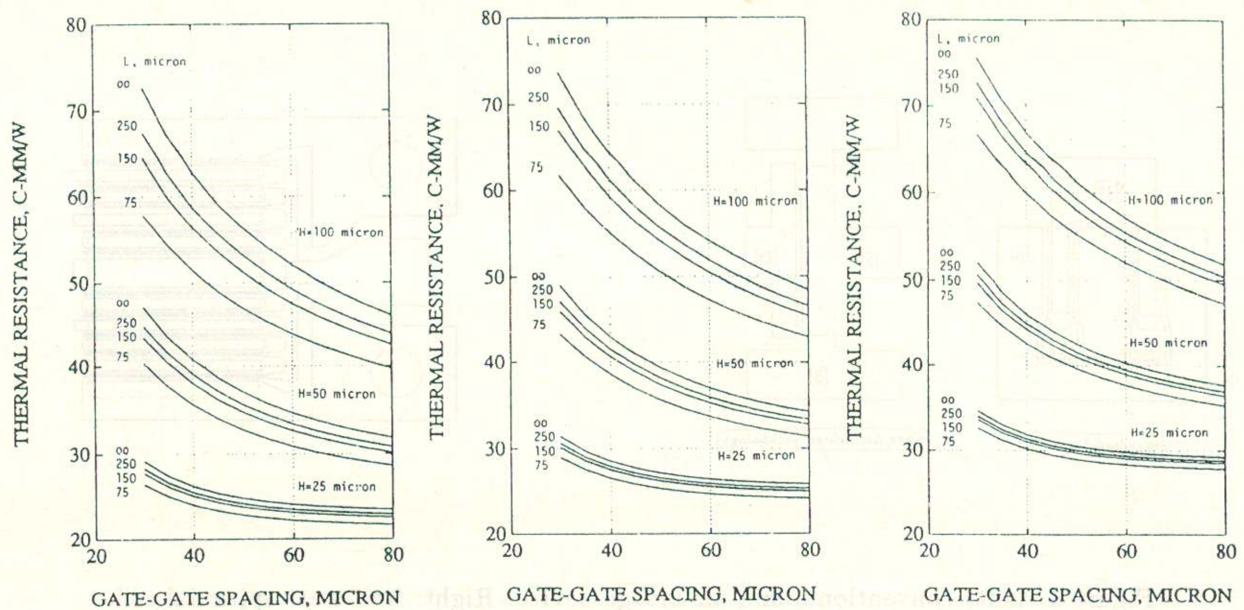


Figure 3: GaAs layer thermal resistance per unit length as a function of geometrical parameters; the GaAs thermal conductivity is evaluated at 60°C. Left: $w_\theta = 8$ $\mu$m; center: $w_\theta = 6$ $\mu$m; right: $w_\theta = 4$ $\mu$m.

## Comparisons with experiment

The purpose of the present section is to provide comparisons between the models developed and experimental data (TELETTRA). Such data refer to two sets of devices, whose layout is shown in Fig.4: a low-power 300 $\mu$m × 0.5 $\mu$m device realized both in conventional and air-bridge configuration [2] (Fig.4, left) and a set of medium-power backside-mounted wire-bound 1 $\mu$m epitaxial devices realized by putting 2 or 4 standard 10-gate, 0.5 W cells (Fig.4, right) in parallel.

The measured and simulated thermal resistances are compared in Fig.5 for a 0.5 $\mu$m MESFET realized both in conventional ana gate-airbridge configuration. The dissipated power is around 230 mW for the conventional mounting and around 400 mW for the gate-aribridge structure; the measured thermal resistances are 60 and 45 °C/W, respectively. The gate-airbridge device is characterized by a better thermal dissipation, caused above all by the absence of the proximity effect between neighbouring gates. Owing to the simple geometrical structure which makes localized defects less likely to occur this device pair is a good test for the geometrical scaling properties of the model. The best agreement is consistently obtained with values of $w_\theta$ of around 7 $\mu$m. The additional dissipation caused by the airbridge itself is fairly negligible since the bridge is not directly connected to the heat sink.

The multi-cell device is obtained from the assembling of one, two or four TX0253 TELETTRA epitaxial MESFETs. The data relevant to the thermal simulation are reported in Table I. The lenght of each gate finger is 150 $\mu$m, the substrate thickness is 50 $\mu$m; a solder layer thickness of 5 $\mu$m is included in the simulation, although its effect is negligible.

The simulated thermal resistance, as a function of the dissipated power, is shown in Fig.5 (right) for all three kinds of device structures. The dots are the measured data as reported in Table I. Good agreement is obtained for the two- and four-cell device with expected values of $w_\theta$, while for the one cell device, the $w_\theta$ needed to match measurements is slightly higher than expected. In fact, the thermal resistances of the one-, two- and four-cell devices ( $R_{\theta 1}$, $R_{\theta 2}$ and $R_{\theta 4}$ ) should approximately follow the law: $R_{\theta 1} \overset{\approx}{<} 2R_{\theta 2} \overset{\approx}{<} 2R_{\theta 4}$. The one-cell and four-cell devices show a lower resistance than expected (or, conversely, the thermal resistance of the two-cell device is higher than expected). The

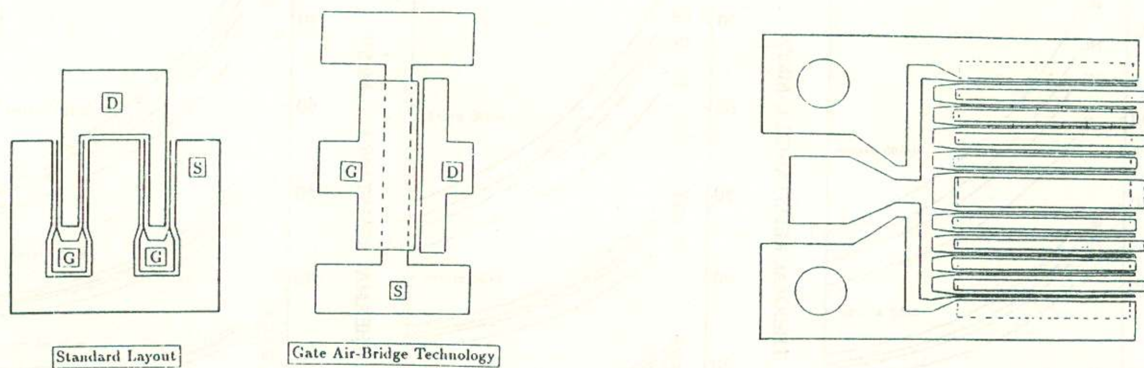


Figure 4: Left: conventional and air-bridge device. Right: half-watt epitaxial cell.

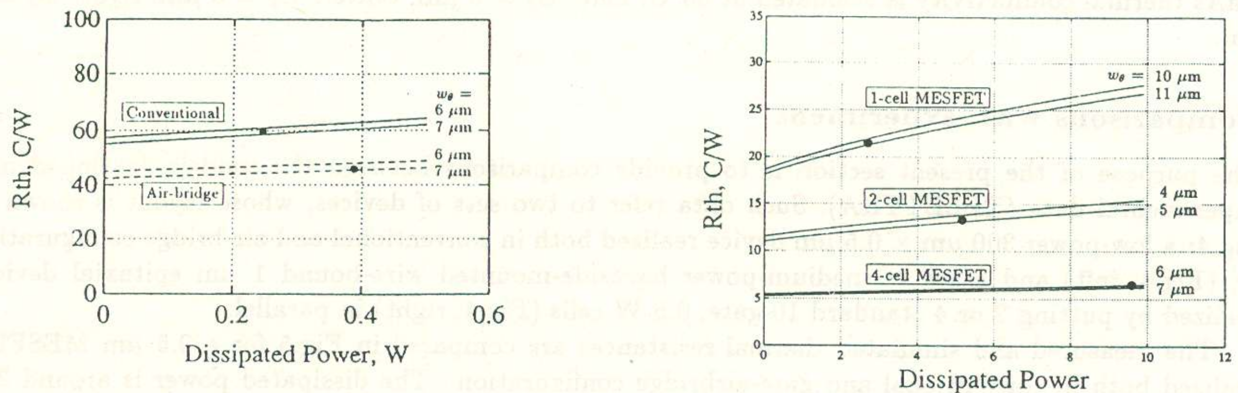


Figure 5: Left: thermal resistance of conventional and air bridge MESFETs. Right: same for 1-, 2-, and 4-cell epitaxial MESFET. Dots are measured data.

discrepancy can be ascribed to the fact that, although all three devices have the same layout, they are not physically the same. The possible occurrence of slight local defect which increase the temperature, more likely to occur in multi-gate structures, can explain why scaling of $w_\theta$ is less successful than for the gate airbridge device, whose topology is considerably simpler.

The comparison of the VI characteristics concerns a single-cell one-micron epitaxial TELETTRA

| | $I_{dss}$ (mA) | $V_{ds}$ (V) | $P_{diss}$ (W) | $R_\theta$ ($^o$C/W) |
|---|---|---|---|---|
| 1-cell device | 336 | 8 | 2.69 | 20.9 |
| 2-cell device | 645 | 8 | 5.16 | 13.5 |
| 4-cell device | 1300 | 8 | 10.40 | 6.4 |

Table 1: Measured thermal resistances for multi-cell device

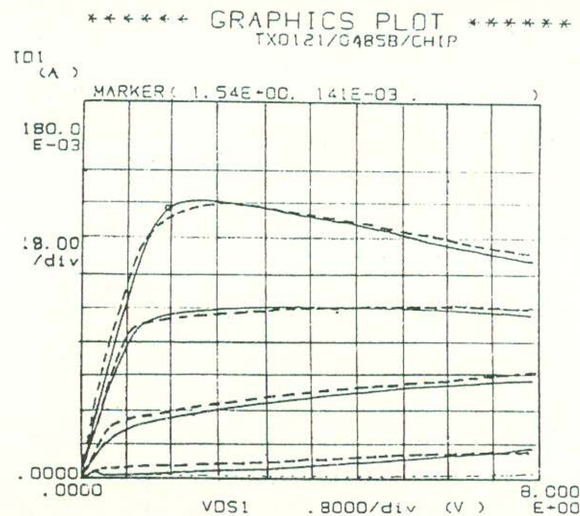


Figure 6: Measured (continuous line) and simulated (dashed line) VI curves of epitaxial MESFET.

device TX0121. The measured (continuous line) and simulated (dashed line) curves are shown in Fig.6. The agreement is good, and in particular the self-consistent model correctly accounts for the downward bending of the drain characteristics for low gate bias and the resulting transconductance reduction. For such a device measured DC data were available with slow-speed sweep, so as to stress the effect of device heating in reducing the device saturation current. The boundary conditions used for the thermal simulation are for a backside mounted structure; the thermal resistance of the bottom of the simulated region is taken as $\approx 18$ °C/W.

## Conclusions

A self-consistent thermal model and a closed-form thermal resistance model have been presented as complementary CAD tools for MESFET thermal performance evaluation and device optimization. The thermal resistance model allows complex, realistic backside-mounted multi-gate MESFET to be accurately simulated with negligible CPU times, while the self-consistent simulation of the VI curves demonstrates that, with proper boundary conditions, the two-dimensional physical model can correctly foresee the quantitative effects of device heating on the device behaviour.

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