POWER OPTIMISATION OF DISTRIBUTED AMPLIFIERS

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Abstract

A linear technique is described for the optimisation of output power and efficiency of travelling-wave amplifiers, together with guidelines for a practical computer-aided circuit design. The design procedure requires the determination of the optimum load impedances of the FET's, and the optimisation not only of the amplifier's gain and return loss, but also of the FET drains' loading.

Introduction

Distributed power amplifiers suffer from two main limitations [1] : first, large FET's have high input and output admittances, that reduce the cut-off frequencies of the two artificial transmission lines, and therefore the bandwidth; second, the "matching" of the amplifier, i.e. the synthesis of the artificial transmission lines, does not provide the optimum power loading of the drains of the FET's. The first constraint affects the total output power for a given bandwidth by limiting the total periphery, in a sort of a power-bandwidth limitation; the second one further degrades the performance of the amplifier by reducing the output power and efficiency of the single devices. It is this latter issue that is considered in this study.

The optimisation of the amplifier under large signal operations is clearly a non-linear design problem, still very burdensome for currently available workstations. An alternative approach is represented by the linear optimisation of the drain transmission line with the goal of optimally loading the FET's, i.e. of matching their large-signal output impedance as obtained for instance from a "load-pull" measurement. This can be accomplished by a careful design of the line itself and by some compromises on the optimisation goals. The increased output power and efficiency show that the basic limitation of improper loading has been removed.

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Circuit design

A standard three-stage 2 - 20 GHz travelling-wave amplifier has first been designed (fig.1). We obtained high return loss and flat gain, but the load impedances (fig.2) and load curves (fig.3, at 18 GHz) for the three FET's clearly demonstrate a mismatch: for comparison, the optimum power load with the -0.2 dB curves in the range 2 - 20 GHz is shown in fig.4. A re-optimisation of the circuit with the additional goal of matching the drains' loading has shown a tendency toward the introduction of unrealisable components (fig.5). In particular, the negative capacitance on the drain line acts as broadband match for the output capacitance of the FET's, and the negative inductances help the line to provide the same load to the other drains while still acting as transmission line.

The circuit cannot obviously be realised as described. We first note, however, that a star of three inductors (one of which negative) can be put in the form of coupled inductances, and find a physical implementation as coupled lines (fig.6). This type of cell has already be introduced as "constant R" element in the gate line of a small-signal travelling-wave amplifier, with the aim of widening the band [2]. In our case however, this component is used to allow the different FET's along the drain line to have approximately the same (optimum) loading.

Secondly, we substitute a practical component for the negative capacitor in the first cell. This problem is also found in the design of a single-ended wideband amplifier, where the required negative load susceptance is approximated with a passive matching network. In our case we prefer to let the first FET to be slightly mismatched, and to use its output conductance to make the impedance of the first cell, FET included, very close to the optimum load with negative capacitance. This "partially active" load is then transferred by the line to the other FET's, that appear to be well matched (fig.7). An undesired consequence of this procedure is a bandwidth reduction to approximately two octaves, nonetheless sufficient for many wideband applications. The schematic of the complete amplifier is shown in fig.8.

Results and Conclusions

Fig. 9a and 9b show respectively the small-signal and power performances of the two amplifiers. The simulation has been performed with LIBRA [3], for both linear and nonlinear operations. The FET is a Harris HMF0310, a 125 mW, 300-micron gate device, for which the non-linear proprietary EESOF model has been used in the simulation; its optimum load impedances have been computed from the same model.

The linear gain of the power-optimised amplifier is still reasonably good; the large-signal performance on the other hand shows a 1.5 dB output power increase at 2 dB gain compression in the band 5 - 20 GHz. Power added efficiency increases from 11% to 18%. The output power level is approximately 25.3 dBm, or 340 mW, when the single device has a maximum output power of 21 dBm, or 125 mW, with an efficiency of 23 %.

The results clearly indicate that the main cause for inefficient power amplification has been removed. The described linear design procedure improves the drain matching while preserving the travelling-wave characteristics of the distributed amplifier; results published in a paper based on similar considerations [4] confirm that this approach is effective for practical circuit design.

Bibliography

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[2] E.M.Chase, W.Kennan: "A power distributed amplifier using constant-R networks", 1986 IEEE MTT-S Symp. Dig., pp.811-815

[3] LIBRA User's Manual, EESOF Inc., Westlake village, CA

[4] J.B.Cole, A.Platzker: "Design technique for high power, high efficiency, broadband distributed amplifiers", 1989 IEEE MTT-S Symp. Dig., pp.941-944

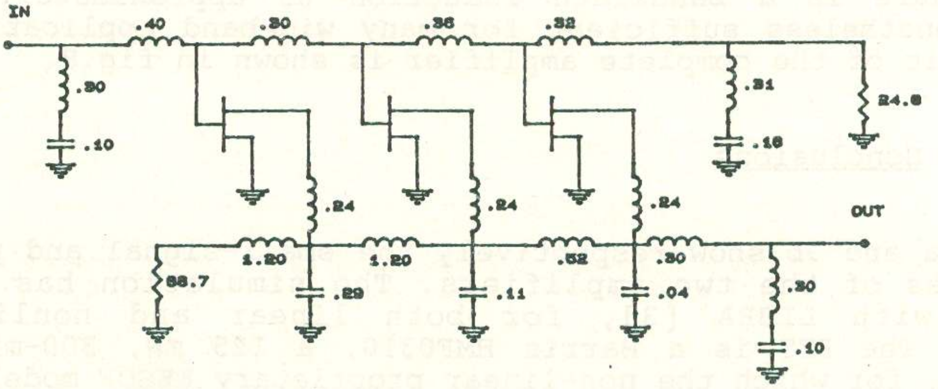


Fig.1 - A standard 2-20 GHz travelling-wave amplifier

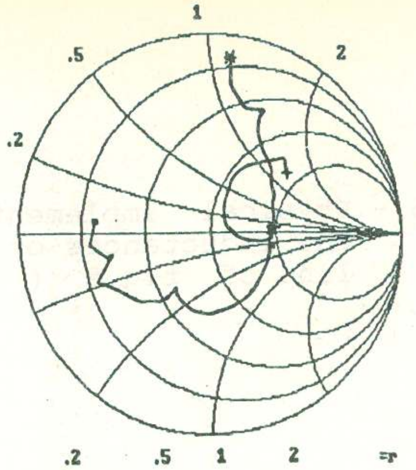


Fig.2 - Load impedances of the three FET's of fig.1, 2-20 GHz

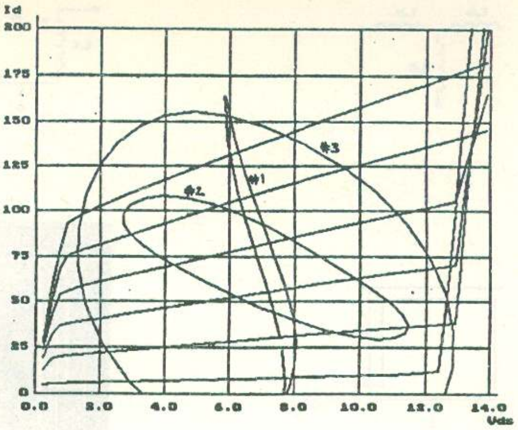


Fig.3 - Load curves of the three FET's of fig.1 at 18 GHz

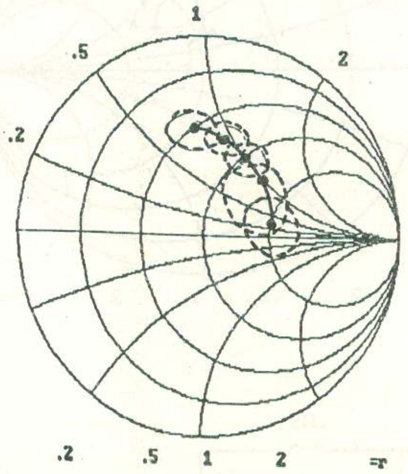


Fig.4 - Optimum load impedance of the FET for maximum output power, 2-20 GHz Also shown the -0.2 dB curves

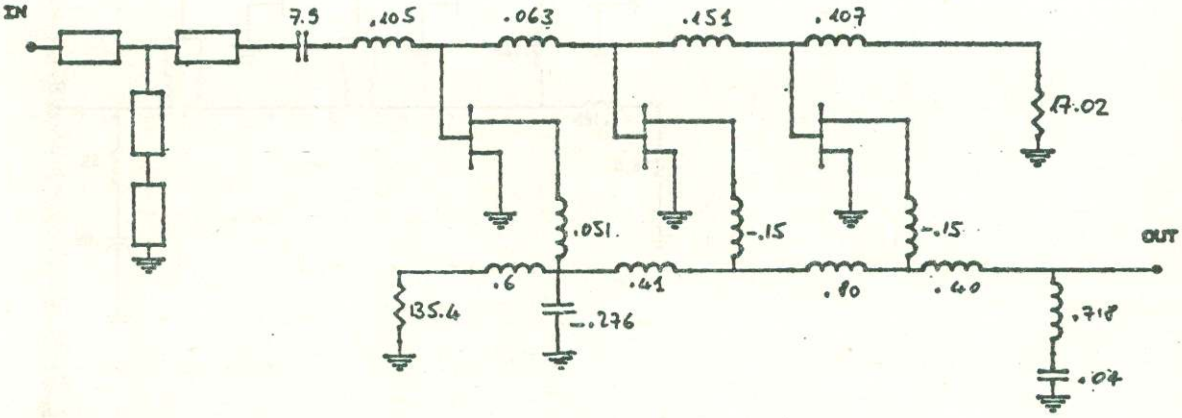


Fig.5 - A preliminary version of the optimised amplifier

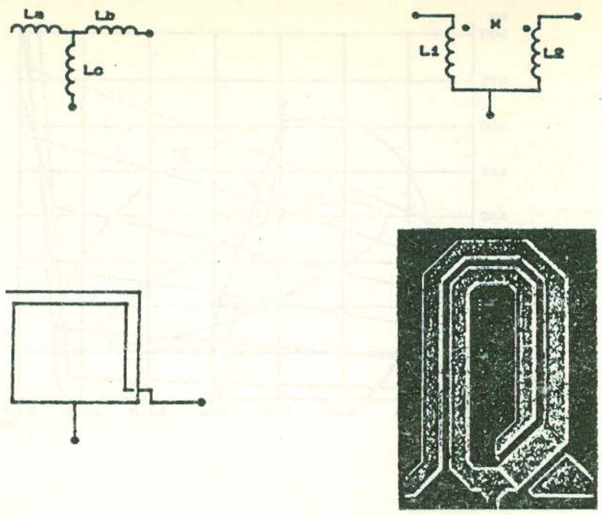
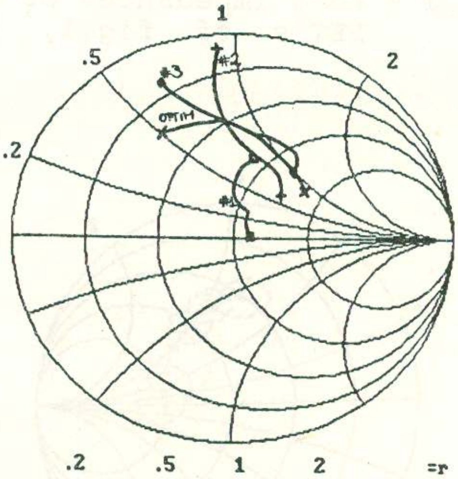


Fig.6 - Physical implementation of the inductances on the drain line of fig.5 (from [4])



ig.7 - Load impedances of the three FET's of fig.8, 5-20 GHz

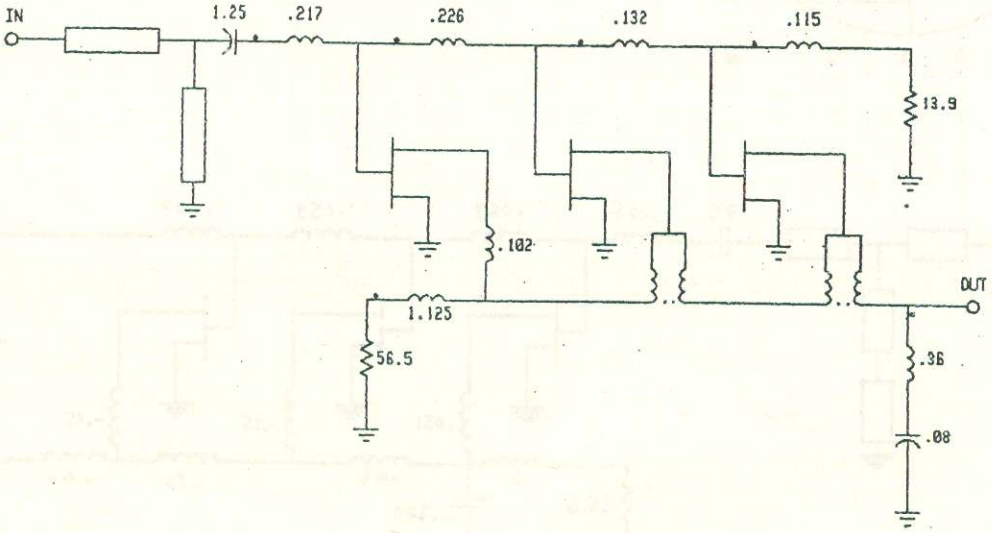


Fig.8 - The final version of the optimised amplifier

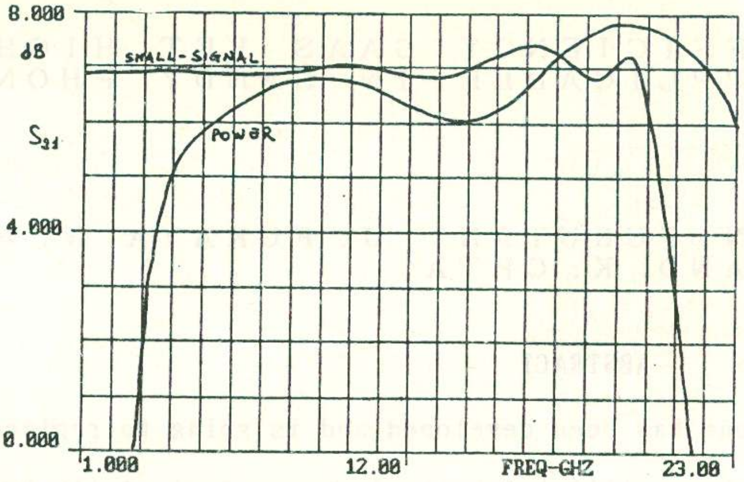


Fig.9a - Gain of the standard (SMALL-SIGNAL) and optimised (POWER) travelling-wave amplifiers

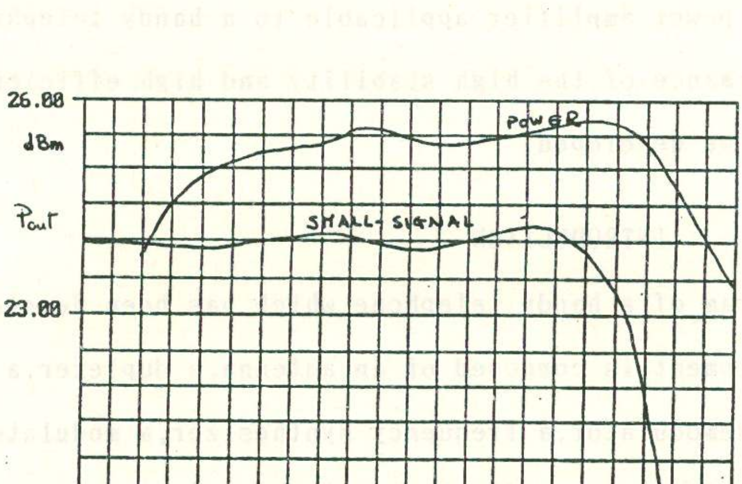


Fig.9b - Output power of the standard (SMALL-SIGNAL) and optimised (POWER) travelling-wave amplifiers