

RF-ON-WAFER TESTABLE COMPLETE MMIC DOWNCONVERTERS

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ABSTRACT

This paper describes the development of a family of RF-On-Wafer (RFOW) testable monolithic GaAs low noise downconverters (LNC's) for direct broadcast by satellite (DBS) use. The paper concentrates on the lower European band of RF frequency range 10.95 - 11.7 GHz, with 0.95 - 1.7 GHz IF. A relatively large and narrow-band prototype LNC was originally designed and tested. This was then developed into a full lower-band, more user-friendly design with less than 4mm^2 GaAs chip area. Conversion gains of 30dB and noise figures below 7dB have been achieved.

Keywords:- Low noise downconverter, DBS, MMIC, RF-On-Wafer

INTRODUCTION

The general schematic diagram of a DBS first stage, low noise block downconverter (LNB) is illustrated in Fig.1. The general LNB specification is a conversion gain of 55dB and a noise figure of less than 1.3dB (Ref.1). A complete MMIC solution is not yet viable because of the need for a sub-1dB noise figure HEMT at the front end. The phase noise considerations of the local oscillator (LO) also necessitates off-chip dielectric resonator (DR) stabilisation. The simplest part-MMIC solution is illustrated in Fig.2. Two discrete HEMTs are used to reduce the noise figure specification of the MMIC LNC to 7dB, with approximately 30dB of associated gain. The LO becomes an on-chip negative resistance circuit (NRC) which is coupled to an external DR puck via a 50Ω microstrip line. The MMIC circuit described in this paper is unique in that RFOW test pads are included on all 3 ports. This allows RFOW testing of the LNC by injection of an external LO signal into the NRC port. This concept is illustrated in Fig.3. RFOW testing of the LNC is highly desirable from a cost point-of-view because it allows pre-selection of RF-good devices before costly operations such as dicing, sorting, package assembly and bonding are performed.

DESIGN METHODS

A prototype LNC was designed using the GEC-Marconi in-house standard foundry process. The circuit was purposely narrow-band, used separate control lines for each constituent, and occupied some 7.5mm^2 GaAs area. A second design utilised various high packing density techniques to reduce chip area. These included $4\mu\text{m}$ tracks and spirals, stacked spirals with $6\mu\text{m}$ tracks, $2\mu\text{m}$ polyimide vias, NiCr resistors and close packing of components. The device supply lines were connected to one positive and one negative supply rail. Through GaAs vias were used to eliminate the need for multiple bond wires on the final diced chips. These also allowed RFOW test compatibility. Final chip area was 3.6mm^2 .

The LNA within the downconverter consisted of a 2-stage single-ended design with 12dB gain and a NF of approximately 4.5dB. A 3-stage design was also produced to increase the gain to 15dB, but more importantly to improve gain flatness. The LNA was modelled using LINMIC+ software from Jansen Microwave, which is a layout orientated simulator. This ensured that the actual physical layout of the critical RF path was exactly as simulated.

The mixer utilised a dual-gate FET as the non-linear element. The advantages of a dual-gate FET over other mixer elements are conversion gain, with isolation between the LO port (gate 2) and the RF input (gate 1). The

mixer was designed to provide a conversion gain of some 2dB. The RF and LO matches were designed to short-circuit the IF frequencies whilst the IF match was designed to short-circuit the RF/LO frequencies. The design schematic is illustrated in Fig.4. When integrating the sub-components into the LNC's, the inter-stage match between the LNA and mixer RF input was optimised to yield adequate Image frequency rejection.

The IFA was again a single-ended 2-stage design. Lossy matching was used to ensure an acceptable match over the required 0.95 - 1.7 GHz IF bandwidth. Stacked spirals were used to minimise the size of the large chokes required at these low frequencies. The gain specification of the IFA was 20dB minimum.

The on-chip NRC utilised a common-source MESFET with capacitive series feedback as the negative resistance generating element. A single wideband NRC circuit was designed to allow use with many LO fixed frequencies. The oscillator was matched to oscillate directly into the mixer LO port without any buffer amplification. The LO circuit was produced by coupling the on-chip NRC to a mechanically tunable DR puck. Coupling was via an Alumina-based 50 Ω microstripline as illustrated in Fig.5. The 50 Ω line was terminated in a 50 Ω resistor to eliminate spurious oscillation modes (Ref.2).

RESULTS

The prototype LNC was initially designed for 1.1 - 1.3 GHz narrow-band IF. The LO was designed to work with various DR pucks from 10GHz to 11.5GHz, allowing potential RF usage in the band 11.1-12.8 GHz. The circuit was first tested RFOW using an injected signal of 10GHz. The circuits were then diced and the chips incorporated into a jig with an alumina substrate. The previous tests were then repeated using the same injected LO. Finally, the injected LO was replaced by a 10 GHz mechanically tuned DR arrangement. Fig.6 illustrates the correlation between all three measurements, and verifies the RFOW compatibility of the design. Fig.7 shows similar LNC performance using DR pucks of 10.8 and 11.475 GHz respectively.

The miniature LNC was designed for Astra satellite TV receiver usage. (RF 10.95 - 11.7 GHz, LO 10 GHz, IF 0.95 - 1.7 GHz). So far the circuits have been measured RFOW only. Fig.8 illustrates a typical result. NF measurements above 1.5 GHz have not yet been attempted. The circuits are currently being diced for jig/DR measurements.

CONCLUSIONS

A prototype narrow-band LNC designed using a standard foundry process has been successfully measured. Gains of 30dB and noise figures below 7dB were obtained. A wider-band miniature design utilising high packing density techniques has also been fabricated. Preliminary RFOW results show great promise. Both circuits have demonstrated the feasibility of pre-dicing RFOW testing by injection of an external LO signal into the on-chip NRC port. Work is ongoing to produce circuits for all Ku-band DBS frequency bands, and to further reduce the chip size for lower-cost manufacture in high volumes.

ACKNOWLEDGEMENTS

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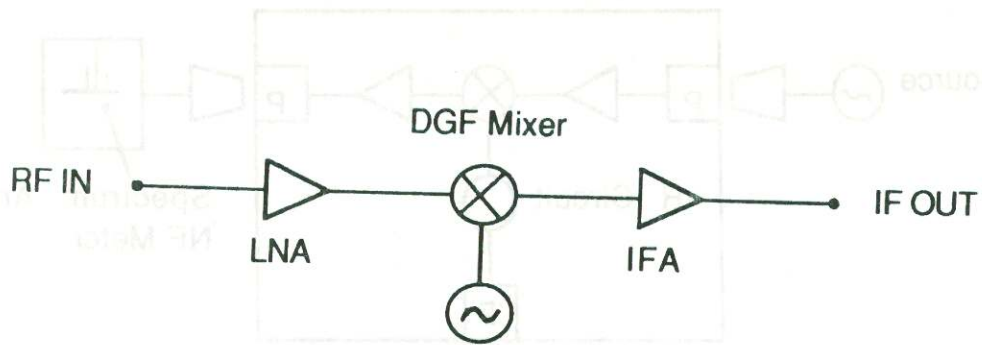


Fig. 1. General DBS LNB Schematic

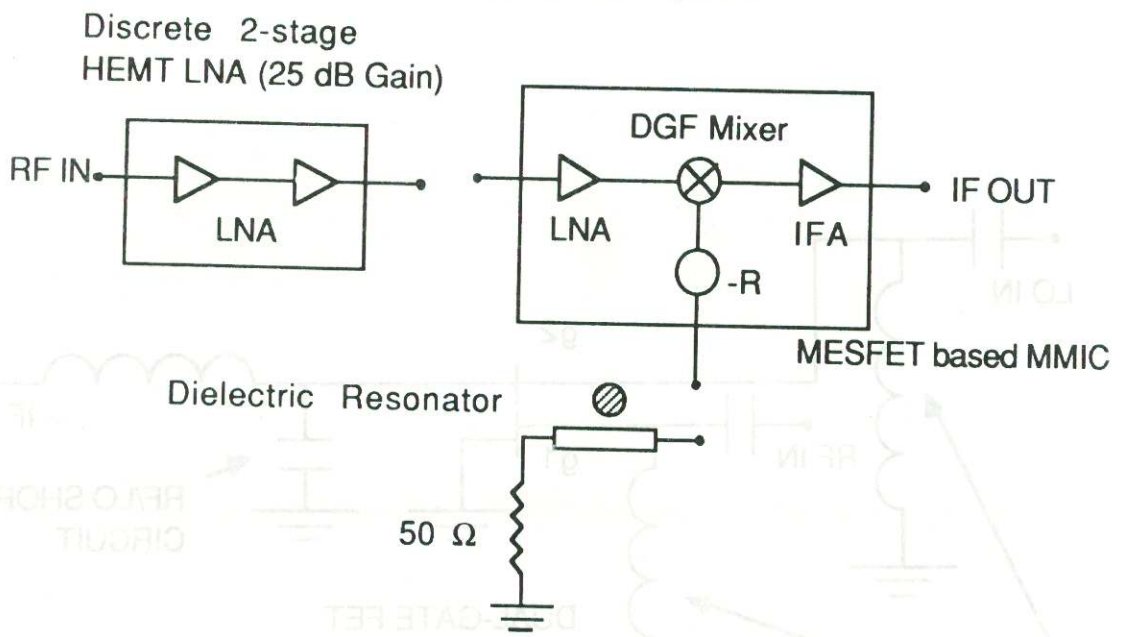


Fig. 2. Part-MMIC DBS LNB Configuration

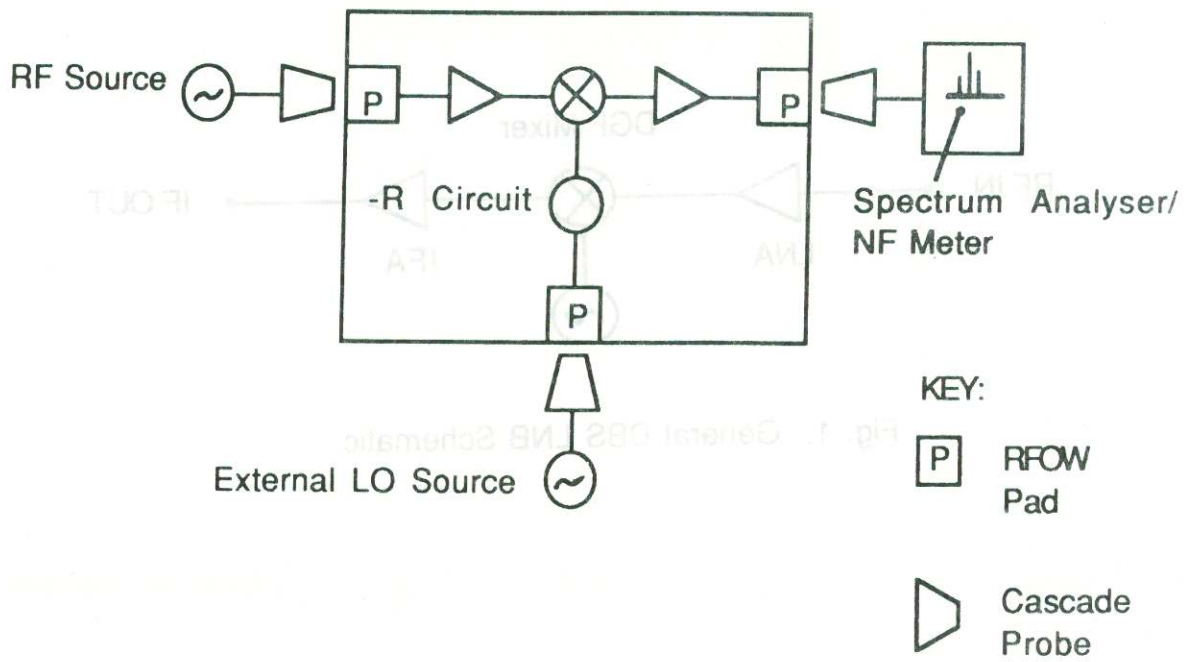


Fig.3. RFOW Testability of MMIC Downconverter chip utilising external LO

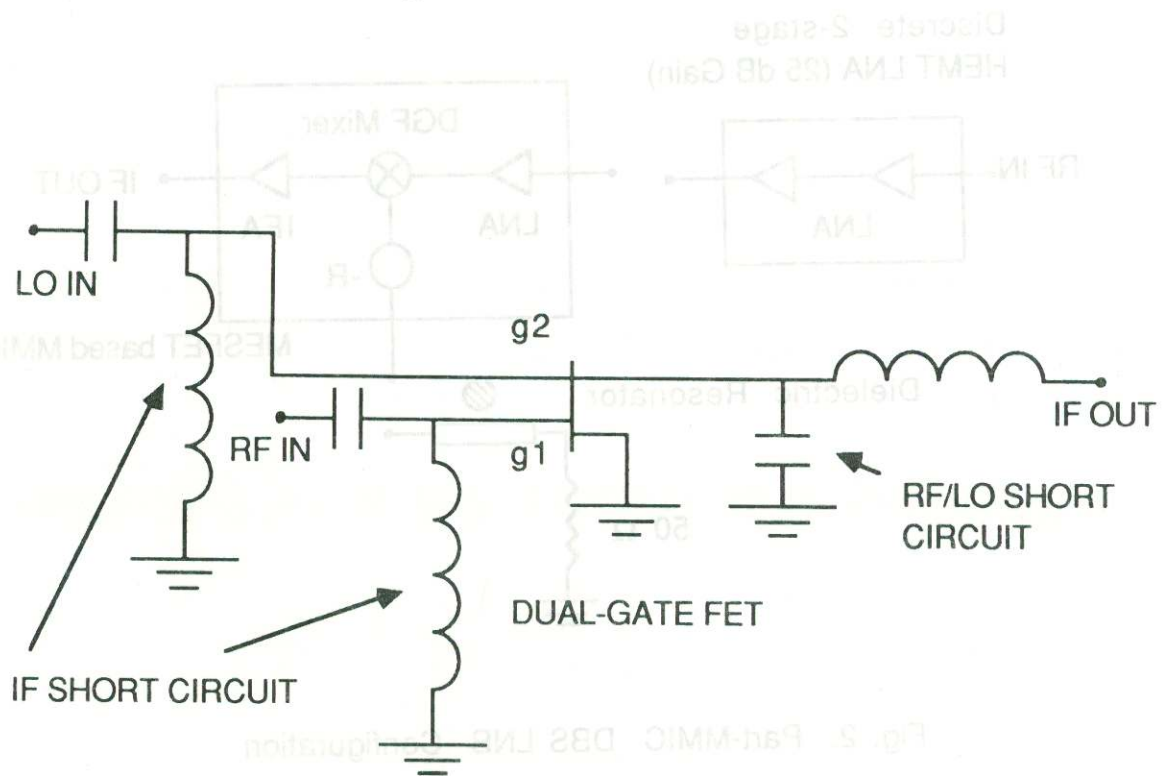


Fig. 4. Dual-gate FET mixer, as used in MMIC LNC

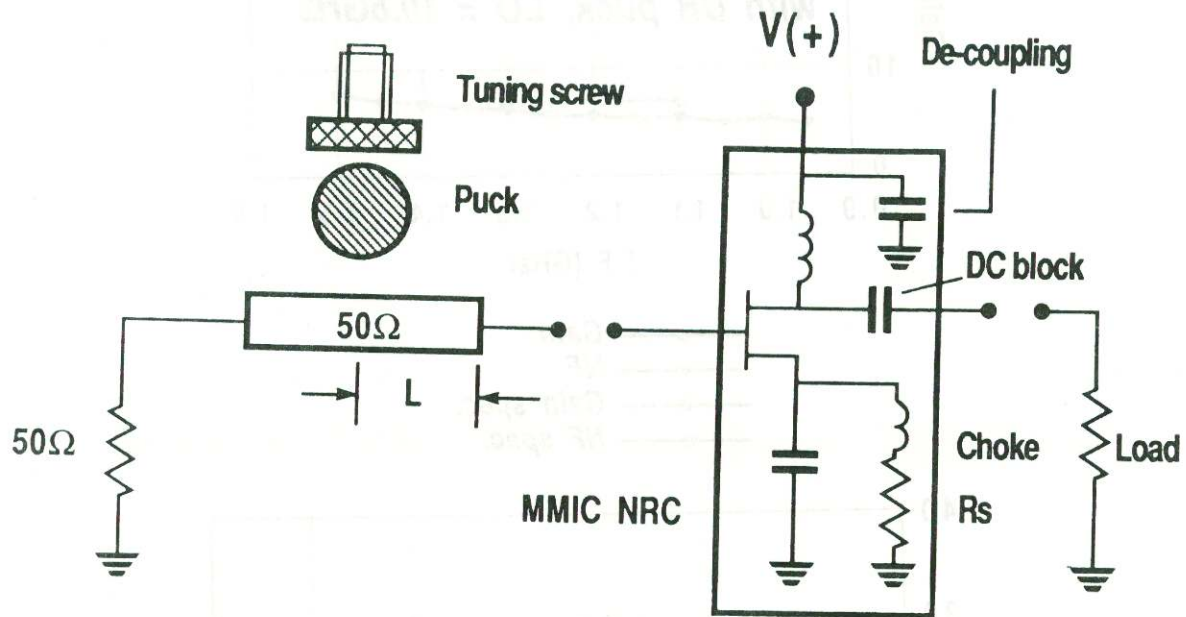


Fig. 5. MMIC-based DRO schematic

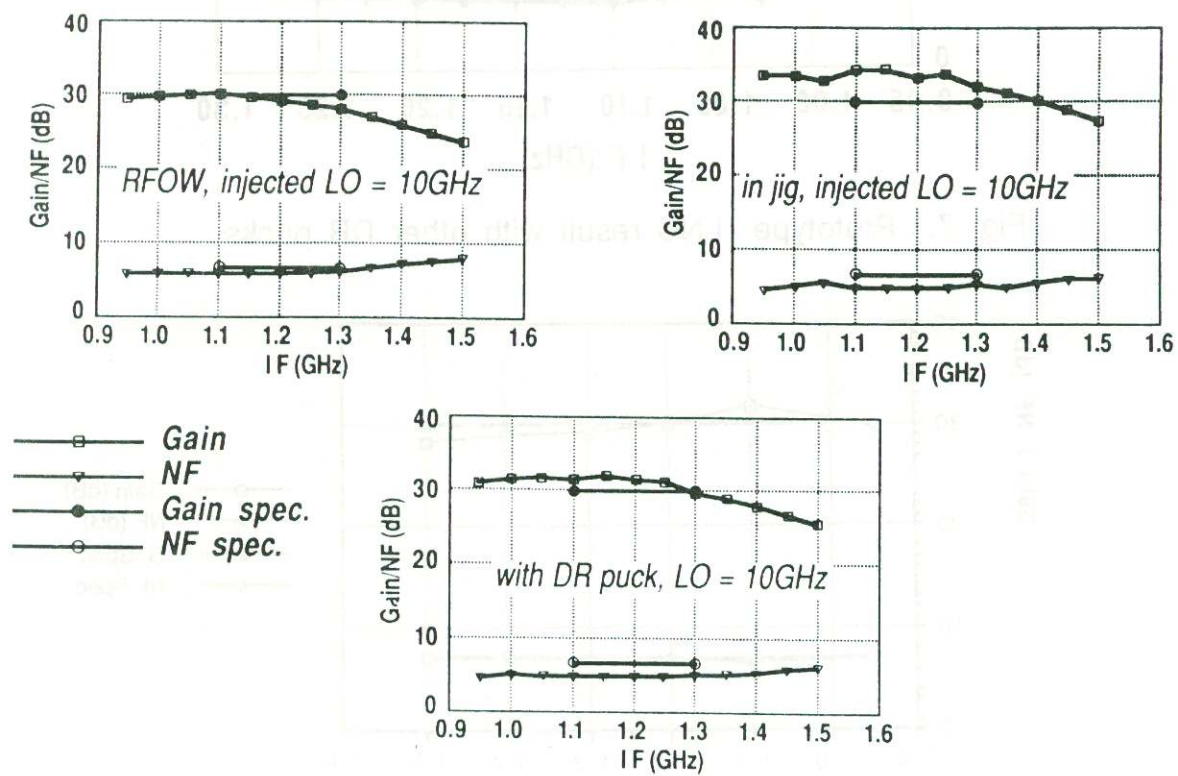
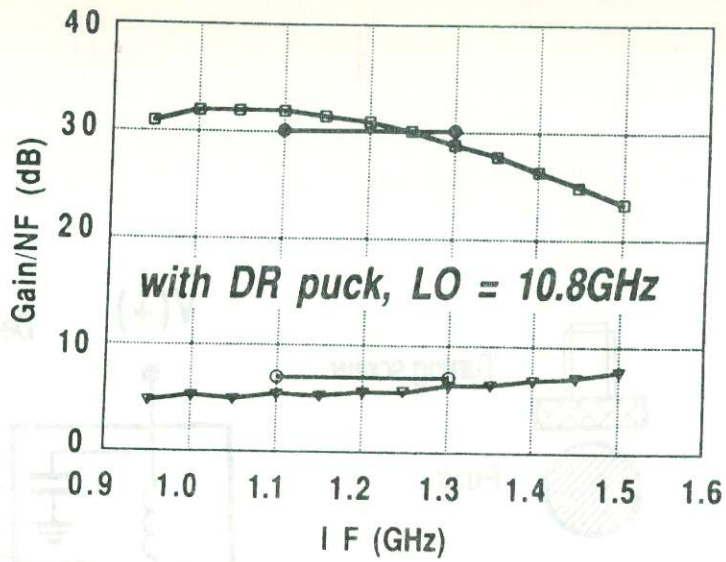


Fig. 6. Prototype LNC result



- Gain
- ▽— NF
- Gain spec.
- ◇— NF spec.

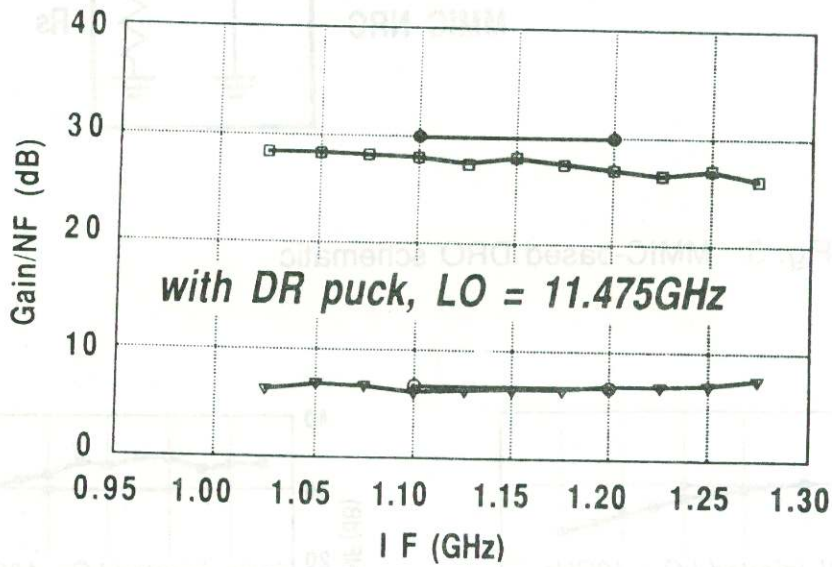


Fig. 7. Prototype LNC result with other DR pucks

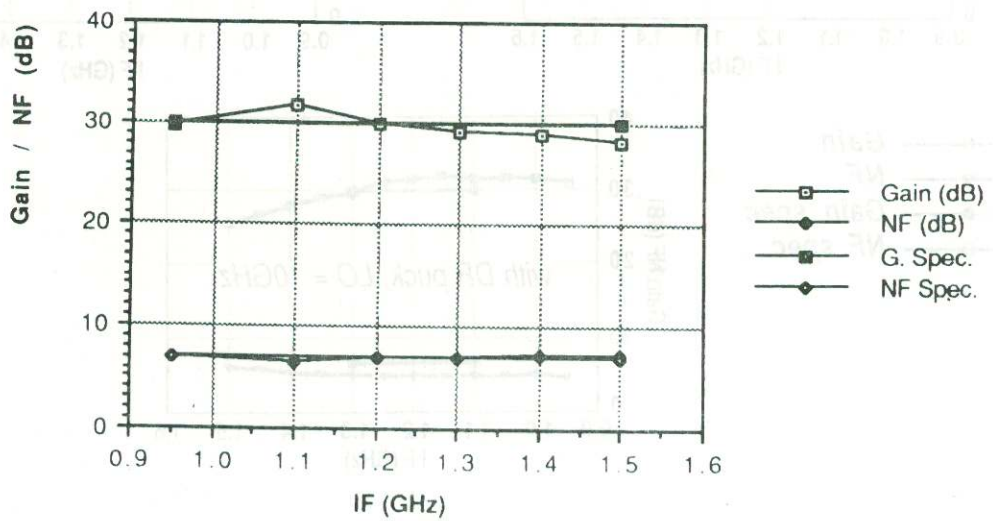


Fig. 8. Mini Astra-band LNC result, RFOW, LO=10 GHz