DEVELOPMENT OF GAIN/PHASE CONTROL BLOCKS FOR SPACE APPLICATIONS

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ABSTRACT

Phase and gain control components are key items for phased array type applications. This paper describes the results on such digitally controlled components up to X-band frequencies.

Keywords: Gallium Arsenide, MMIC, Beam Forming, Phase Shifter, Attenuator.

1. INTRODUCTION

Digitally controlled phase and amplitude elements in GaAs MMIC form are finding an increasing number of applications. System requirements dictate that phase shifter circuits be "amplitude free" and amplitude control circuits be "phase free". Usually multi-bit elements are required for these applications and the requirement for minimal associated parameter variation puts a severe constraint on the design of these components. For example, any mismatch interaction between individual bits in different states can give rise to additional amplitude and phase variations for the overall circuit. For the phase shifter, emphasis has therefore been placed on minimising the differential insertion loss between phase states and the absolute phase shift performance. Similarly for the attenuator.

These circuits were designed using depletion mode MESFETs and their limitation as switching elements was taken into account in the design. Two chips were designed and fabricated to meet the requirements of the X-band digitally controlled phase shifter (frequency range 7.8 - 8.5GHz).

2. PHASE SHIFTER

This X-band digitally controlled phase shifter is based upon two chips. One chip can be used in a coarse resolution system or the two chips can be used together to produce a fine resolution system over an 8.5% bandwidth at X-band frequencies. The first chip contains a 180° and a 90° bit. The second chip contains circuits for the 45° and 22.5° bits and the 11.25° bit.

The 180° degree bit is based on two band-pass circuits with an inherent differential insertion phase of 180°. A simple SPDT switch network is connected at each end and the shift in phase is achieved by toggling between each band-pass network. This technique gives a bandwidth of around 50% for this bit and less than 0.1 dB differential insertion loss over the band of interest. (See Figure 1).

The 90° phase shifter is an embedded fifth order high-pass low-pass filter. The parasitic components of the switch FETs are absorbed by the filter elements. The differential phase shift is obtained as the circuit is switched from a high- pass to a low-pass filter; enacted by changing the path of the RF and by-passing some elements. (Ref:1)

Care has to be taken when attempting to implement a high-pass filter using MMIC technology as the parasitic shunt capacitances give a band- pass characteristic to the insertion loss. Optimisation of the circuit is required to achieve the minimum differential insertion loss between states. (See Figure 2).

The three bit Phase Shifter uses a bridged-T technique for the 45° and 22.5° bits and a simple two element circuit for the 11.25° Phase Shifter. (Ref:2). For the bridged-T technique the series inductances are derived from distributed, high impedance transmission lines. Shunt capacitance is directly derived from pinched-off FET's. (See Figure 3).

For the 11.25° Phase Shifter a transmission line inductance and lumped capacitance are connected in series. Either the capacitor or the inductor is then by-passed by a GaAs MMIC MESFET switch. (See Figure 4).

Measured test results over the 7.8 to 8.5GHz band of interest show, for the most significant bit, a phase accuracy of ±2.9° and a chip to chip phase variation of 1.1°. For the least significant bit, phase accuracy is ±3° whilst chip to chip variation is 2°. Differential insertion loss is ±2dB and ±1.8dB for the most significant and least significant bit respectively.

The phase shift performance for the Most Significant Bit can be seen in Figure 9. All of the phase states for the Least Significant Bit can be seen in Figure 10.

The fabrication technology uses a wafer thickness of 200µm which increases the dimensional width of the transmission lines. Through chip vias are available and are used whenever grounding is required. The 180° bit uses a Lange coupler as a coupled line element which is 2460µm in length. The chip size of the Most Significant Bit is 4.3 x 2.7mm whilst the Least Significant Bit is 1.65 x 2.7mm. The "Y" dimension has been unified to allow the two chips to be directly bonded together if required. Photographs of the two chips can be seen in Figures 6 & 7.

3. GAIN CONTROL CIRCUIT

A control range of 31dB gain variation with a step size of 1dB was required from a single, digitally controlled, chip. To fulfil this, a review of the many techniques proposed in available literature as well as several novel solutions was conducted. For evaluation purposes, precedence was given to parameters in the following order :

Gain accuracy, phase tracking between states, input and output port matches and lastly, insertion loss. Many designs were rejected on the grounds of extreme yield sensitivity to key components.

The technique of steering the signal through either a low loss or attenuative path with SPDT switches, was adapted from previous BAe activities. Active area resistors are difficult to implement in small values (<20Ω) and so "Pi" networks were used for the attenuators. The 4, 8 and 16 dB bits are implementable in this fashion (Figure 7). Gupta et al (Ref:3) proposed combining the switches and attenuators in one structure by replacing the series resistors in a T-attenuator with scaled FETs. This technique can be reduced still further by removing the shunt FET's. In fact, for small bits scaling the FETs is not strictly necessary since the attenuation is dominated by the shunt resistor to ground. But by changing the size of the series FETs the port matches are improved. The 1 and 2dB bits are implemented in this manner and are shown in Figure 8.

One of the main reasons for selecting these two techniques was that the symmetry between the possible RF paths greatly reduced the sensitivity to modelling errors as well as processing and environmental variations. The sensitivity was also reduced by defining resistors in the same bit with a common crystalographic orientation and keeping them as close together as possible. The circuit size is 12 mm^2 with driver circuitry mounted externally.

Predicted results for the gain control circuit are shown in Figures 11 and 12 showing the gain and phase accuracy respectively. Gain setting accuracy is 0.2dB, phase tracking is ±1.2° with port matches better than 18dB and an insertion loss of 10dB.

4. CONCLUSIONS

A 5-bit X-band phase shifter was developed utilising four different techniques on two chips. Measured and predicted results compare well, phase accuracy is better than 4° with good tracking of differential insertion loss.

A 5-bit 1 - 6.5GHz attenuator design has been presented using two process and environment tolerant techniques on a fully integrated chip. 31dB of gain control range is achievable with an accuracy of 0.2dB and excellent phase tracking.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

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2. Christopher Moye, Glenn Sakamoto, Michael Brand, "*A Compact Broadband, Six-Bit MMIC Phaser with Integrated Digital Drivers*," IEEE MTT-S Digest, pp 457-460, 1990.

3. Gupta R. V. et al, "*Modelling And CAD Of An Ultra-Broadband Monolithic 5-Bit Digital Attenuator*", Insistitute for Microelectronik, 1988.

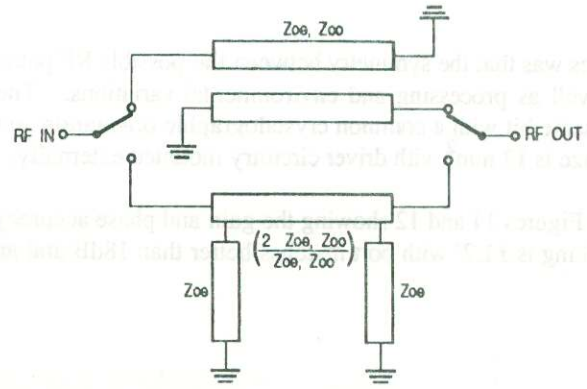

Figure 1: *180 °Bit*

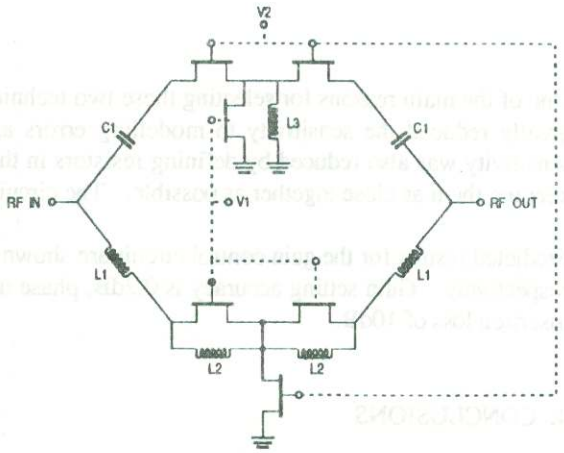

Figure 2: *90 °Bit*

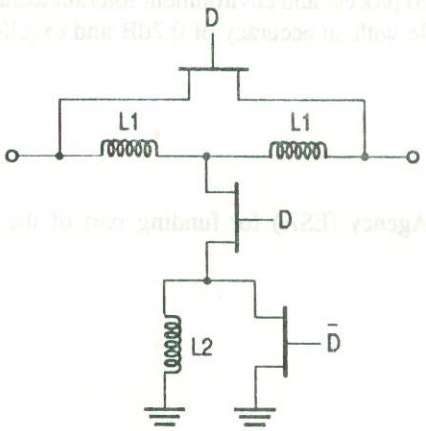

Figure 3: *45 °& 22.5 °Bit*

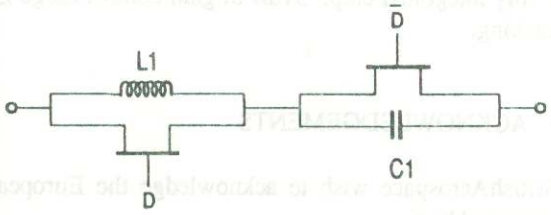

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Figure 4: *11.25 °Bit*

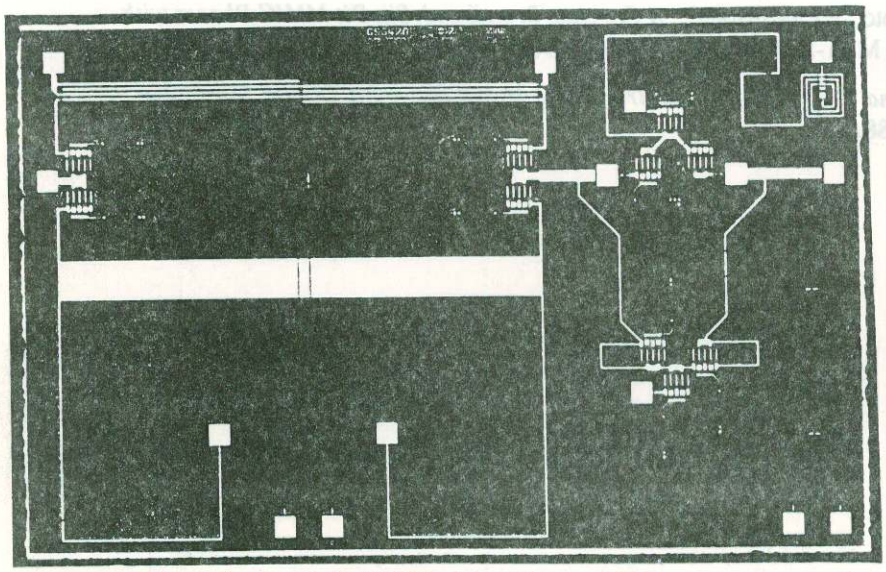

Figure 5: *GaAs MMIC Phase Shifter - MSB*

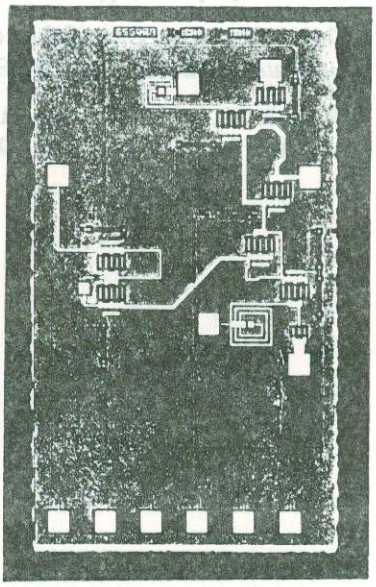

Figure 6: *GaAs MMIC Phase Shifter - LSB*

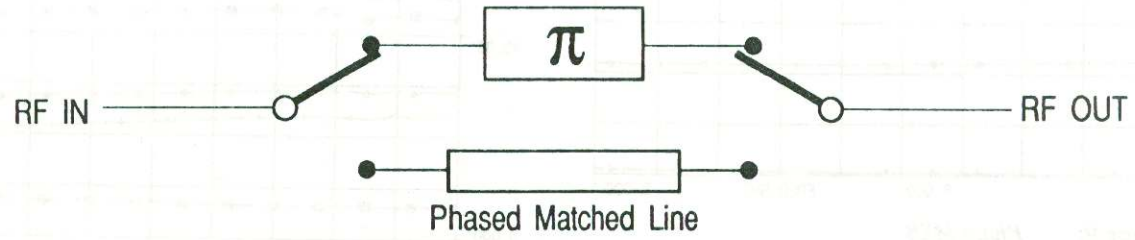

Figure 7: *4, 8 & 16dB Attenuators*

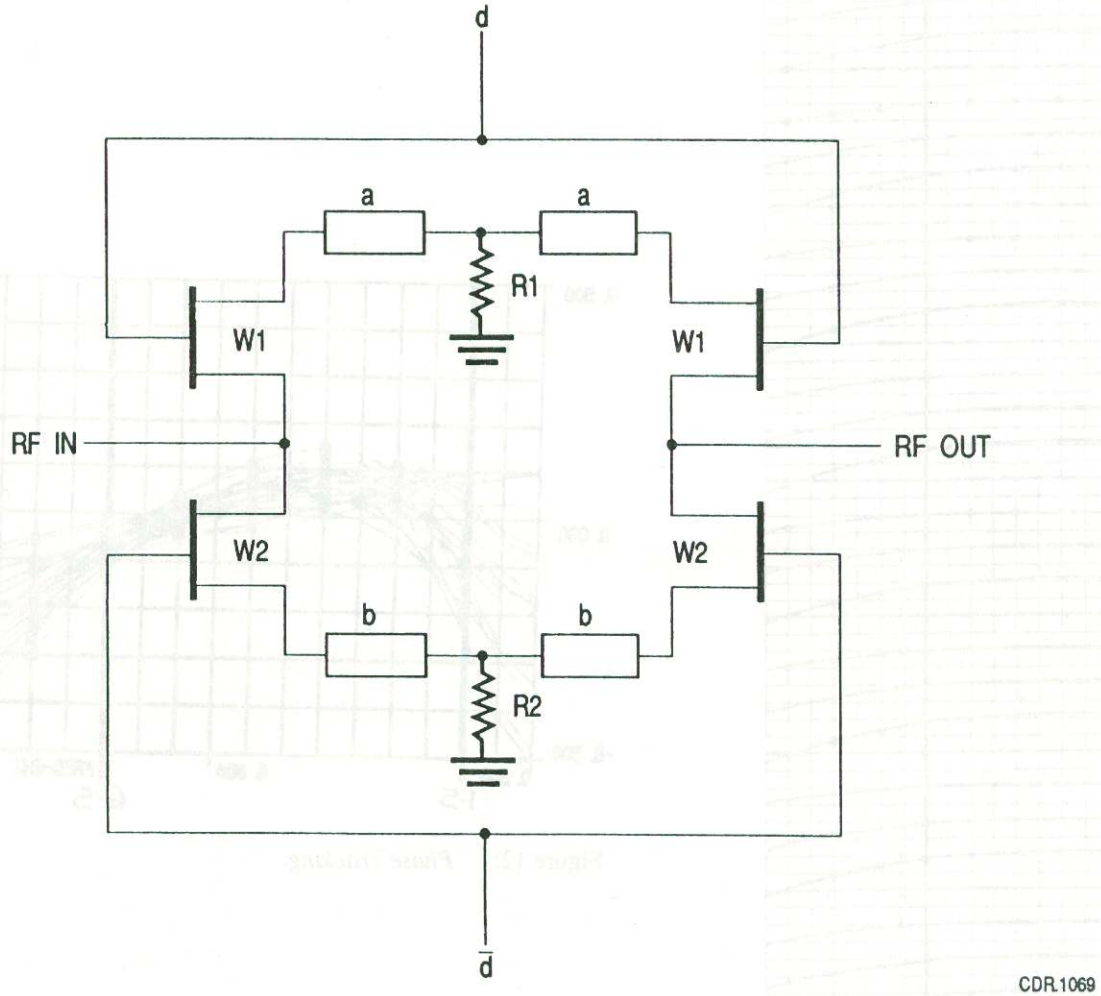

Figure 8: *1 & 2dB Attenuators*

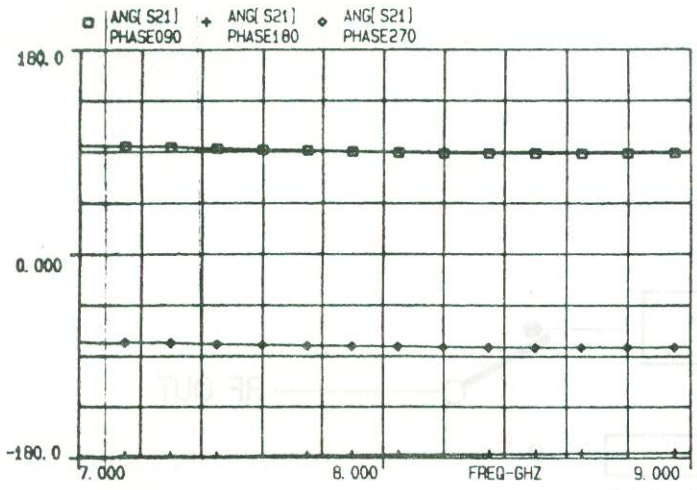

Figure 9: *Phase MSB*

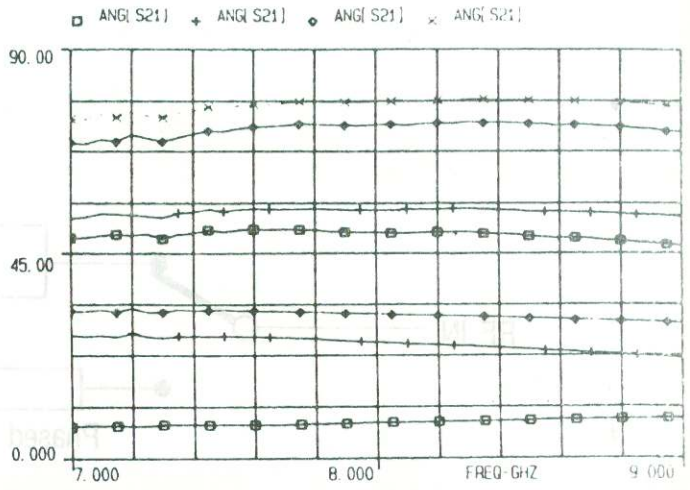

Figure 10: *Phase LSB*

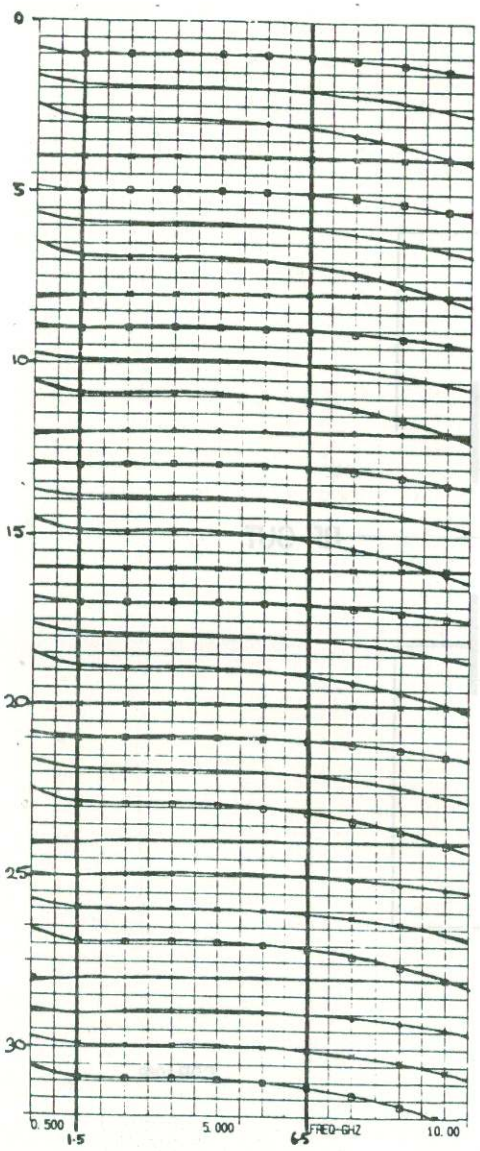

Figure 11: *Gain Set*

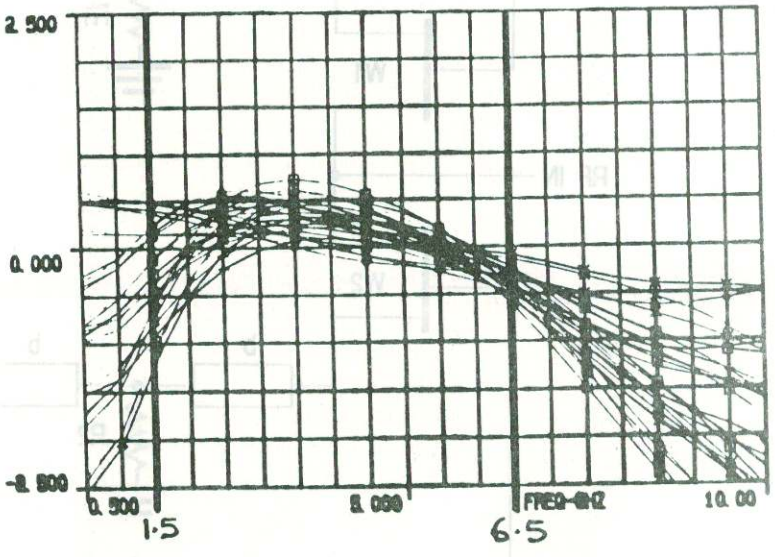

Figure 12: *Phase Tracking*