EEsof - PHILIPS SMART LIBRARY

Peter T. Parrish, Manivannan Peroomal, EEsof, Inc.
5601 Lindero Canyon Road, Westlake Village CA 91362
Ph: (818) 879-6200, Fax: (818) 879-6394

Remy LeBlanc, Philips Microwave Limeil
22 Avenue Descartes, BP15, 94453 Limeil-Brevannes Cedex
Ph: (33) (1) 45699610 ext 9310, Fax: (33) (1) 45694477

Giuliano Gatti, European Space Agency
European Space Technology and Research Center
NL-2200 AG Noordwijk, The Netherlands

Introduction

In this poster paper we present a new MMIC design library -- the EEsof-Philips SMART (Simulateable Microwave ARTwork) Library -- based on a novel design approach that incorporates a file-based parameter list. The SMART Library permits the capture of a MMIC schematic, and can simultaneously display the detailed physical layout and circuit simulation. The library elements consist of schematic symbols, parametrized layout macros and C-language simulation models. The library works in conjunction with EEsof's, ACADEMY^R design environment and Libra^R nonlinear harmonic balance simulator.

Current State of the Art

Until recently, MMIC designers were confined to a difficult and error prone iterative design methodology. This methodology consisted of electrical design using netlist capture and simulation. The resulting design was then translated into a physical layout typically employing a different toolset and computer host. Due to floorplanning constraints, mask-level design rules and limitations in the available cell library, the first layout iteration often failed to realize the original electrical design and a resimulation was required to check performance. Several iterative cycles were commonplace to converge on a design that met performance and layout specifications.

SMART Libraries Advance the State-of-the-Art

The SMART library approach eliminates the iterative design cycle by permitting simultaneous electrical and physical design. When placing a SMART Library element, a common set of user definable parameters is simultaneously passed to the schematic symbol, simulation model and layout cell. For example, a MESFET requires the user to define only the number of gate fingers and unit gate width; whereas a capacitor requires a capacitance, aspect ratio, and selection of top or bottom metal for each node. This parametric approach is quite flexible and insures synchronization of simulation and layout.

Validated Electrical Models and Layout

All simulation models are verified by foundry measurements and the layout automatically obeys all foundry design rules. If a parameter is changed in the design, the schematic symbol data list, circuit simulation and layout all change simultaneously. Simulation and layout can be checked incrementally as the design progresses. The final design can be translated into a GDSII file for shipment to the foundry.

Layout Considerations

A great deal of flexibility has been built into the layout macros, permitting the

designer to define node locations, entry and exit angles and mirroring. Highly compact designs can be realized by taking advantage of this flexibility.

The Technology File -- the Key to Technology Independent Design

The EEsof-Philips SMART Library will eventually support six Philips Microwave Limeil processes, shown in Figure 1. In order to support these multiple processes, we chose to develop ASCII files each of which would contain all the parameters for a single process needed for simulation and layout. Depending on the target process being designed to, a different "technology file" is read at ACADEMY boot time. In this way, the actual technology behind a specific design is transparent to the user.

The technology file approach also improves the maintainability of the SMART Library. Should a given foundry process change over time, the only change required to revise the SMART Library is the modification of the technology file. New processes can be included by creating new technolgy files.

Linear and Nonlinear Models

All models for FETs and diodes have been implemented in such a way that both linear and nonlinear simulation is supported, using the same analytic expressions. In this way, nonlinear simulation at low input power yields the same answers as linear, S-parameter analysis.

Design Example

A computer demonstration of the EEsof-Philips SMART Library will be available at the Poster Session. The demonstration example will highlight the following features: linear and nonlinear simulation, tuning and optimization, changing process technologies, and layout design rule compliance.

Conclusion

The SMART Library approach places all the tools necessary to capture, simulate and layout a MMIC design on the engineer's desk. All aspects of a design -- schematic, simulation and layout -- are created simultaneously. Verified electrical models and correct-by-construction parametrized layout macros eliminate costly and time-consuming design iterations and eliminate design rule violations. The SMART Library approach has improved ease of use, shortened design time and reduced the risk of errors associated with MMIC design.

Process	Vt	Lg	Mode	Comment
D07A	-3.0 V	0.7um	D	
D05AL	-1.4 V	0.5um	D	
ER07AD	+0.175/-2.0 V	0.7um	E/D	
D07M	-3.0 V	0.7um	D	100 um, vias
D05ML	-1.4 V	0.5um	D	100 um, vias
D05AH	-	0.5um	-	PHEMT, 100 um, vias

Fig. 1 Philips Microwave Limeil Proceses to be supported by EEsof-Philips SMART Library