NONLINEAR OPTIMIZATION TECHNIQUES FOR STRONG NONLINEAR MMIC FUNCTIONS

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ABSTRACT

A mathematical optimization approach , including scaling properties of FET devices, has been used in order to control strong nonlinear non autonomous MMIC functions. In particular broadband distributed power amplification and balanced multiplication has been studied. Optimum choice of gate length and embedding impedances permits us to obtain the best compromise between the main performance parameters such as broadband gain, return loss etc, and the power behaviour. Good agreement between theoretical and experimental results has been obtained in order to validate the mathematical approach.

Keywords: Nonlinear CAD, MMIC circuits

1. INTRODUCTION

The general problem in dealing with strong nonlinear MMIC functions such as multipliers, oscillators, mixers, power amplifiers, etc, is to find accurate mathematical procedures to derive optimum operating conditions, that is, optimum bias point, power efficiency, stability conditions, embedding impedances, etc. On the other hand, MMIC technology currently uses the geometrical scaling properties of electron devices in order to provide a maximum degree of flexibility for the designer.

Several authors have proposed nonlinear optimization methods, mainly working in the frequency domain, starting from a previously defined linear embedding, while others use the port voltage and current concept and then the embedding circuit is synthesized [1,2].

The work proposed here joins the mathematical methods for nonlinear optimization and the nonlinear scalable MESFET or HEMT models available from a foundry in a unique algorithm.

Following this mathematical formulation, we have tried the design of a 0.7μ gate width 2 to 18 Ghz five sections distributed power amplifier, and a 4 to 9 GHz input frequency multiplier in balanced configuration. The results obtained agree very well with the theoretical predictions, thus confirming the validity of this approach.

2.- DISTRIBUTED POWER AMPLIFIER

In the case of the distributed power amplifier, traditional techniques [3] fail in output power performance because the design is mainly oriented to the broadband gain characteristics. Thus some of the transistors may not contribute to the output power (dissipating transistors) because the maximum power capabilities of each transistor is not

accurately controlled.

Graphical optimization of load cycles [4] is a good starting point for the design of such amplifiers. Optimum load contours can be obtained at different bias point and frequency. Fig-1 and Fig-2 show these optimum contours for a 0.7μ experimental power technology from THOMSON-DAG. The nonlinear model for this device was derived using Tajima's empirical model.

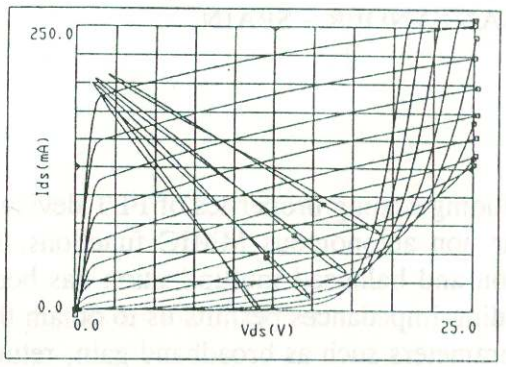

Fig.1 Load Cycles at F=2.0 GHz

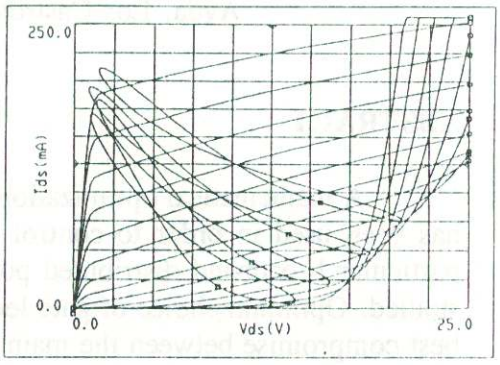

Fig.2 Load Cycles at F=18.0 GHz

As we can observe, the optimum load for maximum added power can be associated with a simple parallel RC network valid from 2 to 18 GHz. This result will greatly simplify any further nonlinear optimization process because the starting point is a very simple one.

The final goal for the five-section distributed amplifier was a 5 dB gain 2-18GHz band with a maximum of added power. The chosen configuration was a classical one with gate coupling capacitors and drain optimizable lines in order to balance the voltage at the gate and drain lines.

Starting from the quasi-optimum load cycle contours, a multiharmonic algorithm [1] of optimization was applied to each transistor in order to reoptimize the maximum added power for each transistor, while maintaining a low content for the superior harmonics:

$$\mathbf{Padd}(\omega) = \mathbf{Pout}(\omega) - \mathbf{Pdiss}(\omega) \qquad (1)$$

where the multiharmonic Jacobian versus the internal control variables of the nonlinear model is obtained in an analytical form.

$$\begin{matrix} \dfrac{\delta \mathbf{Padd}(\omega)}{\delta \mathbf{Vgc}} & \dfrac{\delta \mathbf{Padd}(\omega)}{\delta \mathbf{Vdc}} \end{matrix} \qquad (2)$$

Vgc and **Vdc** represent the multiharmonic vectors corresponding to the internal gate and drain control voltages, and (ω) the frequency vector. It is assumed that mathematical conditions for a minimum power content at higher frequencies were used.

Starting from these results, a new error function has been created in order to equalize the voltage swing and phase delay at each stage of the distributed configuration:

$$Err = Fg[\omega, Cgk, Zgk, Zdk] + Fd[\omega, Cgk, Zgk, Zdk] = MINIMUM \qquad (3)$$

where **Cgk** is the vector corresponding to the Gate Coupling Capacitors.
Zgk is the vector corresponding to the Impedance and Length for the Gate lines.
Zdk is the vector corresponding to the Impedance and Length for the Drain lines.

Tacking into account this error function, we can chose equalization of added power and voltages at the gate and drain lines, thus obtaining broadband gain while maintaining an acceptable power contribution for each transistor. Fig-3 and Fig-4 show the output power of the five stage amplifier for small signal and large signal operation. Fig-5 shows the optimized load contours for each transistor. We can observe that the main problem of existiance of power consuming transistors is overcome. Fig-5 shows the final aspect of the power amplifier using the 0.7μ experimental power THOMSON-DAG process.

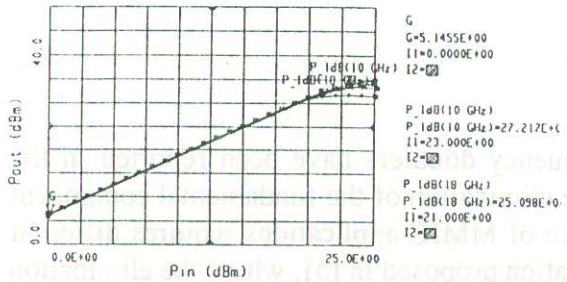

Fig.3 Pout versus Pin

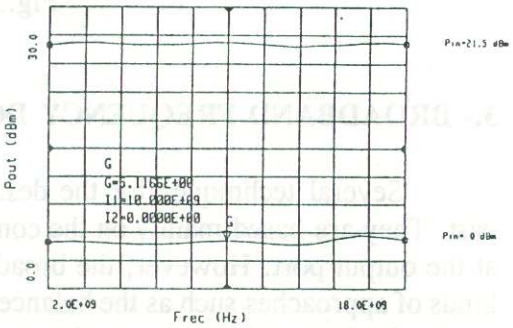

Fig.4 Pout versus Frequency

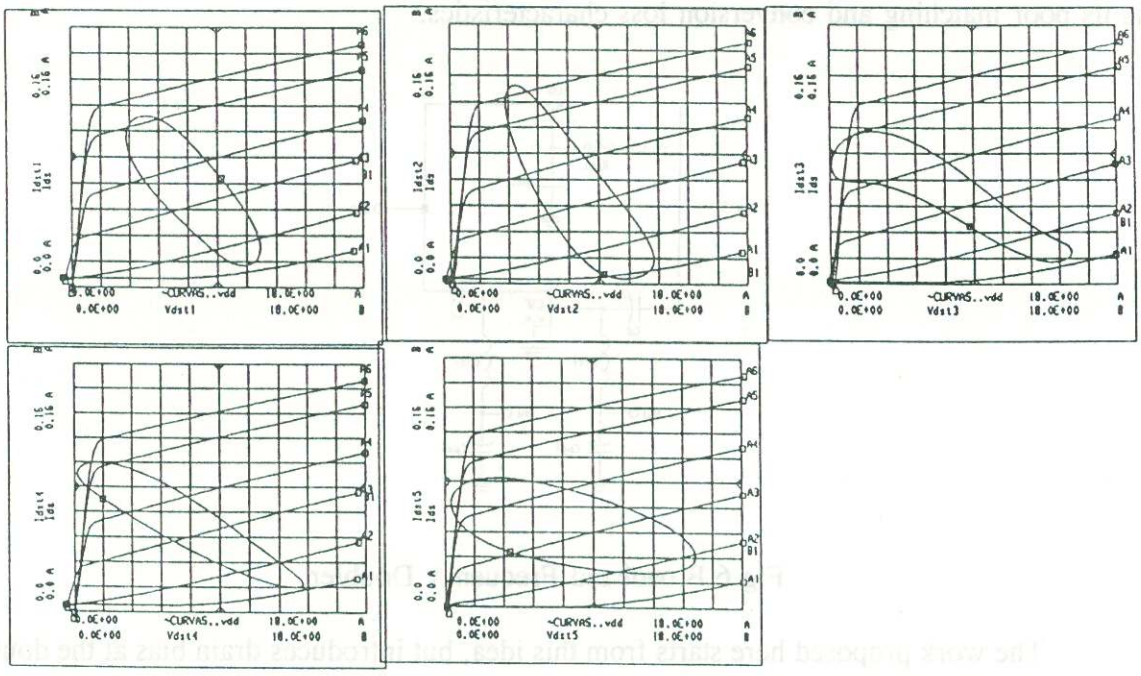

Fig.4 Load Contours at 18 GHz (Pin=21dBm)

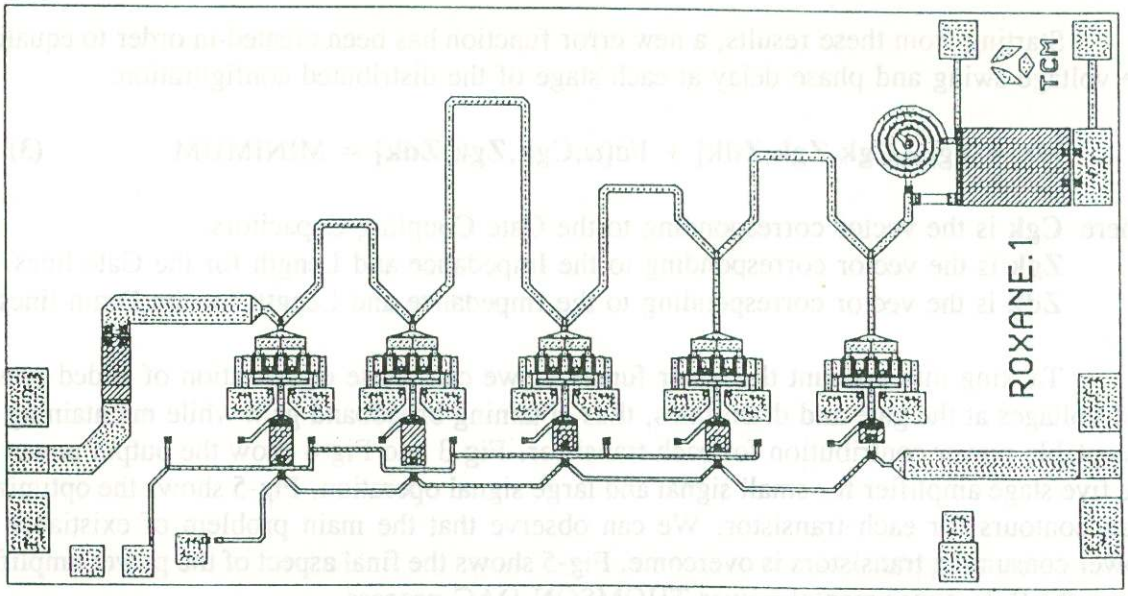

Fig.5 Amplifier Layout

3.- BROADBAND FREQUENCY DOUBLER

Several techniques for the design of frequency doublers have been reported in the past. They are based mainly on the concept of the elimination of the fundamental component at the output port. However, the broadband nature of MMIC applications requires different kinds of approaches such as the balanced configuration proposed in [5], where the elimination of the fundamental content at the output is in a natural form. The advantages of such a configuration, Fig-6, is mainly their simplicity and low size, while the main inconvenience is its poor matching and conversion loss characteristics.

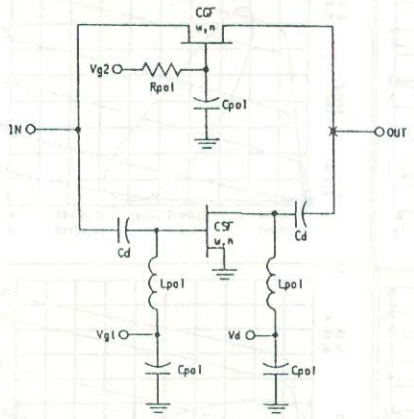

Fig.6 Broadband Frequency Doubler

The work proposed here starts from this idea, but introduces drain bias at the doubler stage and optimizes the overall gate length as well as the bias point. The input port is increased by a simple extra inductor in order to improve the return loss.

Consequently the general mathematical problem is to achieve equalization of the transistor output voltages (fundamental frequency cancel) and to optimize the gate length and bias point in order to obtain a broadband return loss around 15 dB, isolation better than 20 dB and conversion losses better than 8 dB. The Multiharmonic error function proposed here is written in the following terms:

$$Err = F1(\omega, Vgcc, Vdcc, W) + F2(\omega, Vgcc, Vdcc, W) \quad (4)$$

where **Vgcc** is a vector containing the gate bias
Vdcc is a vector containing the drain bias
W is a vector containing the Gate Lengths

It should be noted that the gate length is an optimizable parameter that has a strong influence on the matching and conversion loss properties of this balanced configuration. The minimization algorithm and the constraints for the fundamental and harmonic contents on the output voltages are written in the same terms as (2).

Fig.7 shows the practical realization and Fig.8 shows the main characteristics of the frequency doubler: Input band: 4 to 9 GHz, return loss between 11 and 22dB and isolation between 31 and 18dB for an input power of 10mW, that is, the circuit operating at maximum output power without degradation of the output spectrum.

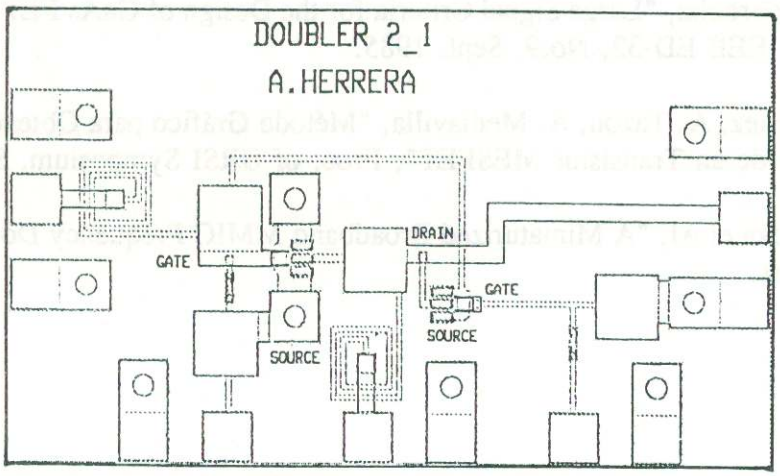

Fig.7 Frequency Doubler Layout

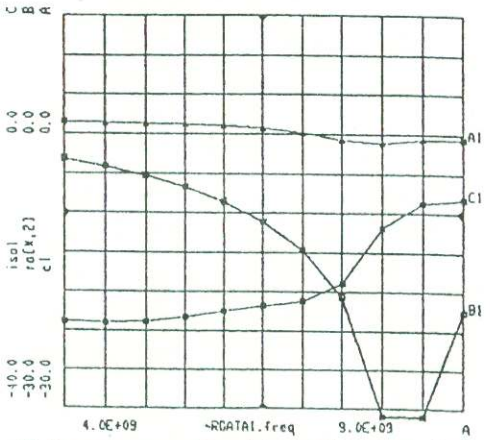

Fig.8 Frequency Doubler Characteristics

CONCLUSIONS

It seems evident that despite the available home made techniques, such as graphical methods or a certain amount of expertise, the numerical large signal optimization techniques are a powerful tool in the design of strongly nonlinear microwave functions. In particular, the use of geometrical scaling of MESFET devices as an extra variable gives excellent results in those circuits that require a maximum of performance, as is the case of MMIC technology.

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