A C-BAND DIRECT DEMODULATION MMIC RECEIVER FOR DIGITAL COMMUNICATIONS SYSTEMS

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ABSTRACT

The feasibility of a microwave direct demodulation receiver has been demonstrated for radio link equipments in hybrid technology [1]. In that case there is no intermediate frequency, so this structure is easier to integrate on GaAs substrate. Having all the elementary functions on the same chip can even lead to a new topology for the MMIC receiver.

Integration interest are a better demodulation performance because of the symmetry of the MMIC circuits and a large useful frequency range which covers several telecommunication bands between 6.4 GHz and 8.5 GHz.

The monolithic designs and realizations of a C-Band direct demodulation MMIC receiver for digital communications systems will be described here. Results are presented for the different circuits which have been independently designed (figure n° 1).

1. LOW NOISE AMPLIFIER

The modulated signal at the RF port of the system is received by an RF gain controlled low noise amplifier. At this input the signal can be as low as -90 dB or as high as -20 dBm in case of overrange. So, amplifier gain must be controlled over 15 dB to keep the RF amplitude at the typical value of -35 dBm. Other characteristics taken into account are the noise factor and the 1 dB compression output power.

The realized amplifier is composed of three stages to achieve these differents goals [2], [3]. The first stage is optimised from the point view of the noise factor. The dynamic range is obtained using a Dual-Gate MESFET (DGFET) in the second stage. The MESFET width in the third stage is large enough to have a 1 dB compression output power higher than 7 dBm. The amplifier chip size is no more than 2 mm from input to output and 1 mm large (figure n° 2).

These circuits have been entirely characterised in S_{ij} parameters at the nominal voltages with on-wafer measurements. For all the amplifiers on the same wafer, the nominal average gain was 18 dB ± 1.5 dB with an input VSWR less than 1.5 and an output VSWR less than 2 in the frequency range 6.4 GHz - 8.5 GHz. With a voltage control range of 2 Volts on the DGFET, the dynamic range is 20 dB (figure n° 3). In order to measure the noise factor of this amplifier, the chip must be set up on alumina carrier. At minimum attenuation, the tested circuits have exhibited a noise factor less than 3.5 dB in the frequency range with a 21 dB associated gain. The degradation with temperature was no more than 0.1 dB per 10 Celsius degrees. Due to the output FET size, the 1 dB compression output power was higher than 7 dBm whatever the input signal was.

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2. DIELECTRIC RESONATOR OSCILLATOR

Several configurations of DRO are commonly used to have a good local oscillator [4]. From the point of view of phase noise, the best solution is a configuration where the resonator is coupled to a microstripline between the gate and the drain of the MESFET. But another good alternative is a dielectric resonator coupled to a microstripline in the gate circuit which structure is easier to implement.

The main part of the DRO is the MMIC circuit which is composed of the MESFET with a source circuit and an active drain circuit. A varactor in the source circuit acts as a negative reaction between source and gate and controls the negative resistance seen from the gate. The active drain circuit isolates the main oscillating circuit from the output load and can present an optimised load to the oscillator MESFET drain (figure n° 4).

A measurement method has been established to test oscillators directly on a wafer. In fact, the output is loaded on the wafer by a 50 Ohms probe whereas the S_{11} parameter is observed at the gate port ; the good circuits present a S_{11} parameter higher than 0 dB. With such a method, 46 good circuits (57%) were found on the same wafer with a static yield of 73%. This step permits to choose a correct site to be installed in a test case.

In that package, the oscillator chip must be linked to an alumina circuit which is composed of the dielectric resonator coupled to a microstripline. With a particular precise position of the dielectric resonator, -100 dBc/Hz of phase noise at 10 kHz from a 5768 MHz has been observed. A smaller resonator leaded to an upper oscillation frequency at 8128 MHz. A resonator position could also be found where the RF noise was always better than -85 dBc/Hz at 10 kHz from carrier whatever the varactor voltage was (figure n° 5). Then, the output power was 12 dBm with a varactor voltage equal to 0 Volt and got down to 10 dBm for a 6 MHz bandwith. This leads to 1 MHz/Volt sensitivity which is sufficient for the modulation access in the receiver.

3. DEMODULATOR

The main part of the demodulator (figure n° 6) is composed of two mixers which must be identical and symmetrical to have a good demodulation performance. So there is of great interest to have an integrated MMIC demodulator.

An original active coupler feed the RF inputs of the mixers. On the LO side, after a Wilkinson divider, signals are phase shifted in order to feed the LO inputs of the mixers with signals in quadrature.

A test version of the active coupler has been measured on the wafer and 23 couplers of the same wafer (64%) present a gain in the range 1.58 ± 0.3 dB. Several couplers were measured in a test case with an input and two outputs. No difference were observed on the HP8510 network analyser either in phase or in amplitude between the two outputs. The VSWR is always better than 1.5 and the 1 dB compression output power is higher than 8.5 dBm whatever the frequency was from 5.9 GHz up to 8.5 GHz.

On the LO side, as regards to the LO level, a Wilkinson divider was preferred. An attenuation less than 4 dB and a VSWR better than 1.5 was found for 36 Wilkinson dividers on the same wafer (95%) in the 5-10 GHz frequency range. This circuit is followed by an attenuator in one way and a phase shifter in the other way. Several circuits in test case have exhibited a 5.8 dB attenuation in each way. With an adequate voltage set on the two "cold" FET's which control the attenuation and the phase, we have obtained the same amplitude and a 90° phase between the outputs in each band from 5.9 GHz up to 8.5 GHz.

The mixer had to be a 180° balanced configuration since the RF and the LO signals share the same band and a filter could not be used to supress LO signal. The operating range for the mixer is 6.4-8.5 GHz for the RF and LO signals and under 100 MHz for the base-band. Because of this latest point, Schottky diodes were selected since they have a better noise figure than MESFET's at low frequencies.

One of the oldest type of 180° coupler is the hybrid ring that splits RF and LO signals between the two diodes in phase and out of phase respectively. But this kind of structure is not compatible with a monolithic implementation in C-band because it requires large GaAs area due to quaterwavelength transmission lines [5], [6]. A monolithic approach of the rat-race is to replace the quarter-wave transformers by their lumped element low and high-pass equivalents. So with the two RF/LO matching networks, the mixer circuit size is 1.5 x 2 mm^2.

The conversion loss are less than 7.5 dB over a 10 MHz to 100 MHz range when LO power is 9 dBm and RF power is-15 dBm whatever the frequency signal was figure n° 7. With an IF frequency of 30 MHz and an LO input power reaches 6 dBm. With a 8 dBm LO power, and operating at the same frequencies, the mixer exhibits a 1 dB compression point of 7 dBm while LO to RF isolation is greater than 20 dB, LO to IF isolation is greater than 40 dB and RF to IF isolation is greater than 30 dB from 6.4 GHz to 8.5 GHz.

CONCLUSION

The first step to the integration of a MMIC demodulation receiver was reached. All the circuits which will be used in the receiver have been satisfactorily designed, fabricated and measured.

These circuits independently realized and tested have been set up on an alumina substrate to evaluate the demodulation performance. But this is not sufficient to build a pratical well-designed receiver. The direct demodulation receiver needs and the MMIC technologie have leaded to define a new receiver configuration.

The next step in integration has taken this specifications into account and now the aim is to realize the MMIC direct demodulation receiver in a few chips with a no more than 10 mm^2 size.

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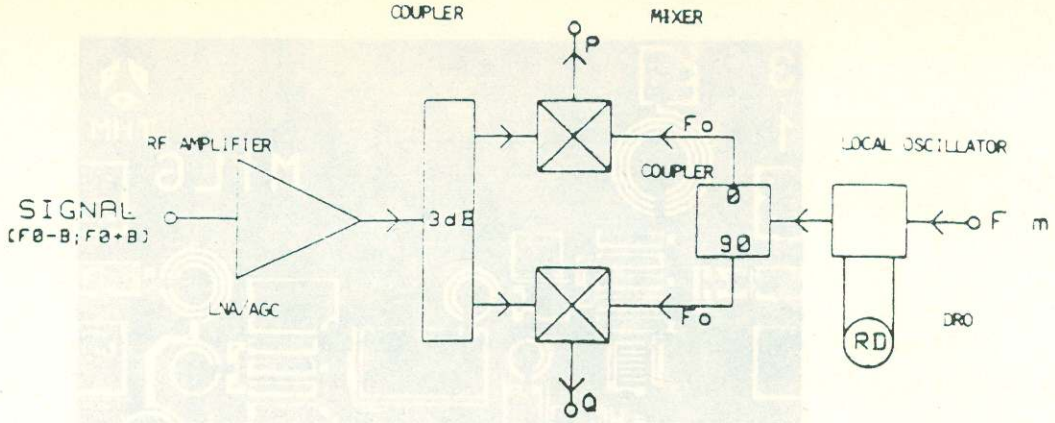

FIGURE N° 1 : DIRECT DEMODULATION RECEIVER BLOCK DIAGRAM

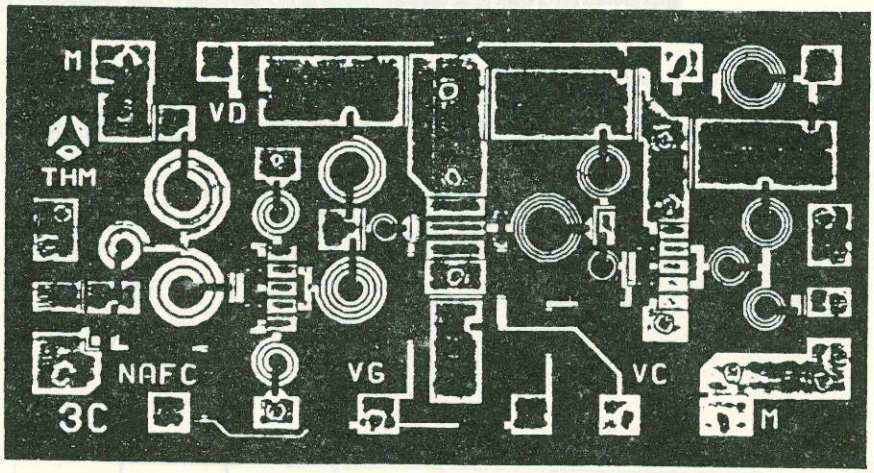

FIGURE N° 2 : THE RF GAIN CONTROLLED LOW NOISE AMPLIFIER

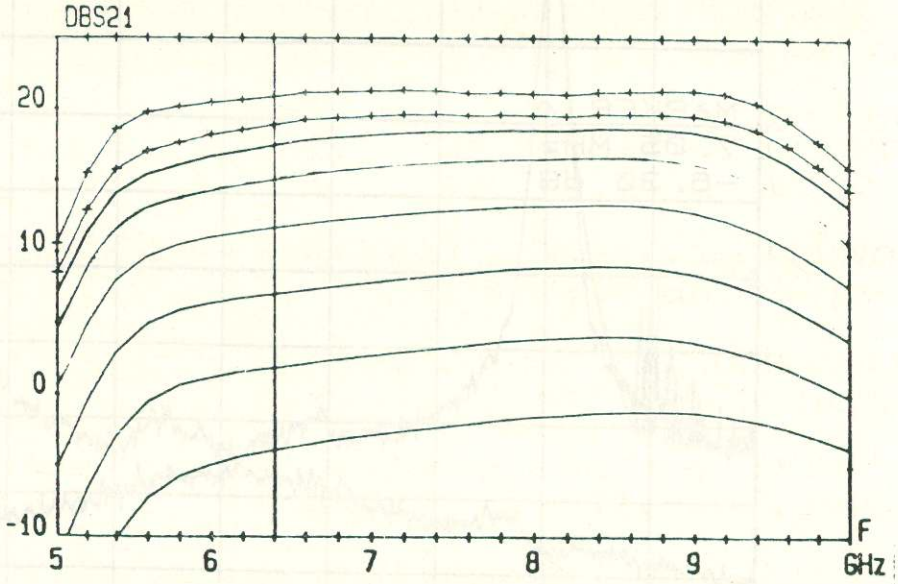

FIGURE N° 3 : DYNAMIC RANGE OF THE RF AMPLIFIER

VC=-1.2V
VC=-1V
VC=-0.8V
VC=-0.4V
VC=0.2V
VC=0V
VC=1V

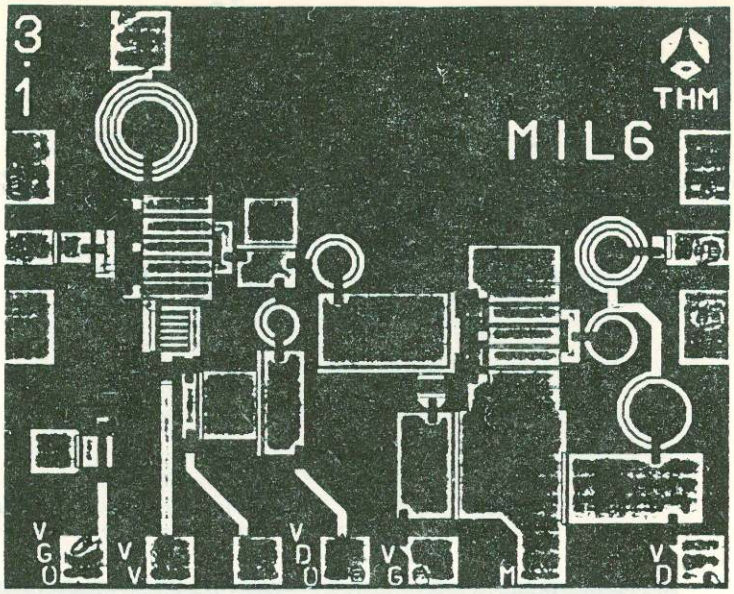

FIGURE N° 4 : THE MMIC CHIP OF THE DIELECTRIC RESONATOR OSCILLATOR

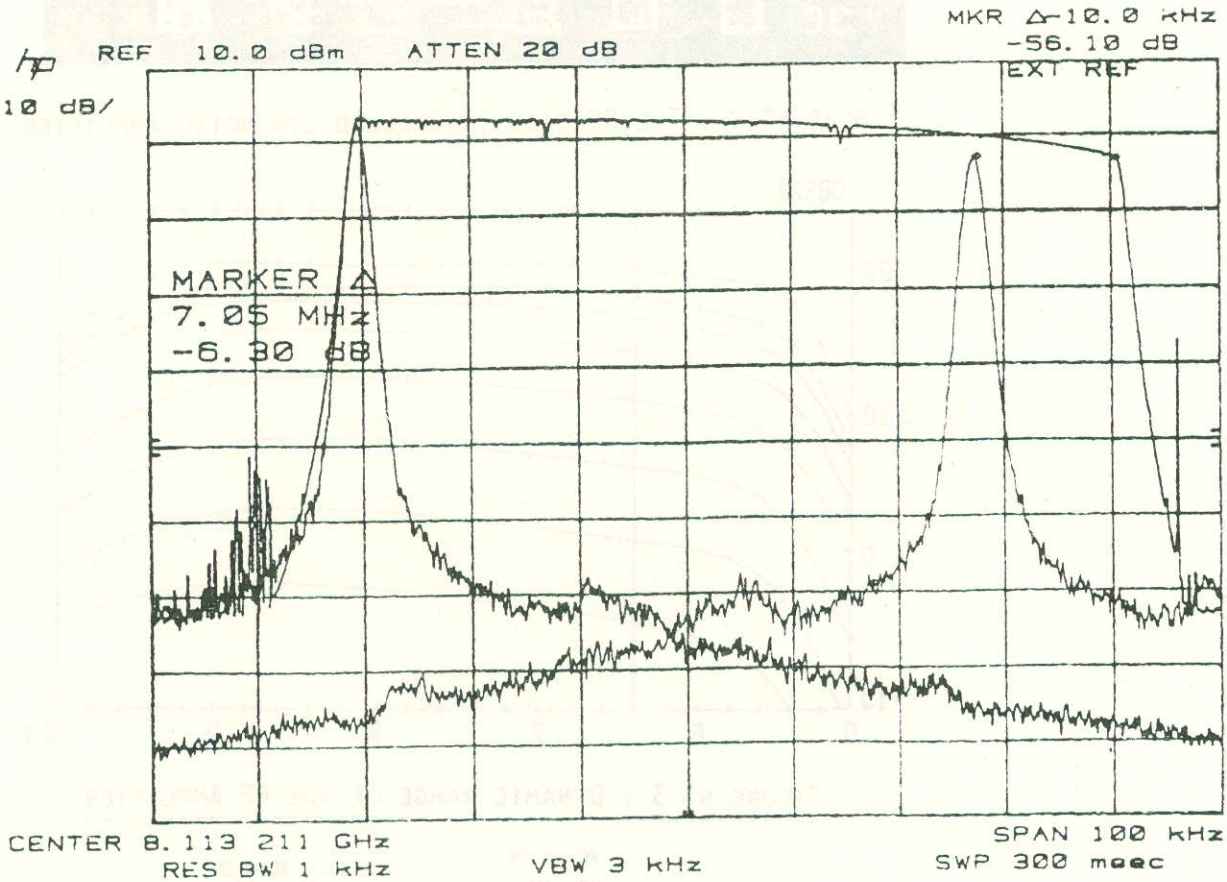

FIGURE N° 5 : SPECTRUM AND BANDWITH OF THE DRO

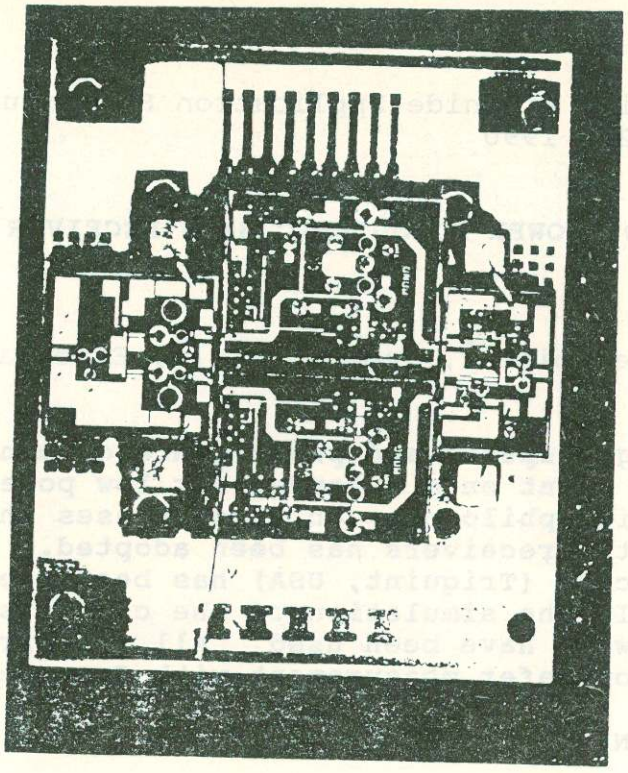

FIGURE N° 6 : THE FOUR CHIP DEMODULATOR

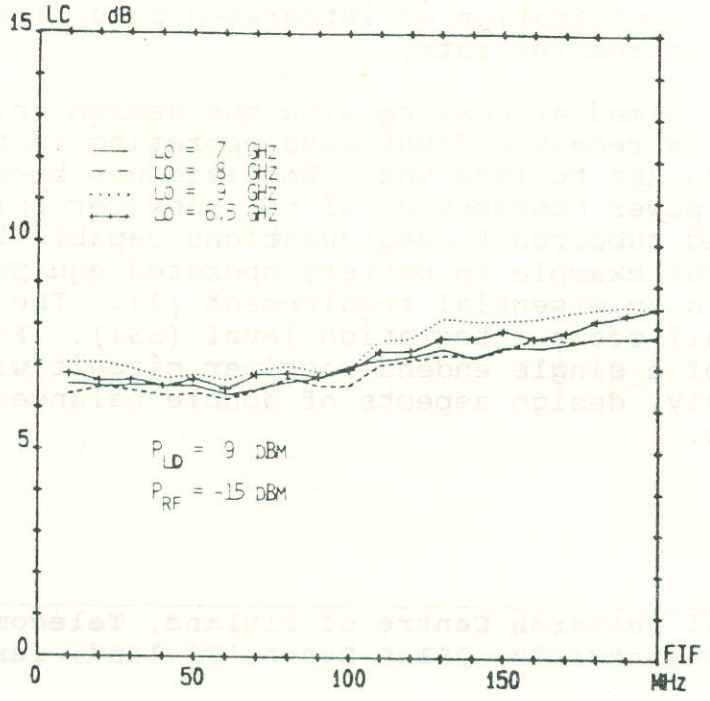

FIGURE N° 7 : CONVERSION LOSS VERSUS IF FREQUENCY