

L-BAND LOW POWER MONOLITHIC GaAs RECEIVER FRONT ENDS

Esa Kemppinen*, Tapani Närhi*, Esko Järvinen*

Abstract - Design aspects and performance of monolithic GaAs L-band receiver front ends intended for low power operation are discussed. Design philosophy which decreases the power consumption of the receivers has been adopted. 1 μm depletion type MESFET process (Triquint, USA) has been used to fabricate the circuits. In the simulation of the circuits MWSPICE and TOUCHSTONE software have been used. All the circuits are accessible for on-wafer measurement with Cascade's probe station.

1. INTRODUCTION

There is a growing demand to integrate a number of functions on one GaAs chip. This applies not only to digital circuits but also to analog microwave circuits. The driving forces of this evolution are economical and technical advantages. Although GaAs technology is far from cheap at present its technical potential, or in general the potential of III-V semiconductors, has well been recognized. With the advent of mass products and reduced price/ mm^2 the exploitation of integrated GaAs circuits is likely to grow with increasing rate.

This paper is aimed at dealing with the design and performance of monolithic GaAs receiver front ends operating in the frequency range from 400 MHz to 1800 MHz. Emphasis has been put on the reduction of power consumption of the receiver chips by employing earlier tested subcircuit configurations capable for low power operation. For example in battery operated equipment low power consumption is an essential requirement [1]. The designs represent small scale integration level (SSI). Firstly, realisation of a single ended receiver circuit will be dealt with. Secondly, design aspects of double balanced receivers will be dealt with.

2. DMESFET RECEIVER

2.1 Circuit design

The schematic diagram of the receiver R3 is shown in Fig. 1. One of the most important design parameters of this circuit has been power consumption. The receiver consists of a low-noise amplifier (LNA), mixer, buffer amplifier for the local oscillator and IF-amplifier. Some flexibility in the design has been achieved by using breakable air bridges. This makes it possible to test the different parts of the circuit independently.

In order to have low current consumption and good noise performance, lossless feed back has been used in the LNA. Cascode configuration provides AGC- function also. With series feed back (source inductance) the real part of the input impedance is transformed to 50Ω . The parallel feed back capacitance decreases the imaginary part of the input impedance which make the input matching easier. Part of the matching has been left to be made outside the chip. For example a simple off-chip series coil or a high pass structure can be used to complete the input matching.

The mixer is a single-ended common-source amplifier with a MESFET acting as a switchable source resistor. The local oscillator (LO) signal controls this resistor and thus the gain of the amplifier. One advantage of this circuit is that the LO feed-through to the IF-port is reduced. In the normal condition, RF-signal is taken directly from the LNA to the mixer at high impedance level. However, an external filter can be inserted between LNA and the mixer in order to reject the image frequency. This mode of operation is obtained by breaking an air-bridge and RF-signal through a common-drain buffer.

Buffer amplifier consists of a common base and an adjustable gain common source stage [2]. Input impedance of the first stage has been designed to 100Ω thus halving the current consumption compared to the 50Ω input impedance version. The second stage employing $75 \mu\text{m}$ DMESFETs is frequency selective having the peak gain at the 1GHz operation frequency.

IF- amplifier employs common drain configuration with a special four- transistor construction. It serves essentially as an active output matching buffer also. It comprises four breakable air bridges and by cutting a suitable combination of them three different output impedances (50Ω , 75Ω and 175Ω) can be realised. The current consumption of the first combination is highest and the current consumption of the last one is lowest.

2.2 Fabrication

The receiver has been fabricated by using 1 μm DMESFET process of a commercial foundry. Figure 2 shows the layout of the circuit. The chip size of the circuit measures 1.5 x 1.5 mm^2 .

2.3 Measurements

On wafer measurements were made by using microwave probe station. Figure 3 shows the measured input impedance of the LNA of the receiver. As can be seen the input impedance curve follows approximately the constant 50 Ω -resistance circle on the Smith chart. The input impedance at 1 GHz is $Z_{in} = 63 - j 264 \Omega$ so that the input matching can simply be completed with an inductance of 42 nH. The noise figure of the LNA was measured in 50 Ω environment with an optional output buffer which is of the same type as the IF- amplifier. The measured noise figure of NF = 3.8 dB was obtained. NF becomes better with the insertion of the off-chip matching coil.

In Fig. 4 are illustrated the output impedance curves for the IF- amplifier when three combinations of the breakable air bridges have been chosen. The output impedance is relatively resistive, with exception of low frequencies.

Measured and calculated results of the buffer amplifier are shown in Fig. 5. The measurement has been made in 50 Ω environment but it must be noted that in real operation the impedance level between the buffer amplifier and the mixer is essentially higher than 50 Ω . Thus voltage mode signal is provided by the buffer to the mixer. It can be seen that the measured results and the simulated ones based on the data provided by the foundry agree well.

The results of the on-wafer measurements of the whole receiver circuit are listed in Table 1.

Table 1. Measured results of the receiver.

Vdd = 6 V	$G_c = 13.5 \text{ dB}$	NF = 12.1dB (DSB)
Idd = 35 mA	OIP3 = 8 dBm	(whole receiver)
	$P_{-1\text{dB}} = -3 \text{ dBm}$ (output)	

It should be noted that the measurements were made on wafer with poor input match to the LNA. Based on the simulation, the external matching coil will increase the conversion gain by 8 dB and improve the noise figure considerably. If an optional band pass filter is inserted between the LNA and the mixer, a notable reduction in the noise figure of the whole receiver would result, as the noise at image- and- IF- frequencies would be rejected.

3. DOUBLE BALANCED RECEIVER

To enhance the performance of the receiver front-end, especially in terms of linearity double balanced versions can be designed. The draw back from the point of view of power consumption is that more active component are needed including phase splitters and double to single ended amplifiers. A reasonable method to overcome this is to use enhancement/depletion mode MESFET process (E/D) instead of the DMESFET process because EMESFETs can provide greater gain than DMESFETs with equal currents. At the Technical Research Centre of Finland the experiences gained from this process have shown, that EMESFETs can be used in the design of MMICs. For example, EMESFETs are less noisier in LNAs than DMESFETs [3]. In amplifier configurations as well as in active phase splitters etc. E/D-process has shown to give reasonable good results. However, careful design is needed because E/D-process is mainly intended for digital design and in analog world such parameters as linearity, compression and noise are very important.

4. DISCUSSION

Design aspects and performance of GaAs monolithic L-band receiver front ends have been discussed. Single ended receiver version resulted in a power consumption of slightly more than 200 mW with a conversion gain of 13.5 dB. Improvement in the conversion gain is possible by employing an external matching circuit. Also improvement in the noise figure of the receiver (12.1 dB, DSB) is possible with an external filter between the LNA and mixer. Double balanced receiver versions result in greater power consumption because of the larger amount of active components on the chip. On the other hand the performance will greatly be enhanced. Further reduction of the power consumption is possible by employing enhancement/depletion process.

REFERENCES

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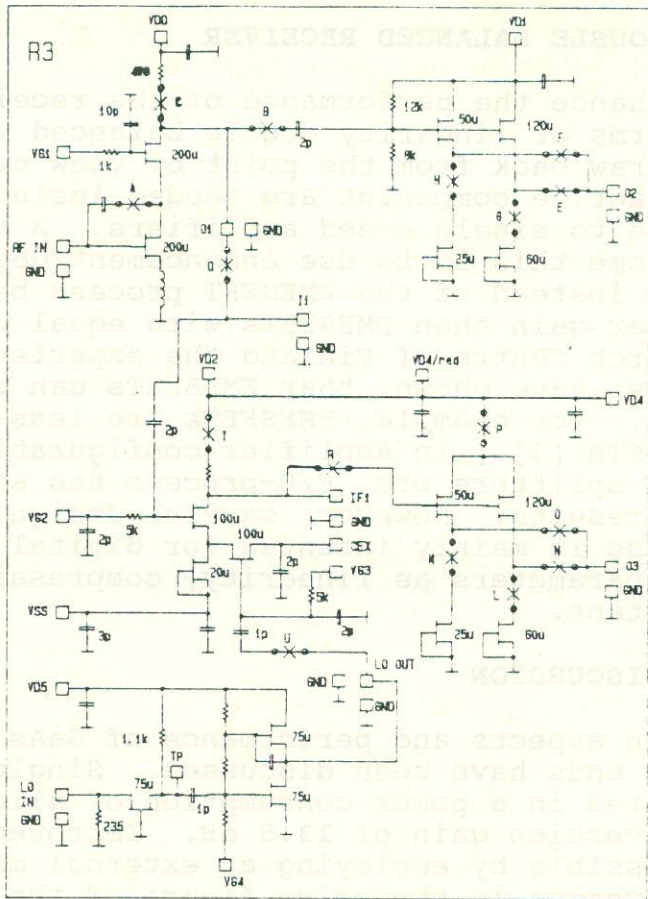


Fig. 1
 L- band receiver R3.

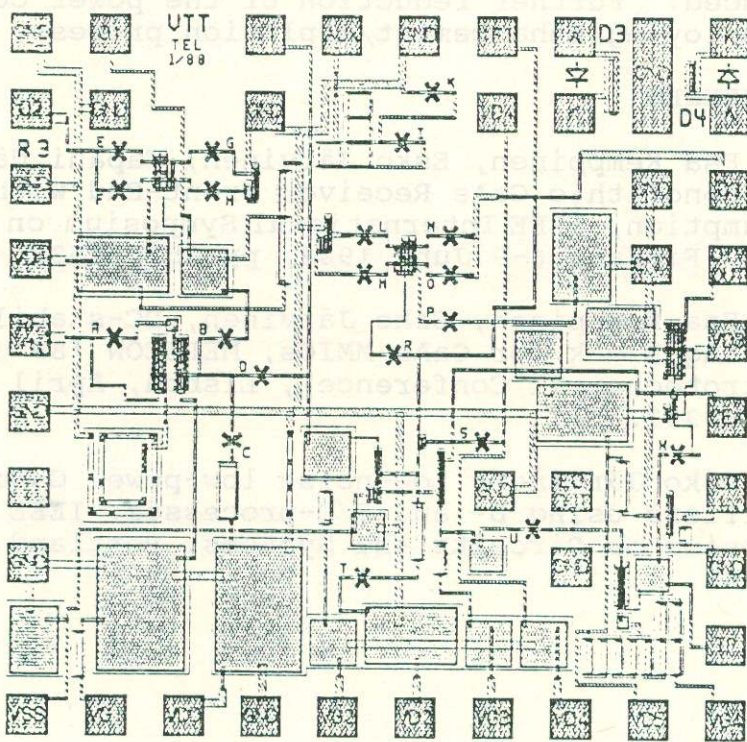


Fig. 2
 Layout of the
 circuit in Fig. 1.

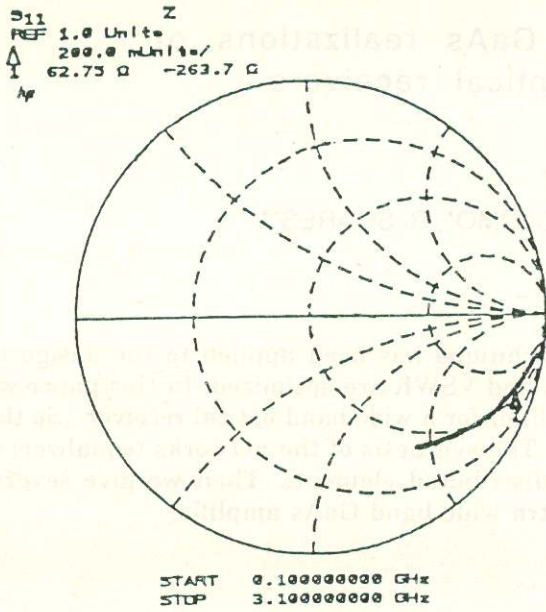


Fig. 3 Measured on-chip input impedance of the low-noise amplifier.

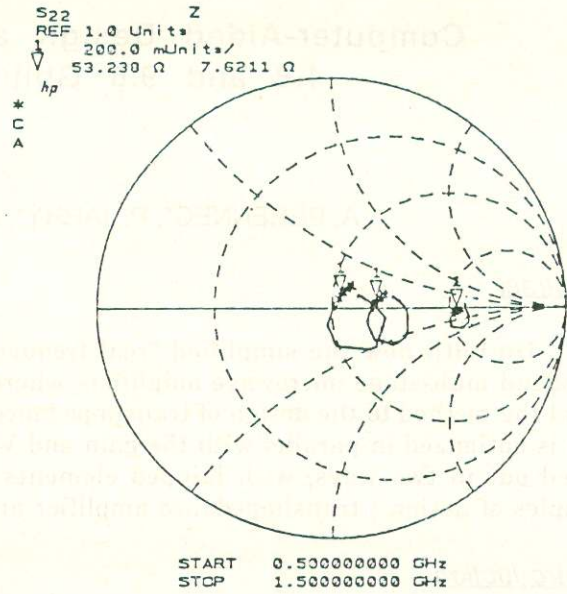


Fig. 4 Three optional output impedances of the output buffer.

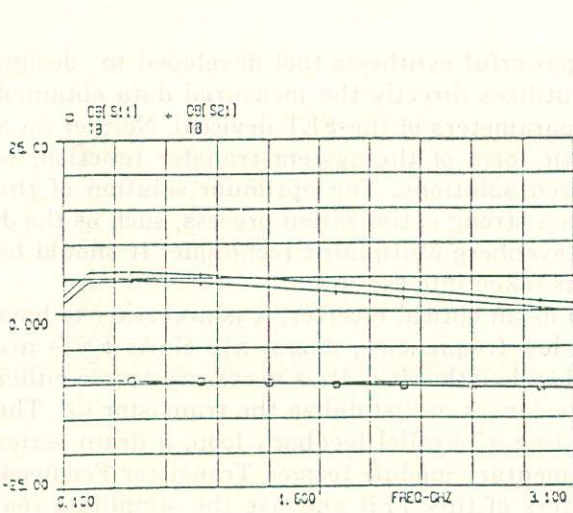


Fig. 5 Simulated and measured S_{11} and S_{22} of the buffer amplifier.