NEAR-FIELD MEASUREMENT OF MICROWAVE ACTIVE DEVICES

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ABSTRACT

A completely new near field mapping system based on micro monopole antenna has been developed in order to determine the electric near-field at the surface of MMIC. The possibilities of this innovative experimental setup are shown by 2D mapping of a bend 50Ω line deposited on GaAs substrate and a coupled-line filter on Duroid 6002. These are supported by 3D electromagnetic simulations. We finally give some results obtained on a real MMIC with a medium resolution of 50µm. The industrial applications are clearly the reliability issues of microwave power devices but also a new tool for MMIC designers. The knowledge of radiated near field will also contribute to optimize the packaging of microwave functions.

INTRODUCTION

With respect to microwaves, an MMIC circuit packaging decreases its performances. The study of electromagnetic mapping allows us to improve MMIC integration and reliability. Currently, the electromagnetic simulation of active devices is very complex. So, the EMC characterization of this type of circuits needs near field measurements.

Some authors propose different techniques using super conducting quantum interference devices (SQUID) [1] [2] or magnetic field probes associated with a scanning force microscope [3] or an electro-optic sampling [4] [5]. All these techniques need a sophisticated and expensive setup.

In order to characterize complex MMIC, we have developed an experimental setup allowing the mapping of electric near-field. Our system has been used in C and X band with a micro monopole antenna. The maximal associated mechanical resolution is about 1 µm.

I- EXPERIMENTAL SETUP

The sample to be scanned is placed on an X-Y displacement driven by a PC (figure 1). The antenna is cascaded with a 60dB low noise, wide band, amplifier. It is possible to insert a double slug adapter between the antenna and the first stage of amplification. The amplified signal is detected and is then transmitted to the PC. A microwave synthesizer allows us to feed (if necessary) the device under test. The main advantage of our method is the possibility to scan a self operating circuit. The PC software controls the displacement, the measurement, and processes the electromagnetic field datas.

Presently the size of the antenna is not optimized (length = 250µm, and diameter = 100µm) This fact leads to some problems as we shall see below.

In order to validate our setup we have chosen to investigate the near field that is located above some very basic samples constituted by a bend 50Ω line loaded either by a short circuit or an open one (figure 2 for the GaAs device setup) and a coupled-line filter loaded with 50 ohms. To remain closer to the requirements of the MMIC manufacturers we have used a GaAs semi-insulating substrate with a thickness of 375µm. The bend line is etched in a 2500Å deposit of Au. Its width (200µm) is calculated to obtain a characteristic impedance of 50Ω at 11.3GHz.

The obtained electric near field mapping is given on figure 3. This measurement is calculated in open circuit condition, the scanned dimensions are 4.5mm x 2mm with a step of 100µm. It is possible to see the standing wave regime. The calculated half wavelength on the line is about 5 mm. The measured distance between two minima (figure 3) gives 5.2mm.

The figure 4 shows the simulation results obtained by 3D electromagnetic simulations (Ansoft HFSS).

The differences between the theoretical results (3D simulations) and the measurements have two main causes. First, the diameter of the probe is too large compared to the width of the line and limits the spatial resolution. The consequence is a spatial integration of the electrical radiated field. This implies that the maximum and minimum of this field are less important.

The second point is the open condition of the device under test. Effectively this structure is connected using wire bonding that induce inductances. The real open condition is not obtained here at 11 GHz.

The second device under test is a coupled-line filter supplied by THOMSON-CSF AIRSYS, but designed for 9.55 GHz on a Duroid 6002 substrate (lower ε_r). The width of this line is about 1.9 mm and the antenna has the same size as above. The result shows the hot spot on this structure as we can compare on the simulation by Ensemble.(figure 5 et 6)

These first results show the interest of such a measurement. Effectively this set up allows us to know the near field with a sufficient dynamic. One could think that the measured field could be at a constant level due to the recombination phenomena and the no-near field conditions. We really measure the field radiated by the line. This measurement has permitted to validate for the first time this kind of approach.

II- MMIC CHARACTERIZATION

After characterizing passive structures with our probe, we have chosen to measure an active device provided by Thomson-CSF Airsys. It consists of a complex circuit composed of different elements (phase shifter, attenuator and amplifiers, see synoptic figure 7). This chip works in the C-band around a central frequency F_0 (the chip is measured at F_0).

Due to amplifiers and attenuators, the power, within the chip, spreads over a large range; that allows us to obtain exploitable measurements for different phase and attenuation states. Considering the electrical aspect, we obtain the power distributions shown in fig.8b and fig.9b (for two different attenuation states but for the same phase state). We know in theory the S-parameters of each phase and attenuation bit, that allows us to foresee approximately the power within the chip. In practice, to get the maps at these two attenuation states, the probe was placed as close as possible from the circuit's surface (about 100µm). Because of the chip supply wires, we can only scan the chip center and not the edges to prevent the breaking of wires. Moreover, to measure high significant fields areas, we have taken a displacement step of 50 µm.

These results are very interesting because they permitted to identify clearly the high field areas. These data are complementary of the electrical simulations. Indeed, we can note that the high field areas follow the power path (high fields are meanly localized near amplifier but also near some inductances in phase shifter (figure 8a and 9a)). This inductance radiation can't be estimated with simulation tools, that's why this method appears very interesting. We can now identify the part of the chip in which the field is the higher. For future designs, the first iteration MMIC's could be measured by this near fields measurement method which allows to locate high fields areas (these regions can generate on die coupling or leakage).This will help to optimize the design more accurately and consequently decrease the number of runs.

CONCLUSION

In this paper we have shown that by means of a relatively simple experiment it is possible to investigate the electromagnetic behavior of a complex MMIC under working conditions. However, this very innovative work is only a first step. Numerous points must be cleared. As an example we must clearly understand the phenomenon that is measured. Then the influence of the probe must be evaluated.

Nevertheless this approach is very interesting for both the device and equipment manufacturer. This kind of map will be a part of a total characterization of a device as the noise figure, the small and large signal parameters, the thermal characteristics… The electromagnetic behavior induces the same problems as the thermal one as an example. The affected parameters are here the reliability and the unexpected electrical behavior. The results presented in this paper are the first step of a global project that will take place in collaboration between industrial partners and universities.

References :

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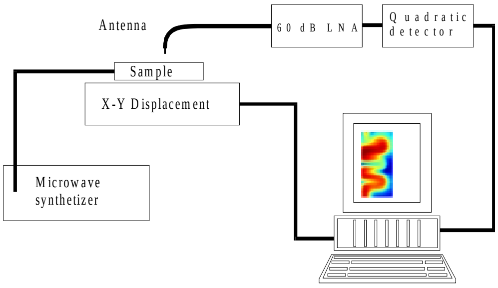

Figure 1 : Experimental setup

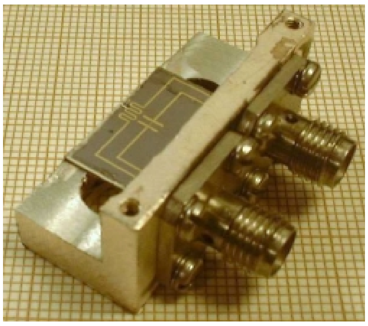

Figure 2 : View of the test device

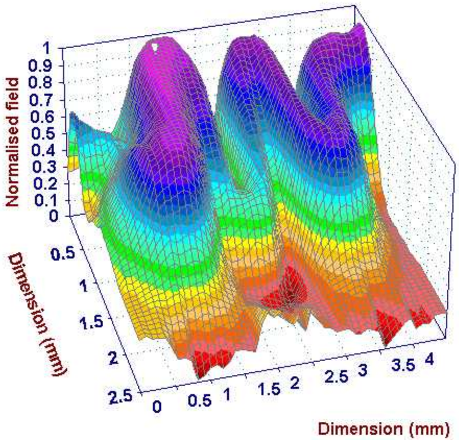

Figure 3 : Measurement

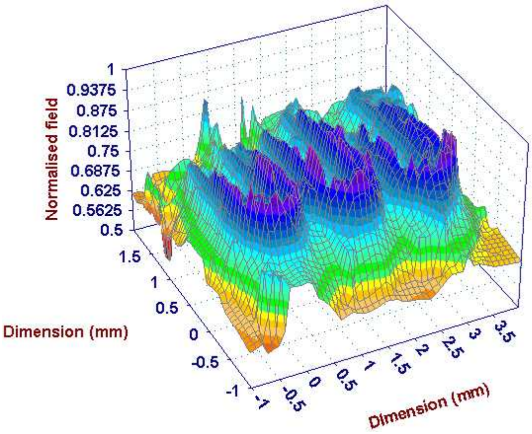

Figure 4 : Simulation

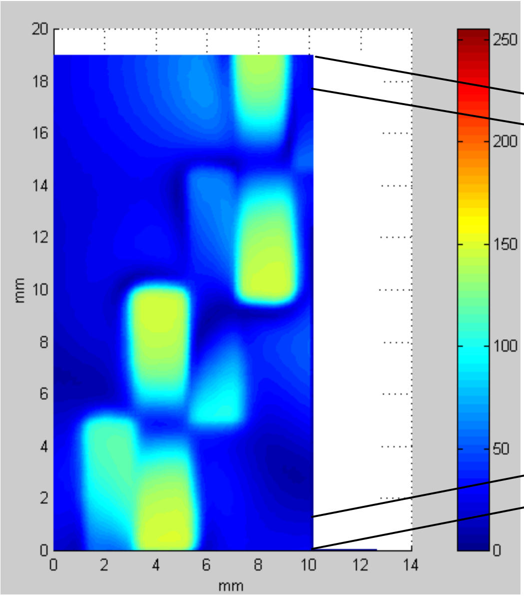

Figure 5 : Measurement(U.A.)

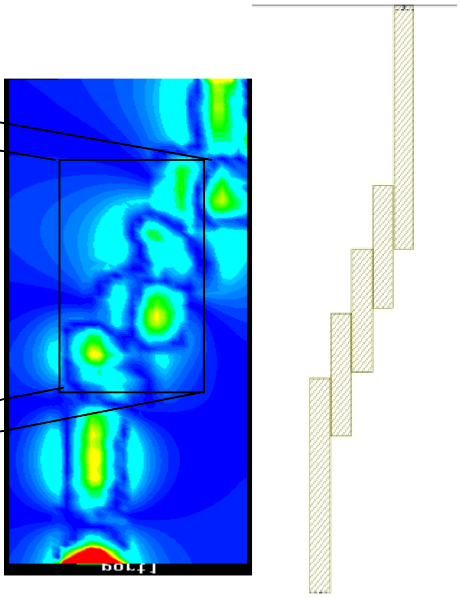

Figure 6: Simulation (UA) and View of the test device

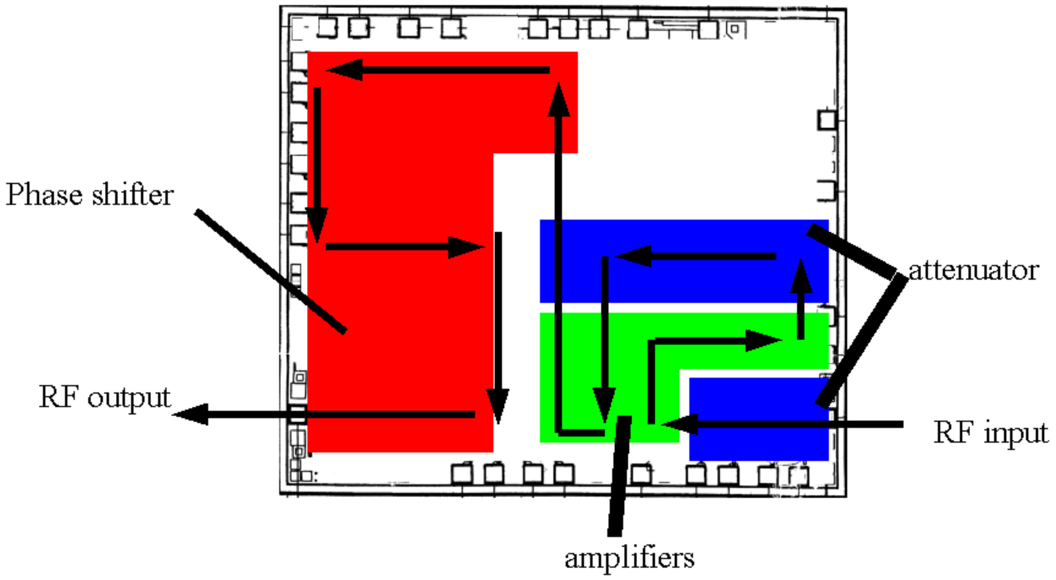

Figure 7: Chip synoptic

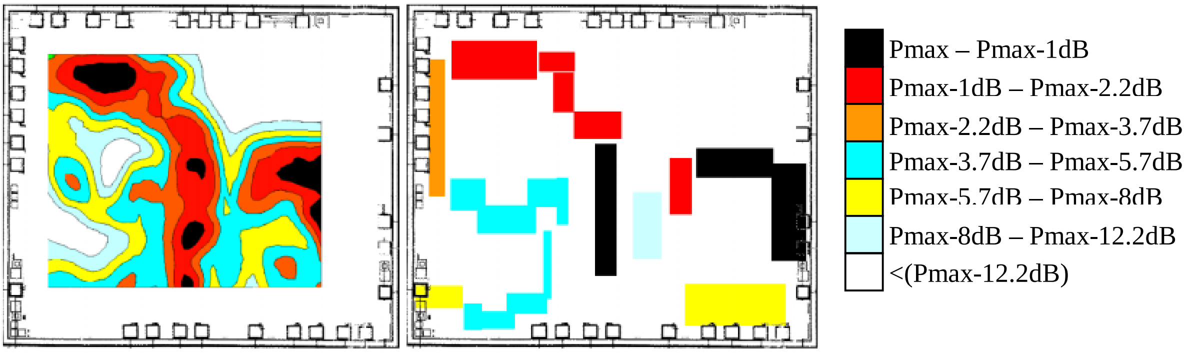

Figure 8a : Measurement *Figure 8b: estimated power*

Low Attenuation

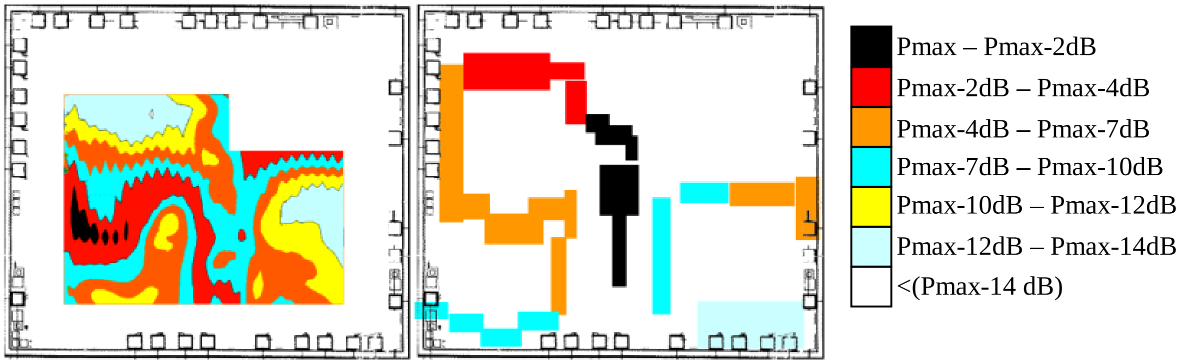

Figure 9a : Measurement *Figure 9b : estimated power*

Zero attenuation