INFLUENCE OF RECESS SHAPE ON THE NOISE AND GAIN PERFORMANCE OF FETs IN THE MILLIMETER WAVE RANGE

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ABSTRACT :

The effect of the recess shape on the FET noise performance is investigated from a theoretical point of view. The noise modelling is based on quasi two dimensional calculation including non stationary transport. The degradation of the noise figure with the recess-to-gate and gate-to-recess distances is emphasized.

I. INTRODUCTION

To provide high noise performance, a field effect device (MESFET, HEMT) has to show low parasitics especially source and gate resistance. In order to reduce the gate resistance, mushroom gate are usually used while the recess structure is used to reduce the source resistance. It is well known that the recess structure (height, width, gate position) is an important parameter determining the device behaviour [1], [2]. However, if some results are available concerning the influence of recess shape on the small signal equivalent circuit and/or the gain, this influence is not well known on the noise performance and this problem constitutes the aim of this paper. In the first part of this communication the noise modelling will be presented while the main results will be given in the second part.

II. HIGH FREQUENCY NOISE CALCULATION IN FET's

In any noise modelling, three different steps are necessary :

(i) calculation of the DC characteristics Ids (V_{gs}, V_{ds})

(ii) calculation of the small signal equivalent circuit.

(iii) calculation of the drain and gate noise sources as well as their correlation coefficient.

At this step it should be emphasized that a noise calculation (2nd order) can be performed if and only if the small signal circuit (1st order) andDC characteristics (0 order) can be given by the modelling with enough accuracy. For this reason, we have choosen to develop a quasi two dimensional modelling including non stationary electron dynamics [3], [4]. For the calculation of the rf and noise performance, the concept of local small signal equivalent circuit has been used. Since it constitutes a key point of our modelling, it seems important at this step to briefly recall this method.

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Basically, each slice of the device is equivalent (figure (1)) to a ΔC_g-g_m-ΔR_d incremental fourpole. These three elements can be deduced from the current Ids, the electrical field E(x) and the amount of free carrier in the slice N(x) [3]. As a consequence, all the device can be described by a non uniform ΔC_g-g_m-ΔR_d active line (figure (2)).

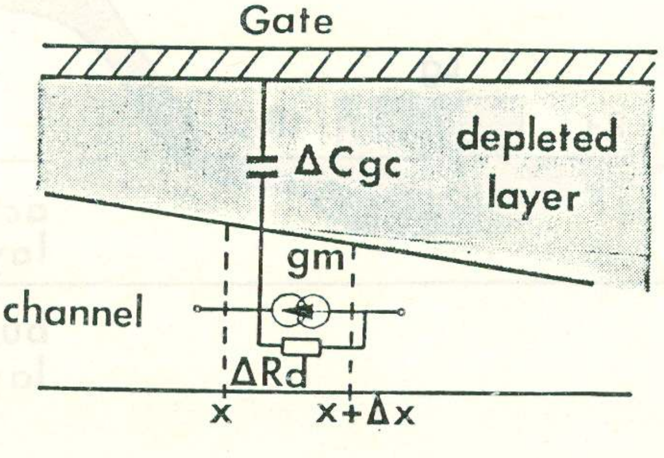

Figure 1 : The local small signal equivalent circuit.

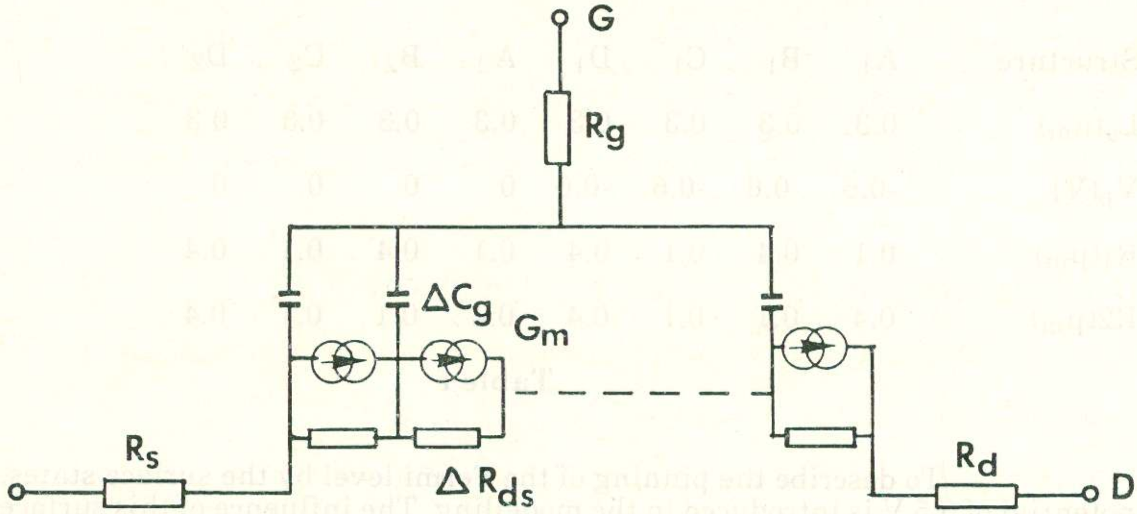

Figure 2 : The FET equivalent active line.

From the knowledge of all the line elements, a simple circuit calculation allows to calculate the equivalent Y or Z matrix of any part of the device between two abcissa x0 and x1 [3]. Obviously, considering the whole device provide the device Y parameters and therefore the small signal equivalent circuit, that can be easily deduced from the Y matrix.

In order to calculate the device noise properties, the impedance field method (IFM)is used. In the IFM, the effect of the noise source located between x and x + Δx is obtained as follows :

(i) the noise current *in* is introduced at x + Δx

(ii) the noise current *in* is removed at x.

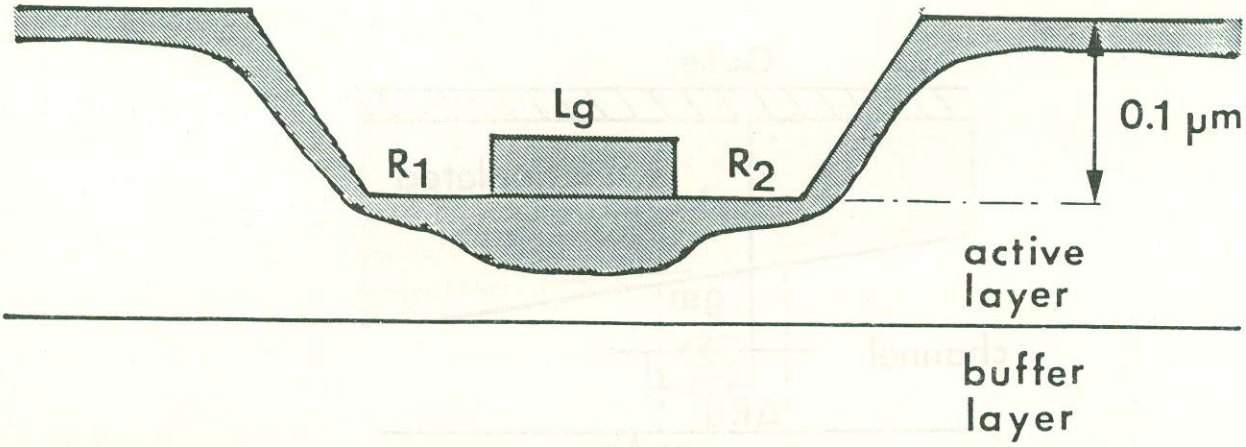

Figure 4 : Investigated structure and definition of the geometrical parameters.

Structure	A_1	B_1	C_1	D_1	A_2	B_2	C_2	D_2
L_g(µm)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
V_p(V)	-0.6	-0.6	-0.6	-0.6	0	0	0	0
R_1(µm)	0.1	0.4	0.1	0.4	0.1	0.4	0.1	0.4
R2(µm)	0.4	0.1	0.1	0.4	0.4	0.1	0.1	0.4

Table I

To describe the pinning of the Fermi level by the surface states, a surface potential of 0,5 V is introduced in the modelling. The influence of this surface potential is very important since it increases the source resistance and can provide an electron heating before their transit under the gate.

II. RESULTS

Table II gives the small signal equivalent circuit, noise and gain performance of the investigated structures. The DC drain current and drain voltage are kept constant ; I_{ds} = 45 mA/mm and V_{ds} = 2 volts. Typical values of extrinsic elements (inductances, pad capacitances, contact resistance...) have been introduced for the noise figure and gain calculation. The operating frequency is 30 GHz. The gate width is 200 µm

By superposing these two states we obtain the drain voltage and gate current fluctuations resulting from the noise source located between x and x + Δx [3]. As a consequence the main problem is to define the drain voltage and gate current fluctuations resulting from the introduction of a noise current at x + Δx. This calculation is carried out using the active line previously define as shown figure (3).

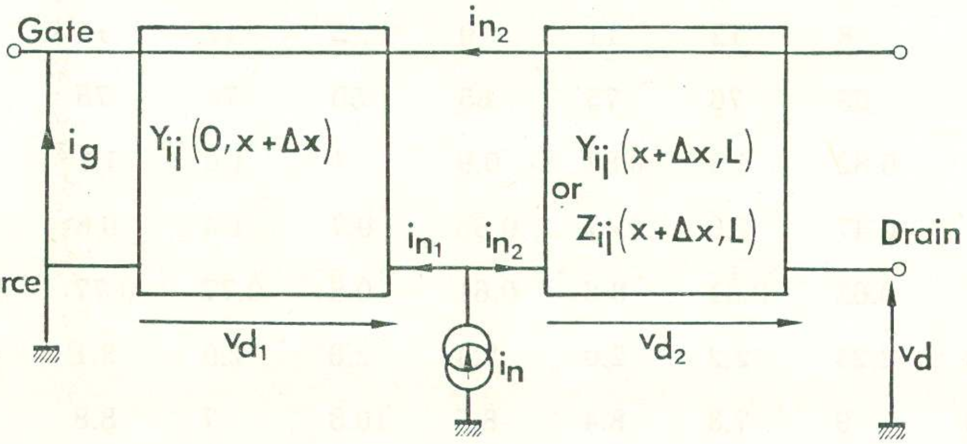

Figure 3 : Basic principle of the impedance field calculation.

Assuming that the noise sources located at two different abscissa are uncorrelated, the total drain voltage, gate current and correlatioin coefficient are calculated by quadratic summation.

Finally it is convenient to transform the drain voltage noise source into a drain current noise source and to define three dimensionless noise parameters by [5]

$$\overline{id^2} = 4\,kT\,g_m\,P\,\Delta f$$

$$\overline{ig^2} = 4\,kT\,Cg_s^2\,\frac{\omega^2}{g_m}\,R\,\Delta f$$

$$\overline{ig\,id^*} / \sqrt{\overline{ig^2}\ \overline{id^2}} = C_{or} = C' + jC$$

In conclusion, the device noise properties are entirely characterized by the small signal equivalent circuit and the three noise parameters P, R and C. Using the method previously described, all these parameters are obtained at any frequency.

Returning now to the recess shape problem, figure (4) shown the investigated structures.

For the sake of simplicity, a conventional MESFET structure has been choosen. The recess is supposed to be V-groove with 45° etch side wall. Two different values of the recess-to-gate distance R_1 and gate-to-recess distance R_2 are considered as well as two differents pinch-off voltage (V_p = - 0.6 V and V_p = 0). Table I summarizes the parameters of the investigated structures.

Structure	A_1	B_1	C_1	D_1	A_2	B_2	C_2	D_2
g_m (mS)	42	38	44	37	42	33	49	30
C_{gs} (fF)	103	80	93	91	131	71	101	97
g_d (mS)	2.74	3.1	3.5	2.4	1.12	1.5	2.2	0.8
C_{gd} (fF)	8	12	11	9	5	12	11	6
F_c (GHz)	65	76	75	65	50	74	78	50
P	0.82	0.9	0.87	0.9	1	1.6	1.1	1.4
R	0.47	0.6	0.47	0.56	0.7	1.4	0.8	1.1
C	0.62	0.61	0.6	0.61	0.8	0.77	0.77	0.81
F_{min} (dB)	2.24	2.2	2.0	2.4	2.6	2.9	2.1	3.44
Gass (dB)	9	7.8	8.4	8.5	10.3	7	8.8	8.7
MAG (dB)	12.4	11.7	12	12	12.7	11.3	13.3	11.1

Table II

Concerning the main parameters of the small signal equivalent circuit, three main phenomena can be observed :

(i) increasing the recess-to-gate distance R_1 reduces the transconductance.

(ii) increasing the gate-to-recess distance R_2 diminishes the output conductance gd, the feedback capacitance C_{gd} but also increases the gate-to-source capacitance C_{gs}. As a consequence, the cutoff frequency fc decreases as R_2 increases

(iii) these trends are more marked in the case of normally-off devices.

Concerning the noise coefficients P, R, C the noise figure and the associated gain the following remarks can be made :

(i) increasing R_1 increases the noise coefficients P and R while the imaginary part of the correlation coefficient C remains nearly constant.

(ii) increasing R_1 and/or R_2 increases the noise figure. This increase is more marked in the case of normally-off devices.

(iii) the gain decreases with increasing R_1.

CONCLUSION

A reduction of R1 and, perhaps in a less extent, of R_2 is needed to provide low noise device in the millimeter wave range. In addition, reducing R_1 and R_2 is more important for low V_p (quasi normally off devices) since the performance degradation is more important in that case. Since the noise mechanisms are similar in MESFETs and HEMTs, this conclusion probably Holds also for HEMTs.

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