2-18 GHz BROADBAND MMIC SPDT SWITCHES
BASED ON GMIC AND HETEROLITHIC CIRCUITS

Charles M. Howell, John J. Regan

INTRODUCTION

Monolithic integrated circuit switches can be fabricated using either GaAs FETs or with PIN diodes as the active elements. Each offers advantages and disadvantages to the circuit design. It has been shown that because of their higher switching Q[1,4] that PIN diodes should exhibit lower loss and higher isolation in the same circuit than a switch made with a FET as the switching element. Conversely, FET based switches offer an advantage of less control power and better DC to RF isolation of the control currents. This paper will discuss a family of MMIC PIN diode based SPDT switches which are designed to give the lowest loss and best isolation from 2-18 GHz.

In order to minimize losses from the passive elements such as inductors, capacitors and RF lines, these are built in a GMIC[3] circuit (glass microwave circuit). The active elements (PIN diodes) are built on a HETEROLITHIC circuit. In a HETEROLITHIC circuit the PIN switching elements are suspended in a low loss tangent, low dielectric borosilicate glass. This glass reduces the normal loss seen in RF lines on silicon or gallium arsenide. It's smaller dielectric also allows larger conductor lines, without excess capacitance to ground.

The GMIC circuit is designed to allow either a silicon PIN or GaAs PIN switch interchangeable as the active element.

Several broadband circuits were built with the designed frequency being 2-18 GHz. Electrical results are excellent, with loss (including all circuit elements) being ~0.8 dB at 18 GHz and isolation being >35 dB.

The following section discusses the design of the switch and a comparison of these switches with GaAs FET SPDT switches used to 18 GHz.

THE SWITCH DESIGN

1) Switch Design

This switch family design effort was performed as a joint effort by 2 widely separated groups as M/A-COM. The HETEROLITHIC switching element was designed and built at the M/A-COM Burlington, Massachusetts semiconductor facility and the bias circuit was simultaneously designed and built in Chandler, Arizona.

The object of the design was to make as small a MMIC switch "chip" as practical that would operate from 2-18 GHz and have a maximum loss of 1 dB and 40 dB minimum isolation.

The actual HETEROLITHIC switching circuit is designed to operate from ~0.1-26 GHz. The switches were simulated and masks designed using Touchstone. The initial CAD design showed a 0.1-26 GHz bandwidth with isolation of ~42 dB at 18 GHz and loss 0.5-0.6 dB. The first wafer run of silicon SPDT's showed actual RF characteristics of loss ~0.8 dB and isolation 38-40 dB at 18 GHz. These results excluded losses of the test holders and it's connectors.

The switch design uses non-symmetrical series and shunt PIN diodes which are spaced ~0.3 mm apart. The actual switching element can use either silicon or GaAs as the semiconductor. The first element was a silicon switch. It uses a glass frame to hold the circuit and to suspend the PIN diodes (see figs. 1&2).

The series diode is electrically isolated from ground by a via at the bottom of the chip which is subsequently filled with a low loss dielectric. The total junction and parasitic capacitance of the series diode is less than 25 femtofarads. The shunt diode is spaced less than 0.3 mm from the series diode and is grounded. Capacitance of the shunt diode is ~100 femtofarads and on resistance $\leq$ 2 ohms. Both diodes have reverse voltage of 100 volts.

Charles M. Howell, Marketing Manager, M/A-COM Semiconductor Products
John J. Regan, Staff Engineer, M/A-COM Semiconductor Products

The diode connections were deposited on the glass frame. The switch has 1.2 mm^2 bonding pads. The process proved very reproducible and SPST, SPDT and SP3T switching elements are made at more than 80% wafer yield. The Touchstone file was then sent to Chandler, Arizona to enable the GMIC bias circuit designer to be able to correctly RF match the switching element with the bias network.

2) GMIC Bias Circuit Design

In order to use a switch with PIN diodes an effective bias circuit is necessary. This bias circuit can require much more area than the switching elements themselves. If deposited on a semiconductor substrate, it can increase circuit loss and decrease yield of good chips.

A GMIC bias circuit can have both lower RF loss and be much less expensive to manufacture. The GMIC process has been developed specifically to meet the requirements of modern military and commercial applications for low cost, highly reliable, reproducible microwave military components. A typical GMIC wafer, with a full circuit, costs only ~20-30% as much as the same size silicon MMIC wafer to fabricate.

The GMIC^3 process uses a layer of low loss borosilicate glass laminated to a silicon carrier. The interface between the two materials is a thick layer of plated gold. The thin film circuit patterns are formed on the exposed top surface of the glass.

GMIC glass is a special electronics grade formulation which has the following attributes:
1) Low dielectric loss at microwave frequencies
2) Thermal expansion coefficient that closely matches silicon
3) Absence of any alkali oxides.

This glass layer serves as a microstrip transmission medium, while the silicon wafer provides both the necessary support and creates an integral carrier for both the bias and switch circuit. The gold film between the glass and silicon provides a low loss ground plane to minimize RF losses (see figs. 5&7).

Passive elements used in the GMIC bias circuit include:
1) Deposited MIM thin film capacitors
2) Chemically milled via holes for ground plane access and semiconductor mounting
3) Air-bridge interconnections
4) TaNi thin film resistors
5) High resolution gold conductor patterns
6) Air-bridged spiral inductors with series resonance of >20 GHz and DC current capability to 250 mA

The initial design of the GMIC was a 2-18 GHz switch bias circuit with <1 dB insertion loss and 35 dB isolation at 18 GHz. The restrictions on total frequency bandwidth were due to low frequency cut off of the spiral inductors. They are ~80% air-bridged over their total length in order to raise their resonant frequency above 20 GHz (see fig. 7).

3) Electrical Performance

Initial electrical characteristics have been far better than expected. Measured RF characteristics of the full switch showed insertion loss to be ≤1 dB up to 22 GHz and 20 mA bias current and isolation 30 dB up to 22 GHz and >35 dB up to 18 GHz. Figure 7 shows the completed 2-18 GHz switch. Figures 8&9 show the electrical performance of the HETEROLITHIC switch element. Figures 10&11 show the completed switch performance.

4) Conclusion

A 2-18 GHz family of PIN diode based MMIC switches have been fabricated that are smaller and have better RF loss and isolation than discrete MIC switches. The insertion loss at 18 GHz of <1 dB compares very favorably with a nominal value of 2 dB for the best FET based MMIC switches. Isolation of <35 dB is equal or greater than most FET based MMIC switches. These switches should be inexpensive to manufacture. Experience on the first ~50,000 HETEROLITHIC SPDT chips indicate their cost and yields are very similar to a single beam lead PIN diode.

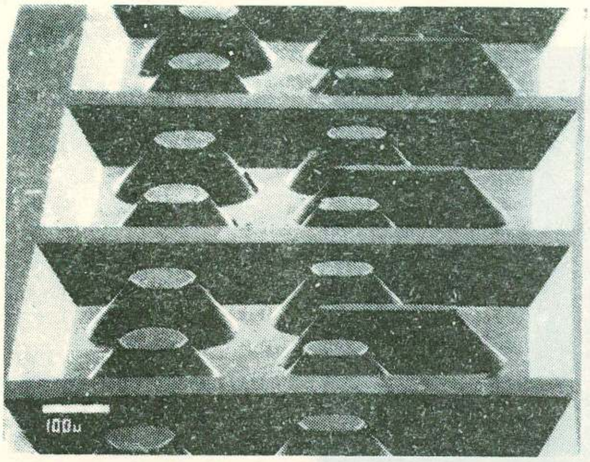

Figure 1. SEM View of the Cavity and the PIN Diodes

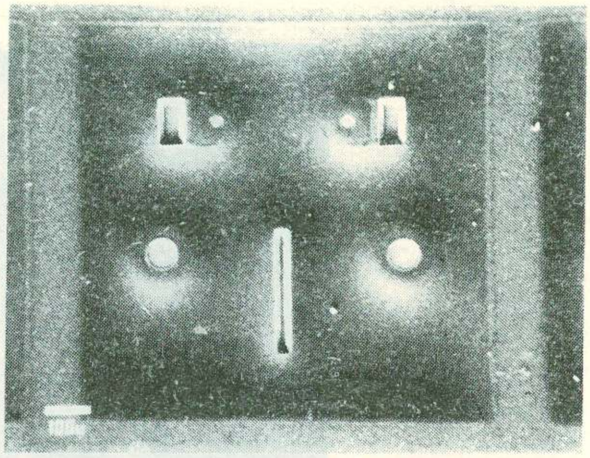

Figure 2. View of the Switch Filled with Glass and Contact Holes

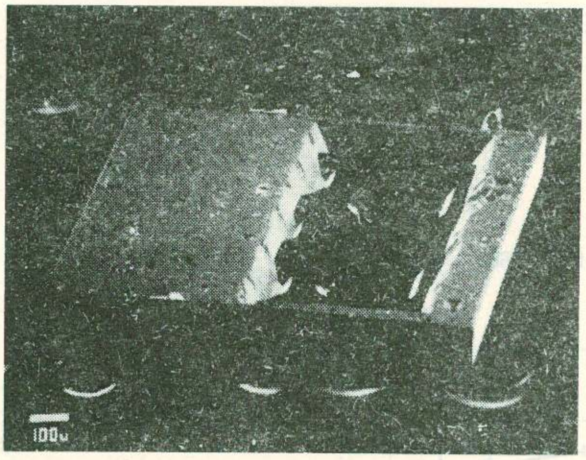

Figure 3. Via Hole to Isolate the Series Diodes from Ground

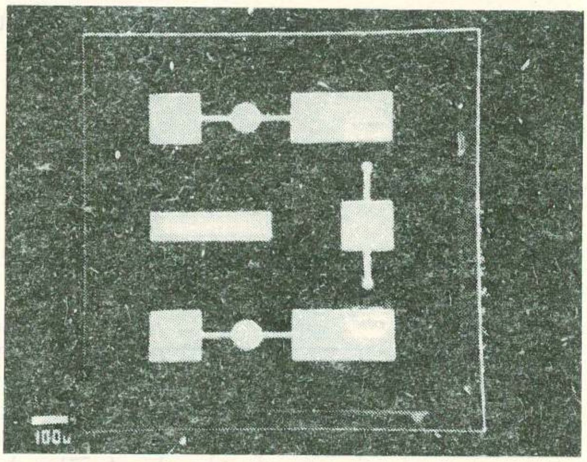

Figure 4. Final Switch Metallization

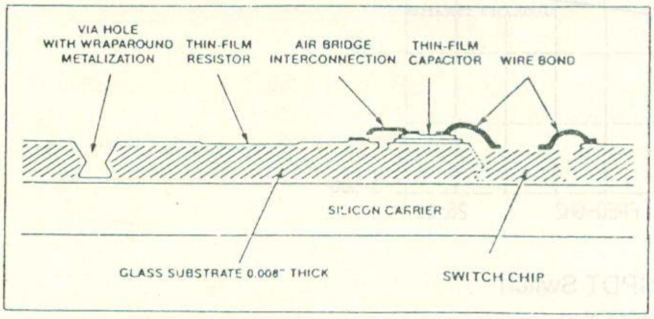

Figure 5. GMIC cross-section

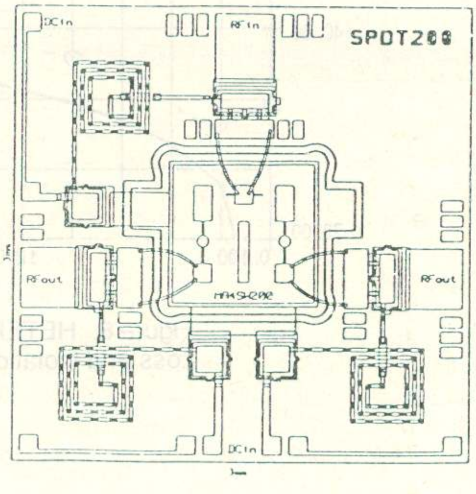

Figure 6. GMIC MMIC SPDT Switch

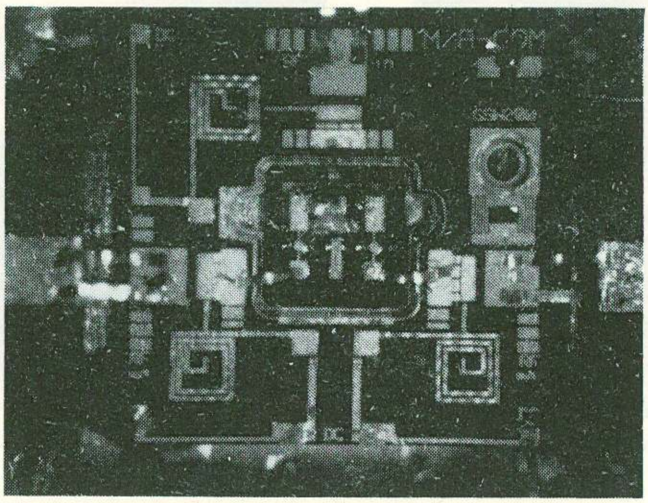

Figure 7. Photo of the Full GMIC Switch in a Test Mount

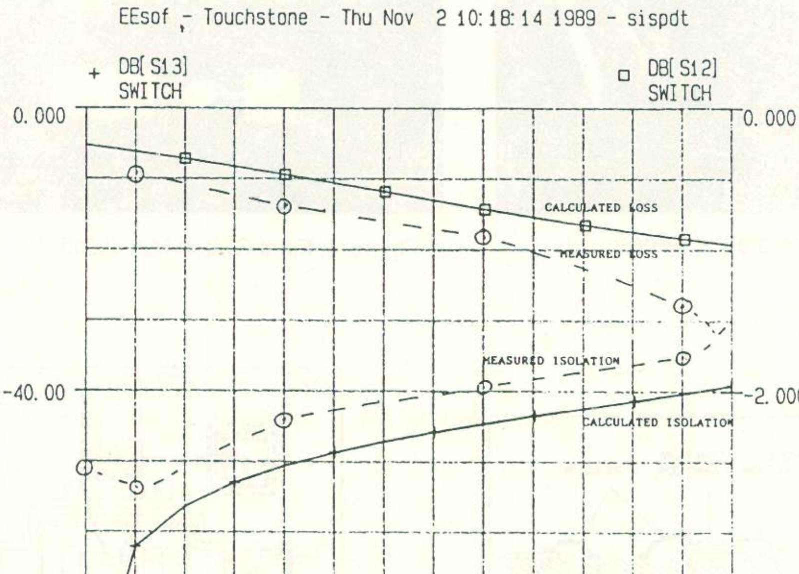

Figure 8. HETEROLITHIC SPDT Switch Loss and Isolation vs. Frequency

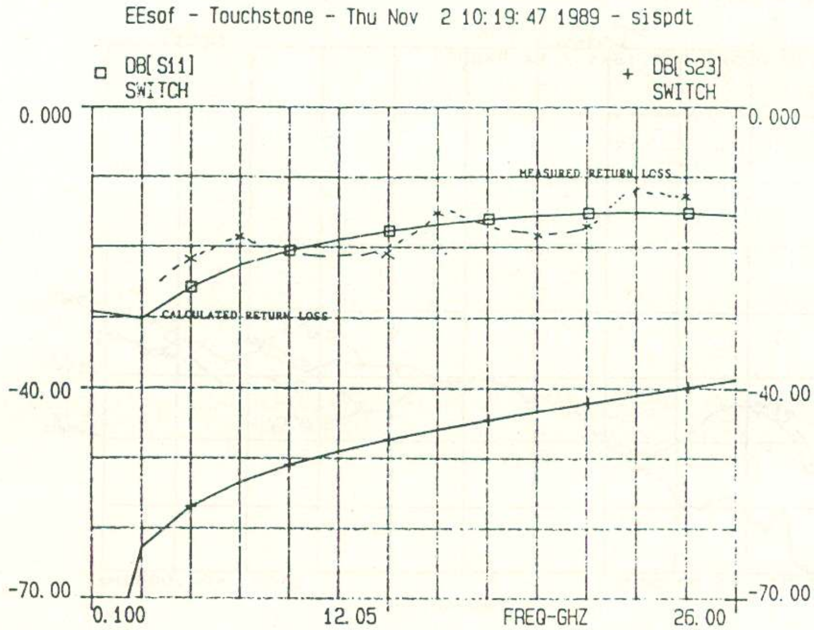

Figure 9. HETEROLITHIC SPDT Switch
Return Loss vs. Frequency

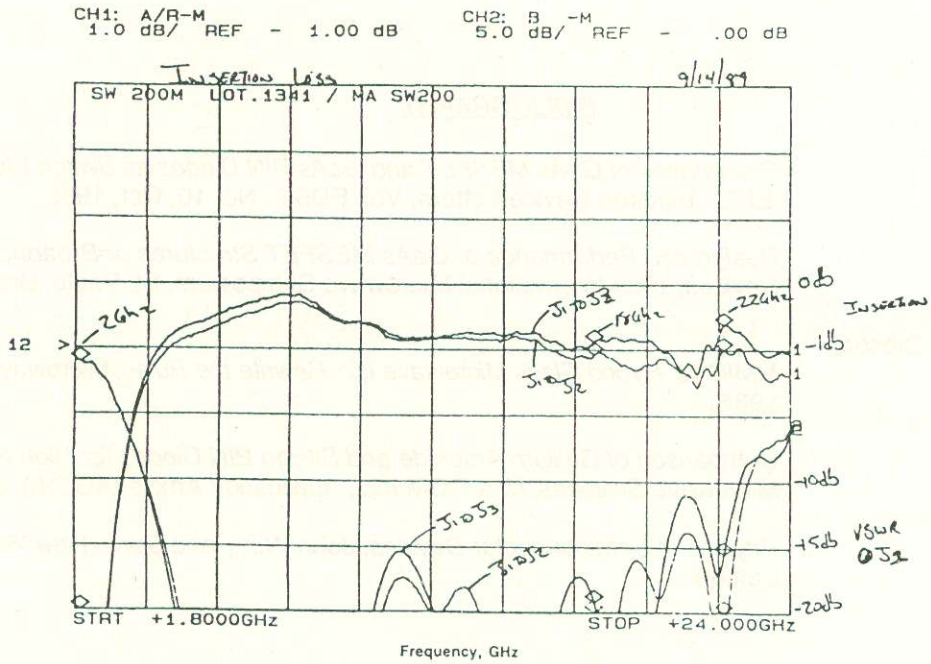

Figure 10. GMIC-HETEROLITHIC MMIC Switch
Performance 2-22 GHz (Insertion Loss and Return Loss)

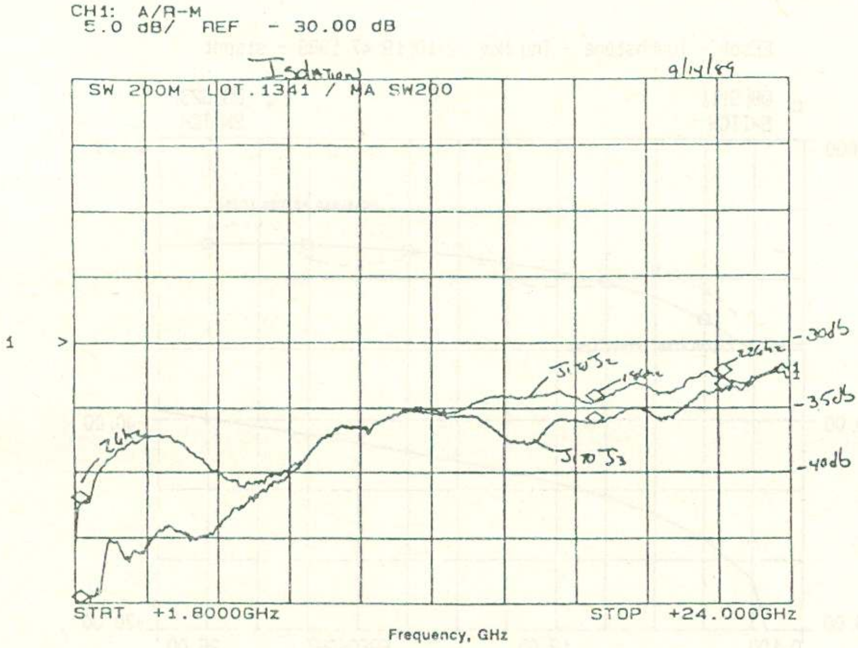

Figure 11. GMIC-HETEROLITHIC MMIC Switch Performance 2-22 GHz (Isolation)

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